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Design and Verification of AHB Protocol using Universal Verification Methodology (UVM)

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***Abstract*—The on-chip protocol is a set of rules on how communication happens between a set of components in a chip. Nowadays, AMBA is the most widely used protocol in soc designs and microcontrollers. There are various types of AMBA protocols based on their features and advancements. Mainly, AMBA consists of three buses, namely, Advanced System Bus (ASB), Advanced Peripheral Bus (APB), and Advanced High Performance Bus (AHB). When compared to the other two buses AHB is a high performance, high bandwidth and for high clock frequency system modules, so the System designers select AHB as their primary choice. Verification is also an important aspect in VLSI domain to verify whether the design works according to the specification and requirements.so, this paper mainly focuses on the design of AHB protocol which supports single master and multiple slaves in Verilog and verify using Hardware verification language such as System Verilog and standard Methodology such as Universal Verification Methodology (UVM). QuestaSim (an Advanced verification tool from Mentor Graphics) is an EDA tool used to simulate and verify the design.**

***Keywords*— AMBA, AHB, APB, ASB, OCB, SOC, UVM**

I. INTRODUCTION

Communication protocols on microcontrollers have been implemented from UART agreements to AMBA. Among these AMBA agreements are the most commonly used microcontroller contracts today, as they have many features and different versions based on their specifications. It is an open standard, in the definition of chip interconnect for connection and management of active blocks in the system on the chip. They are even used on smartphones, gadgets and a wide range of chips. The AMBA family contains several versions of the AMBA protocol that will be distributed in this paper on an ongoing basis. AMBA is widely accepted by many industries due to its versatility and different versions that can be used in all different sub-controls, AMBA is compact and flexible compared to other basic principles which is why it is widely used.

AMBA has three buses, namely Advanced System Bus (ASB), Advanced Peripheral Bus (APB), and Advanced High-Performance Bus (AHB). The ASBs (Advanced system buses) used to describe the most efficient buses can be used in embedded microcontrollers. Advanced Peripheral Bus (APB) is used for low voltage bandwidth connection. The AHB bus is the latest generation of AMBA bus that aims to manage the needs that meet the requirements of a well-functioning design style. A standard system bus that supports multiple bus managers and provides high bandwidth performance. AMBA AHB uses the features required for standard, advanced clock systems.

AMBA AHB-lite is one of them A simple type of AHB with only one master and many slaves. Therefore, there is no need for complex things about confirming mediation or retrying.

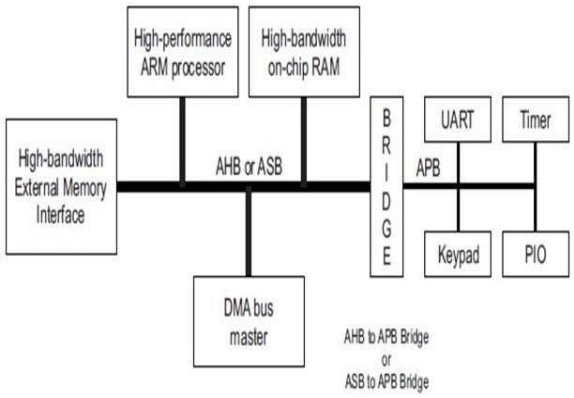

Fig. 1 AMBA bus Block Diagram

The figure shows the standard AMBA-based football design using AHB or ASB protocols for high bandwidth connections and APB protocol for low-bandwidth peripheral interconnects. The AHB or ASB bus provides high bandwidth connections between the elements involved in most transmissions. Also, there is a bridge to the low bandwidth of the APB where most of the peripheral devices in the system are located.

Verification is the most important aspect of the VLSI domain. All soc designs designed must be verified to determine their functionality, whether they operate according to the information provided or not.

Verification increases the productivity of the semiconductor industry but the verification process must be fast and efficient, so in order to get effective authentication we use UVM (universal authentication method). UVM is a standard procedure to be followed in the authentication process. It is faster, reusable, efficient, and portable compared to other verification processes.

In this Paper, we focus on the development of an AHB protocol that supports one master and many slaves, in Verilog and ensures the use of Hardware verification language such as System Verilog and standard Methodology such as Universal Verification Methodology (UVM). QuestaSim (Advanced Verification Tool from Mentor Graphics) is an EDA tool used to mimic and validate a design.

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II. LITERATURE REVIEW

Design and validation of an AMBA AHB bus that includes one master and a multi-slave design in the descriptive language of Verilog Hardware and displays the output of literacy performance. [1] The design under test is verified using Verilog system environment. This paper tells us that the cover report received is small. Questa sim is an EDA tool used to find simulation output.

The paper introduces the Design Method [2] main functional interaction and slave interaction based on a limited-language machine that describes the Verilog hardware and uses the Mentor Model sim 10.03a image tool to simulate and design integration is done with Xilinx. ISE design tool. The completed AMBA AHB system was then tested to determine the correct link between the master and the slave. This article tells us that it does not use verification language similar to Verilog system.

In this case the successful design of the AMBA controller is designed and tested [3] to read and write tasks using the Xilinx template. Literacy activities using AMBA are illustrated with simple examples.

As reported in the paper [4], AHB's main interface and arbiter interface are designed using state-of-the-art equipment in the descriptive language of the Verilog computer hardware and the design simulates with the help of Questa Sim. The AMBA AHB system was then tested to ensure that the interaction of the king and the slave communicated in a non-judgmental way.

The above review tells us about a lot of work related to the descriptive language of Verilog computer hardware and a lot of work to be done on authentication. The current function uses verification language such as Verilog system and standard operating system such as UVM (universal authentication method).

III. DESIGN METHODOLOGY

The Design Under Test (DUT) Block diagram contains many masters and slaves. The master is m1 and the slaves are s1, s2, and s3. Key as address and control signals like HADDR, HTRANS, HBURST and HSIZE. Slave as address and control signal like HADDR, HREADY and HRESP. Drawing of DUT block such as master blocks, slave, decoder and Multiplexor blocks.

The Master sends the transmission by dialing control signals and directs these signals containing information about the width of the transmission direction of the address and even indicates the transmission performing the explosive function. There may be a single transmission and the increasing explosion does not wrap around the boundaries of the address and the explosion of the Wrap wraps around the boundaries of a particular address. The data is transferred by the data bus from the master to the slave in the same way read the data bus is moved from one slave to another. All transfers contain data category and address category, a considerate servant cannot request an address category. All slaves should be able to sample the address, this time one slave can ask the master to expand the data section with the H-READY signal. When the signal is low, it causes the waiting conditions to be included in the transfer and allows the slaves to have more time to provide or sample the data. The slave uses the H -RESP signal used to indicate the failure or success of the transfer.

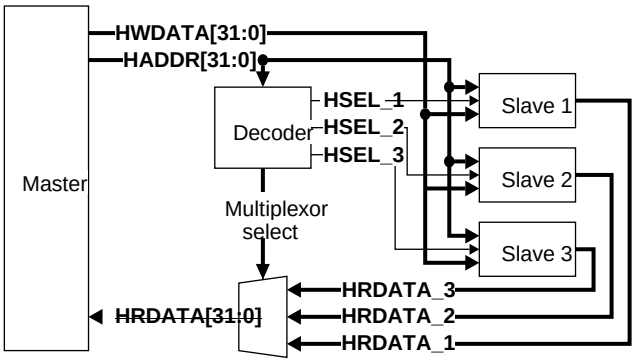

Fig.2 AHB block diagram

Figure 2 shows an AHB-lite block diagram with one master and a multi-slave configuration system. The bus interconnect logic contains address recorder, and slave-to-master multiplexer. The decoder is used to monitor the address from the master to select the required slave and multiplexer routes corresponding slave exit data back to the master is how AHB-lite performance occurs.

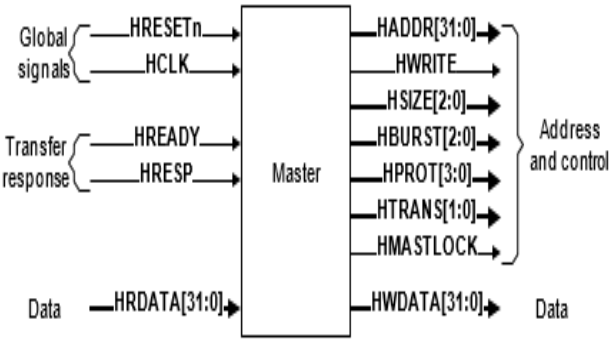

Fig.3 Master interface

Figure 3 shows the AHB-lite master responsible for the reading and writing function in the protocol. It consists of transfer response signals that keep the master and slave transfers, global signals are not washed and reset as is the whole process which is why they are called global signals, address and controls are the ones that deal with transtransfers. and maintains transmission and response control, and there are data signals that roll the data in and out of the specified transmission.

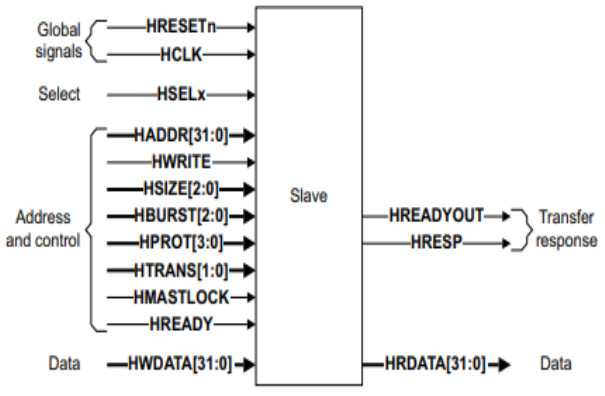

Fig.4 Slave interface

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Figure 4 is an AHB-lite slave that contains the identical signals because the Master but out of the Master is that the slave input. and there's a particular signal selecting the desired slave for this function.

Decoder determines the address of every transfer and provides the chosen signal of the slave involved within the transfer. It also provides an impact signal in multiplexor.

A multiplexor from slave to master is required to multiplex the read data bus and response the signals coming from the slaves to the master. The decoder provides control for the multiplexor. one centralized multiplexor is required altogether implementations that use two or more slaves.

IV. VERIFICATION METHODOLOGY

Due to the increasing complexity of designs and circuits these days validation is required to avoid chip failures. But no matter how good the certification works or not, there are methods in the authentication domain but many industries use UVM as their certification method because of its efficiency and reusable environment.

RTL designs and circuits are validated using the same design language i.e., Verilog language using a test bench, but later as the complexity of the region grows these conventional methods were difficult to use as they had many problems such as delay delays and slow process, then, later. Going forward, they suggested a language that could be used in both the formulation and advanced verification called System Verilog.

System Verilog is presented in both design and validation, much more advanced than the Verilog language and more flexible than the descriptive hardware language. the Verilog system is set up as the IEEE 1800, the Verilog system is based on the Verilog with some enhancement and expands into a transition to Verilog.

The universal verification method is a framework for system verilog classes where we can build fully functional test benches. The design of the RTL (Register transfer level) is verified using the Standard Method such as Universal Verification Methodology.

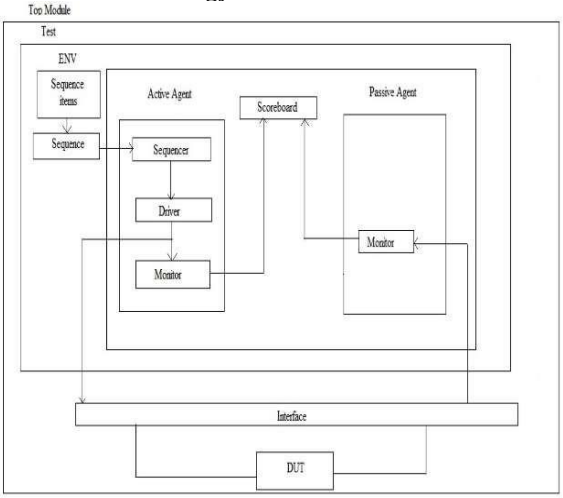

Fig.5 Universal Verification Methodology(UVM).

Universal Verification Methodology includes a basic classroom library encoded in System Verilog. A validation engineer can perform different parts of the validation by extending these components. In addition, UVM provides a number of useful verification features such as using macros to perform complex tasks and creative industries. Figure 8 below is a UVM area. Environment combines interface with DUT with test bench. The test bench area consists of agent, tracker, and driver and monitoring as small components.

Tracking item: Using the uvm_sequence_item section, transactions are extended to send random data to the driver for bus call. Field automation macros are used on these class members as well.

Sequence: A series is a series of actions. In the sequence phase, users can create complex interventions. This sequence can be randomly extended, expanded to create another series and can be merged.

Tracker: The flow of data between the Tracker and the driver is signed in the confirmation part of the sequence. The sequencer has an integrated sequence collection called a sequence library. The sequence set used by the scanner is called the sequence library. This type of component is also known as a driver sequencer.

Driver: The driver collects the object in sequence and moves it to the next lower level such as DUT (Design under Test) using the interface. Produced by expanding uvm_driver.

Monitor: DUT signal monitoring samples using a virtual interface are converted to packet level and then sent to other components, such as score boards for analysis. Done by expanding uvm_monitor.

Agent: Agent contains verification components such as driver, monitor, collector and tracker. It was common to connect these components using a TLM connection. Agent as one of the most effective or efficient methods. In active mode, the agent starts the driver, the sequence tracker and monitors while in the operating mode it only starts monitoring and adjusting.

Environment: The Environment class consist all the sub components such as agents, driver and monitor etc. and configures them.

Testbench: The uvm_test class tells the test cases for the test bench mentioned in the test. The Different test cases is applied to enable the configuration of the test bench and verification components. The uvm_test is wrote by extending from the uvm_component.

V. RESULTS AND DISCUSSION

The Figure 6 shown below shows the simulation output for AMBA AHB protocol. Figure 7 shows the UVM testbench Waveform for single master and four slaves.

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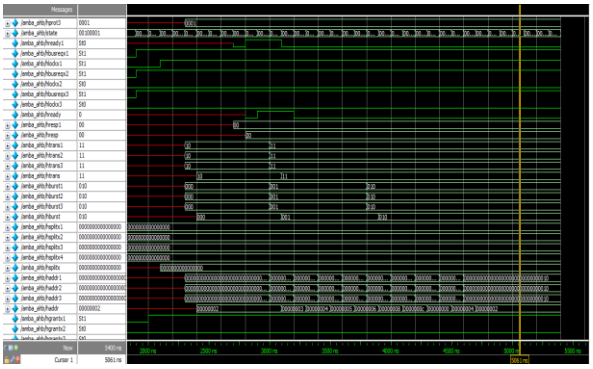


Fig.6 Simulation result of AHB protocol

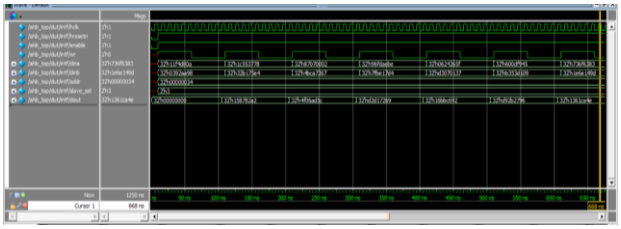


Fig.7 UVM testbench environment

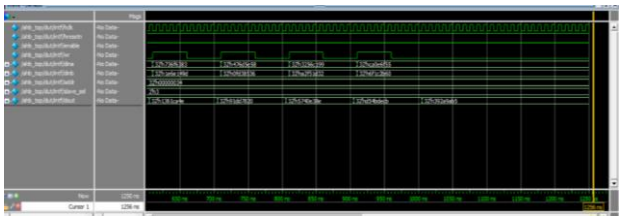
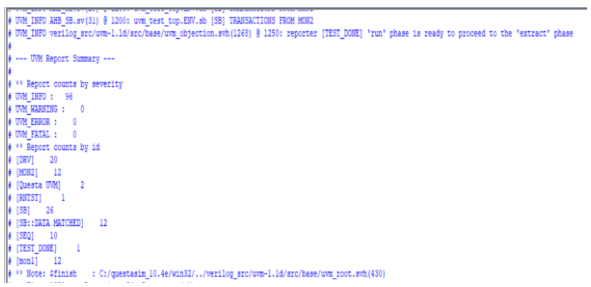


Fig.8 Extension of UVM testbench environment

UVM report gives information about the result obtained after Simulation of UVM test bench. Figure shown below the UVM report generated after passing all the UVM phases. UVM_INFO in the report conclude that there are 96 information messages. The UVM report Summary explain the design as no errors and it does not have fatal error.



```
# UVM_INFO AHB_SB.sv(31) @ 1200: uvm_test_top.ENV.sb [SB] TRANSACTIONS FROM MON2
# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1268) @ 1250: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
#
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM_INFO :   96
# UVM_WARNING :    0
# UVM_ERROR :    0
# UVM_FATAL :    0
# ** Report counts by id
# [DRV]     20
# [MON2]     12
# [Questa UVM]     2
# [RNTST]     1
# [SB]     26
# [SB::DATA MATCHED]     12
# [SEQ]     10
# [TEST_DONE]     1
# [mon1]     12
# ** Note: $finish    : C:/questasim_10.4e/win32/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
```

Fig.9 UVM report summary

VI. CONCLUSION

In this article, we explained the different versions of AMBA protocols, their nature of operation and their contribution to microcontrollers, and we have designed AMBA AHB which supports single master and three slaves. As we know complexity of VLSI chips and their logic is increasing very rapidly we need a fast reliable and efficient verification of designs. So we have verified the design using system Verilog and Universal verification methodology. The Tool used is Questa sim is an EDA tool used to simulate and verify the design. The UVM report summary also ensure that functional Correctness of the design.

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