Design and Synthesis of 2-bit Asynchronous and 2-bit Synchronous Counter with Conventional and Reversible Logic

[1]Ms.T. Bhanu Sandhya
M.Tech Scholar, Department of ECE,
Sree Vidyanikethan Engineering College,
Tirupati – 517102, India

[2]Mr. C. Venkata Sudhakar
Assistant Professor, Department of ECE,
Sree Vidyanikethan Engineering College,
Tirupati – 517102, India

[3]Dr. G. Ganesh Kumar
Associate Professor, Department of ECE,
Sreenidhi Institute of Science and
Technology, Hyderabad -501301, India

***Abstract* – The Researchers are interested in reversible computing because of its low power consumption and low heat dissipation. The Reversible logic circuits don't drop information plus input vector also recovered from the output vector. Reversible logic has applications in various fields they are Low Power CMOS Design, Nanotechnology, Optical computing and cryptography. In this term article, sequential circuits such as JK Flipflop, T flipflop, Asynchronous counter and Synchronous counter are designed using reversible logic gates which gives less delay, low power consumption and less number of gates when compared to sequential circuits designed with conventional logic gates. The comparison between conventional and Reversible Asynchronous and Synchronous counter in conditions of power, delay and number of gates is given within this paper. The codes are modelled in Verilog HDL and simulated for XC7Z020-3CLG484 FPGA in Xilinx ISE 14.7 Tool.**

Keywords:- Reversible logic gates, Flipflops, counters, Delay and Power dissipation.

I. INTRODUCTION

Power indulgence is the main problem in today's technology. The cause of power dissipation is loss of information and this firstly predicted by R. Landaure in 1960.

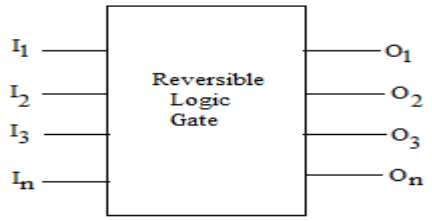


Fig. 1. Block Diagram of Reversible logic gates [2].

Landauer has shows that heat generated for the period of computation isn't due to the processing of bits, however its due to the bits that were erased all over the procedure. According to his principal k*T*ln2 joules energy dissipate into environment when loss the one bit of information. Where Boltzmann's constant (k) and absolute temperature (T). Generated heat can be problematic for larger circuits. One more researcher C. H. Bennett [2] in 1973 proposed that number of bits lost is directly related to energy dissipation. KTln2 [2] dissipation of energy wouldn't occur, In the event that a working out is passed away in a reversible way.

The number of bits deleted for the period of computation has a direct relationship with the amount of energy dissipated in a device [3]. Esig=1/2CV2 is the energy of voltage-coded logic signals, and this energy is degenerate whenever switching occurs in conventional (irreversible) logic implemented in CMOS technology[3].

The logical reversibility means the number of input and output lines should be equal. In the reversible logic gates," input can also be recover as of the output". The second law of thermodynamics guarantees that the system will not produce any heat if it meets these two conditions. In the reversible logic have two limitations. They are

1. Fan-out is not allowed [2].
2. Feedback is not allowed [2].

Reversible logic are used in various fields which include quantum computing, digital signal, image processing, optical computing, Low power VLSI etc [2].

Inputs		Output
A	B	C = A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table For Irreversible EXOR Logic

Inputs		Outputs	
A	B	P=A	Q = A⊕B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Truth Table For Reversible EXOR Logic (Feynman Gate)

Fig.2. Difference between Irreversible and Reversible logic gates.

II. LITERATURE REVIEW

In 2020, V. Ganesh Raja has proposed the Design Approach of specific Sequential circuits using Reversible gates [1]. They designed a D Flipflop, JK Flipflop, T Flipflop, and linear feedback shift register and priority encoder using reversible logic gates. They intend to decrease delay, power consumption and garbage outputs. They proposed priority encoder, it shows great improvement than other designs. In upcoming, they want to realize reversible 4 and 8 bit LFSR and PROMs.

In 2018, C. Venkata sudhakar has designed and Synthesis of Combinational Circuits using Reversible logic [2]. They designed combinational circuits like decoders, comparator, full adder and multiplexer with reversible logic gates are fredkin gate, CNOT, Peres gate and R-I gate [2]. They designed 3 to 8 decoder using 2 to

4 decoder followed by 4 R-I gates [2] and also designed the 4 to 16 decoder using 3 to 8 decoder followed by 8 R-I gates with quantum cost 56.

In 2018, Harish Naik K. P has proposed design of Asynchronous Counter using Reversible logic gates [4]. They designed Reversible D-latch and four bit asynchronous counter using reversible T Flipflop. Two SG [4] gates and one Feynman gate[2] are used for design of T Flip-flop with less garbage outputs and number of gates as 3 and 3. 4-bit asynchronous counter[4] are proposed with reversible T Flipflop contains Reversible Gates are 15, Constant Inputs are 11 and produce Garbage Outputs is 12.

III. DESIGN OF FLIPFLOPS AND COUNTERS USING CONVENTIONAL LOGIC GATES

A Flip flops are the circuits and it is used for data storage.

A.JK Flipflop [1]

The JK Flipflop is the resourceful of basics Flipflop. The JK Flipflop is basically gated SR Flipflop. The JK Flipflop is differ compare to the SR-Flipflop. The JK Flip-flop prevent the unacceptable condition of SR flip flop (S = 1 and R = 1). The JK Flipflop has one clock input, 2 control inputs (J & K) and 2 outputs (Q & Qbar).

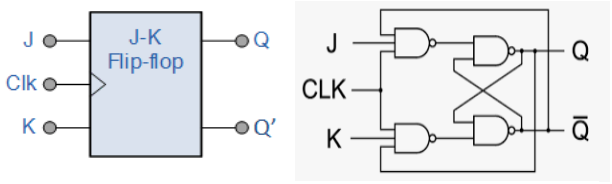


Fig. 3. Symbol and Circuit diagram of Conventional JK flipflop.

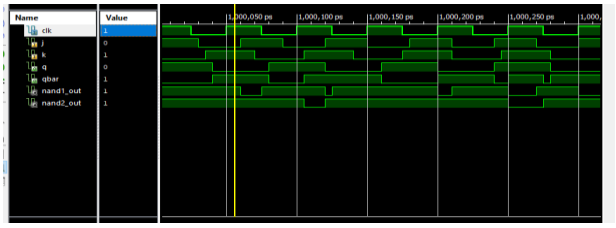


Fig. 4. Simulated Output of Conventional JK Flipflop.

B. T Flipflop

T Flipflop has single input that is constructed by connecting the input of JK Flipflop. At each timer edge, the T Flipflop output is changes. The output of T Flipflop is the half frequency of T input.

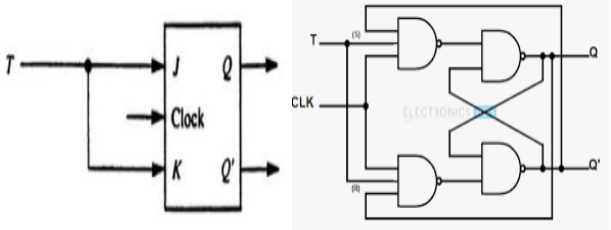


Fig. 5. Symbol and Circuit diagram of Conventional T Flip flop.

The T Flipflop used in constructing of binary counters and binary addition devices. It is able to obtain from the JK Flipflop when J and K together are high on the input.

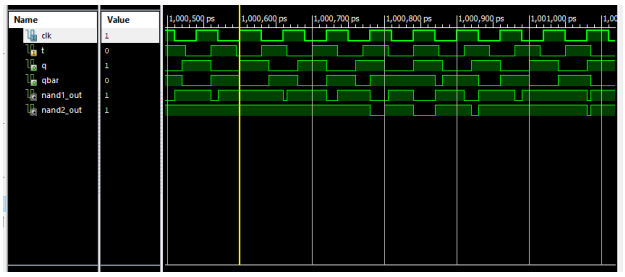


Fig. 6. Simulated Output of Conventional T flip flop.

C. Two-bit Asynchronous Counter

In the Asynchronous counter [3], only one Flipflop is connected to outside Clock. All succeeding Flipflops [1] are attached to previous Flipflop output. The vary of state of a given Flipflop is dependent on state of other flip-flops.

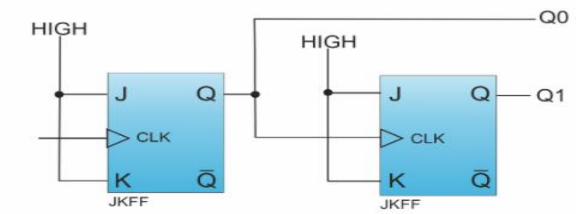


Fig. 7. Two-bit Conventional Asynchronous Counter.

Another name for asynchronous counter is Ripple counter. Synchronous counter is faster than the asynchronous counter. Because Asynchronous counter has more delay of the pulse from one Flip flop to another Flip flop.

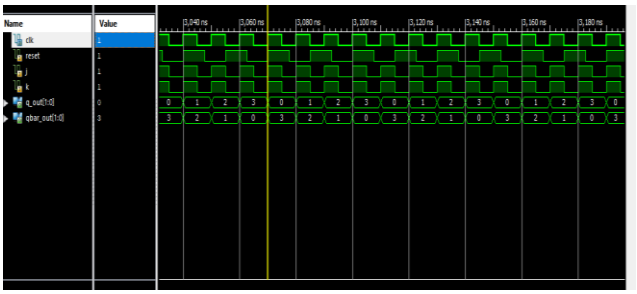


Fig. 8. Simulated output of Conventional Two-bit Asynchronous Counter.

D. Two-bit Synchronous Counter

In synchronous counter [3], all the Flipflop are trigger with similar Clock. Synchronous counters is faster compare to the asynchronous counters. In synchronous counter decoding errors are not present. The design of synchronous counter is complex because number of states increases.

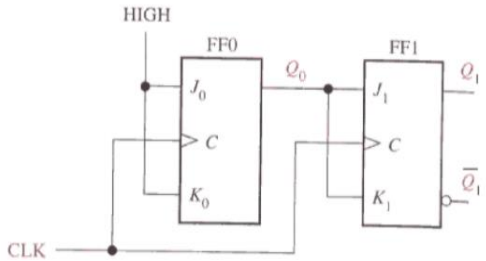


Fig. 9. Conventional Two-bit Synchronous Counter.

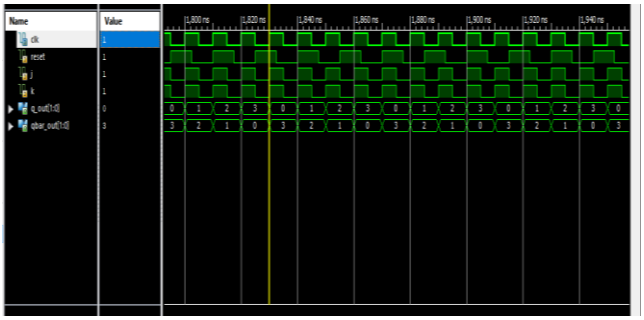


Fig. 10. Simulated output of Conventional Two-bit Synchronous Counter.

IV. REVERSIBLE LOGIC GATES

A memory-less logic element that realizes an injective logic feature is known as a reversible logic gate. There are an the same number of inputs and outputs within reversible logic. Between the vectors of input and output, there be a one-to-one mapping. In the proposed modules, four reversible logic gates are used they are MG-1 gate, MG-2 gate, Peres gate and Feynman gate. MG means 'Mamun Gate'.

A. MG-1 Gate

The MG-1 logic gate is a four-by-four reversible logic gate. MG-1 gate has four inputs and outputs. In MG-1 gate, (A, B, C, D) are the inputs and outputs be a P=A XOR D, Q = (A' B) XOR (A C'), R=A'C XOR AB and S = (A'C) XOR AB XOR D. MG-1 gate as shown below.

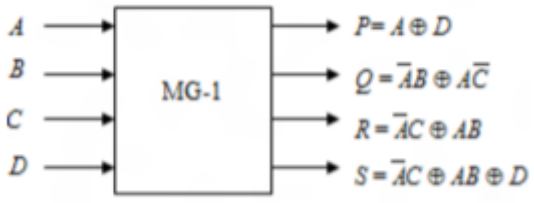


Fig. 11. MG-1 Gate.

TABLE I.
MG-1 GATE THRUTH TABLE

A	B	C	D	$P = A \oplus D$	$Q = \overline{A}B \oplus A\overline{C}$	$R = \overline{A}C \oplus AB$	$S = \overline{A}C \oplus AB \oplus D$
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	1	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	1	1	1	0
1	0	0	0	1	1	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	0	0	0
1	0	1	1	0	0	0	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	0
1	1	1	0	1	0	1	1
1	1	1	1	0	0	1	0

B. MG-2 Gate

A 4*4 Reversible logic gate is the MG-2 gate. It has four inputs and four outputs. In MG-*2* gate, (A, B, C, D) are the inputs and outputs are P=A, Q=(A'B) ^ (AC'), R = (A'C) XOR (AB) and S = A ^ D [5]. MG-2 Gate as shown below.

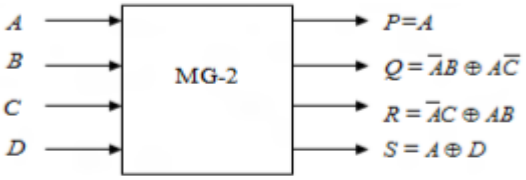


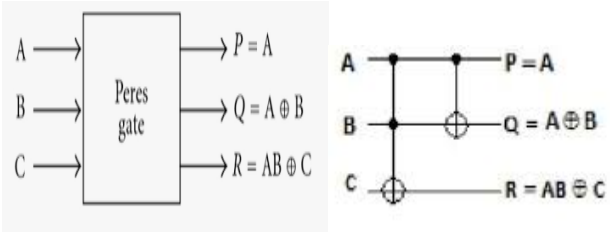
Fig. 12. MG-2 Gate.

TABLE II.
MG-2 GATE THRUTH TABLE

A	B	C	D	$P = A$	$Q = \overline{A}B \oplus A\overline{C}$	$R = \overline{A}C \oplus AB$	$S = A \oplus D$
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

C. Peres Gate

A Three-by-Three Reversible logic gate is the Peres gate. Three inputs and outputs in Peres gate. The inputs are (A, B, C) and outputs are (P, Q, R) be as follow: P=A; Q=A^B; R=(AB)^C. Peres gate as shown below.



(a)Block Diagram (b) Symbol

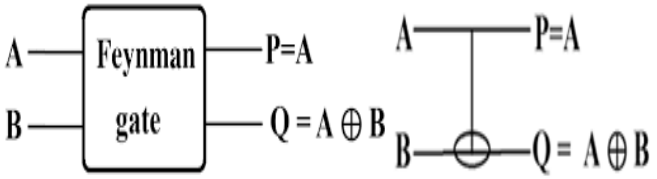
Fig. 13. Peres Gate.

TABLE III.
PERES GATE THRUTH TABLE

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

D. Feynman Gate

Feynman gate is 2*2 Reversible logic gate. Feynman gate has two inputs and two outputs. The inputs are A and B and outputs are P = A and Q = A^B.



(a)Block Diagram (b) Symbol

Fig. 14. Feynman Gate.

TABLE IV.
FEYNMAN GATE THRUTH TABLE

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

V. DESIGN OF FLIPFLOPS AND COUNTERS USING REVERSIBLE LOGIC GATES

A.JK Flipflop

Two Reversible gates are used to create JK Flipflop. They are one is MG-1 gate and another one is MG-2 gate. The typical equation for JK Flipflop is Q = (JQ') + (K'Q). Clock, J and K are inputs and Q and Qbar are outputs.

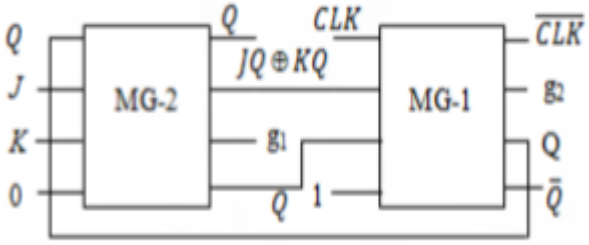


Fig. 15. Reversible JK Flipflop.

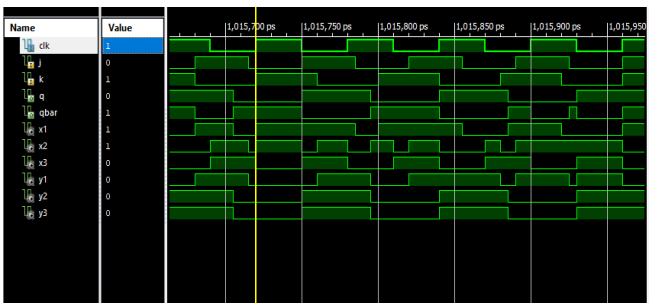


Fig. 16. Simulated output of Reversible JK Flipflop.

B. T Flipflop

Three Reversible gates are utilize to construct the T Flipflop. They are one Peres gate and two Feynman gates. The typical equation for T flipflop is Q =TQ' + T'Q. Clock and T are the inputs. Q and Qbar are the outputs.

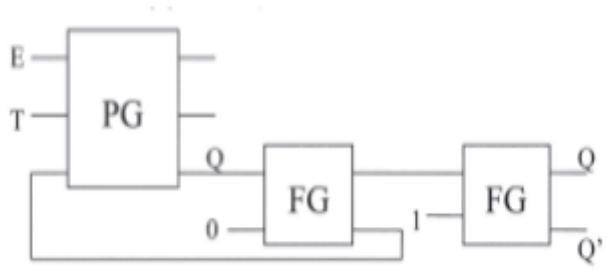


Fig. 17. Reversible T Flip flop.

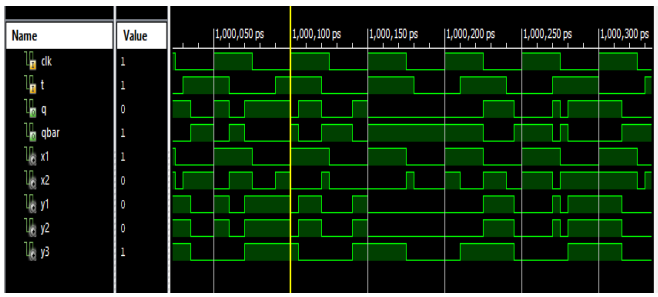


Fig. 18.Simulated output of Reversible T Flipflop.

C. Two-bit Asynchronous Counter

A Two-bit Asynchronous counter designed by using two reversible JK Flip flop and one Feynman gate. The clock input is given to Feynman gate and Feynman gate output is connected to Reversible JK Flip flop as clock input.

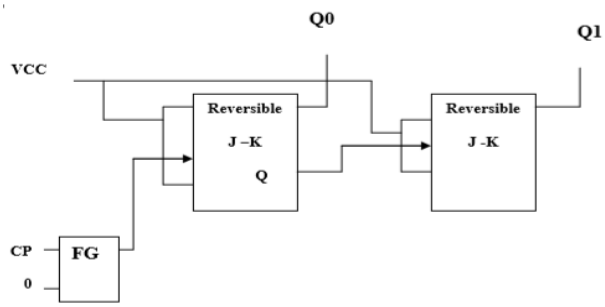


Fig. 19.Reversible Two-bit Asynchronous Counter.

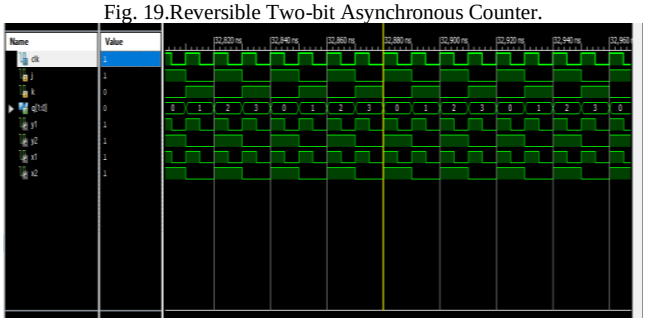


Fig. 20. Simulated output of Reversible Two-bit Asynchronous Counter.

D. Two-bit Synchronous Counter

A Two-bit synchronous counter designed by using two reversible JK Flip flop and two Feynman gate. The clock input is given to Feynman gate; Feynman gate output is connected to another Feynman gate as input and also joined to reversible JK flipflop as clock input.

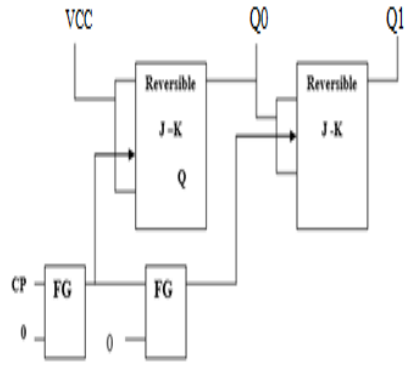


Fig. 21. Reversible Two-bit Synchronous Counter.

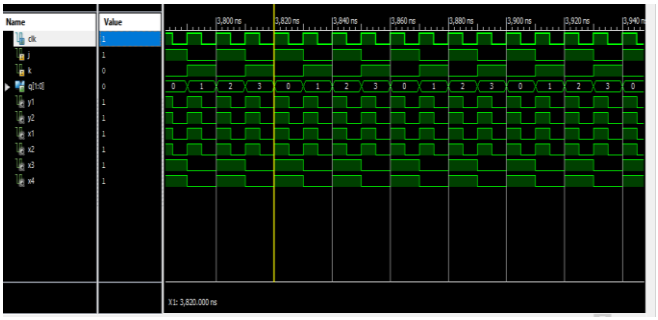


Fig. 22. Simulated output of Reversible Two-bit Synchronous Counter.

VI. COMPARATIVE STUDY

The proposed research compares the Design of Sequential circuits with reversible logic gates and design of sequential circuits with irreversible logic gates in conditions of delay, power and number of gates.

TABLE V.
COMPARISION OF VARIOUS PARAMETERS FOR FLIP-FLOP AND COUNTER

Parameters	Conventional JK flip-flop	Reversible JK flip-flop	Conventional T flip-flop	Reversible T flip-flop	Conventional 2-bit Asynchronous counter	Reversible 2-bit Asynchronous counter	Conventional 2-bit Synchronous counter	Reversible 2-bit Synchronous counter
Total power	114mW	114mW	114mW	113mW	114mW	113mW	114mW	114mW
Delay	1.433ns	1.093ns	1.012ns	1.008ns	1.691ns	1.342ns	1.685ns	1.000ns
Number of gates	4	2	4	3	8	5	8	6
Total signal power	0.02mW	0.02mW	0.02mW	0.01mW	0.02mW	0.01mW	0.09mW	0.01mW
Total data power	0.02mW	0.02mW	0.02mW	0.01mW	0.01mW	0.01mW	0.09mW	0.01mW

VII. CONCLUSION

Reversible logic gates are used to implement sequential circuits in this paper. Sequential circuits are flip-flops and counters. The Flip-flops are used in several circuits like RAM, Logic blocks of FPGA. Here, Four modules are designed, they are JK Flipflop, T Flip flop and Counters. The JK Flipflop, T Flipflop, two-bit Asynchronous and two-bit Synchronous counter are designed with reversible logic gates which gives low power consumption, less delay and less number of gates when compared to sequential circuits designed with conventional logic gates. Comparison between reversible JK Flipflop, T Flipflop, two-bit Asynchronous and two-bit synchronous counter and conventional JK flipflop, T flip flop, 2-bit asynchronous and 2-bit synchronous counter in terms of power, delay and number of gates is given in above table.

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