Design and Simulation of RF Receiver for LTE

Pooja Arali
M.Tech Student
R V College of Engineering
Bengaluru, India

Madhusudhan Rao Kothari
Assistant Manager, LTE
Tata Power SED
Bengaluru, India

Dr. K Sreelakshmi
Professor, Dept. of TCE
R V College of Engineering
Bengaluru, India

***Abstract*: RF front-end architecture plays a very vital role in a transceiver system. The design should be such that it provides a better noise figure and gain and good rejection to image frequencies and undesired noise. The purpose of this paper is to design receiver architecture for a long term evolution (LTE) base station for band 28 having an uplink of frequency of 703MHz to 748MHz. The conceptualised design of the receiver chain is to meet the various standards of 3GPP such as Receiver sensitivity, Noise figure and Gain. Choosing of proper components for meeting the requirements of both cost effective as well as performance enhancement is necessary. The schematic design of the receiver chain is drawn and is simulated using software tool NI-AWR for VSS simulations. The obtained simulated values provide us with the noise figure, gain, P1 dB, IIP3 and signal power.**

***Key words*: *LTE, Gain, Noise Figure, MSD, P1DB*.**

I. INTRODUCTION

The new trend of high speed data and voice has become very popular and useful. The demand of high speed data rate, better spectral efficiency, high mobility and high quality of service (QOS) has lead to evolution of new era of LTE. The LTE standard was developed by 3rd generation partnership project (3GPP) in release 8. The LTE has uplink peak rates up to 75MBPS and downlink is up to 300MBPS. It has a scalable bandwidth from 1.4MHz to 20MHz. The various frequencies of LTE are divided into bands divided into only TDD and both TDD and FDD [1].
Here in this paper the design of receiver architecture is explained. The receiver operates in a LTE band 28 whose frequency ranges from 703MHz to 748MHz. Band 28 is used for military applications.
The paper is organized as follows; section 2 presents the receiver design, explaining block diagram and its description, section3 presents system design parameters section 4 simulation results of receiver and section 5 is conclusion.

II. RECEIVER DESIGN

The receiver is designed such that it provides optimum results. The circuit level diagram is drawn and then the simulation of the receiver is done in a simulation tool called NI-AWR explaining about the noise figure (NF), gain, IIP3, and other 3GPP specifications.

A. BLOCK DIAGRAM

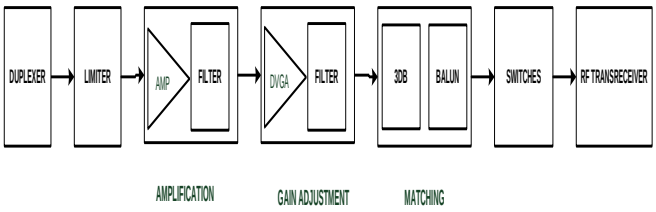

Figure1. Generic Receiver Diagram

The fig 1 depicts the generic receiver diagram having the most important 3 stages, amplification, gain adjustment, matching. Due to the dynamic range, the signals are differentiated between weak signal and strong signal that is near subscriber and far subscriber. The design is made such that it provides a good cascaded noise figure and cascaded gain and good rejection to the noise. The three stages, described above are main steps to be carried to achieve the desired output; hence the components should be chosen such that it optimizes the result.

B. BLOCK DIAGRAM DESCREPTION

To begin with, to share the common antenna for receiver and transmitter and isolating each other, the duplexer is used. This device allows bi directional communication on a signal path. The duplexer is chosen such that it gives good isolation and less insertion loss.
The limiter is chosen to reduce the signal level to an amplifier level that will not overdrive the receiver LNA. The criterion to choose limiter is low insertion loss.
Then this signal is amplified in the amplification stage. The amplification stage is designed for having a combination of LNA and a band pass filter. The LNA is required for the reducing the noise through its gain, boost up the power signal. The LNA in the design is chosen such that it has high gain, low noise figure and high compression point i.e., P1dB. The bandpass filter helps in cancelling the out of band frequencies. The antenna may pick up frequencies of unwanted band hence to get a clear signal, a filter is necessary. The band pass filter is chosen such that it has good input output matching and provides low insertion loss at the frequency of interest.
Once the amplification stage is done, the gain adjustment is done using DVGA. Here in this the gain is adjusted to such a level that the noise figure of overall chain is less. And again it is accompanied with the filter.
Then matching input output is done with the help of 3dB

pad. 3dB pad is a pure resistive network which helps in input output matching provides isolation and attenuates the signal.

After these three important stages, we go for transreceiver. Transreceiver is a RF Module which processes both transmitter and receiver signals and communicates with another device wirelessly. These compromises of PCBs of various RF devices, TX circuit, RX circuit, antenna and serial interface for communication to the main processor. This communicates to FPGA, microcontroller and other devices in digital domain.

III. SYSTEM DESIGN PARAMETERS

The system is described by its various important design parameters which are Gain, Noise figure, IIP3, P1dB. These are calculated for the cascaded link[4].

Gain: it is the parameter which amplifies the power signal. If the powers of signals are defined in linear units that is(W or mW) or decibels (dBW or dBm)

then the gain is defined as follows:

G = Pout, mW/Pin, mW (1)

Or

G (dB) = Pout, dBm - Pin, dBm (2)

Noise figure: this an important parameter of receiver describing the amount of signal added to the system.

NF = SNR in, dB – SNR out, dB (3)

Where SNR is signals to noise ratio, we can say that noise figure is simply the comparison of the SNR at the input and the output of the circuit.

P1dB: The 1-dB decrease may be specified as the input level that produces it or the output power where the 1-dB drop occurs.

IIP3: for 2nd and 3rd harmonics, usually fall out of band and can be easily filtered. But sometimes, when two frequencies collide, their sum and difference occur within the band, these are hard to filter and they occur as interference and degrade the linearity of the devices. We always have to maintain the IIP3 to a high level. The IP3 point is typically about 10 dB above the 1-dB compression point.

Once these are described, it is important to calculate the Minimum signal that can be detectable.

By the standards of UMTS, we set the LTE receiver's Noise figure as 4dB. The measure of sensitivity with SNR set at 4dB for bandwidth of 10MHz is which is according to 3GPP standards.

The noise floor can be defined as the measure of the signal created from the sum of all the noise sources and unwanted signals within a system. This noise floor is the value which decides how much greater the signal should be then noise floor to get detected. To calculate the noise floor, we use formula [6],

Noise floor= -174dBm/Hz + NF + 10log (BW) (4)

Noise floor = -174dBm/Hz + 4 + 10log (10^7) (5)

Noise floor= -100dBm (6)

Hence the -100dBm, calculated noise floor, tells that any signal to get detected must be more then this value, that is now defining Minimum Detectable Signal (MSD).

“A minimum detectable signal is a signal at the input of a system whose power produces a signal-to-noise ratio of m at the output”.

The difference between the power signal and noise signal required to know the MSD is called Signal to Noise Ratio (SNR).Now to calculate the MSD, we see that our signal must be greater than the noise by SNR times. Hence the calculated MSD is,

$P_{in,\ min}$ = -174dBm/Hz + NF + 10log (BW) +SNR (7)

$P_{in,\ min}$ = Noise floor +SNR (8)

$P_{in,\ min}$ = -104dBm (9)

Therefore -104dBm is the minimum detectable signal required.

IV. SIMULATIONS AND RESULTS

The simulation is done in a tool NI-AWR. The simulation results show the noise figure of the cascaded chain and how it varies at every component.

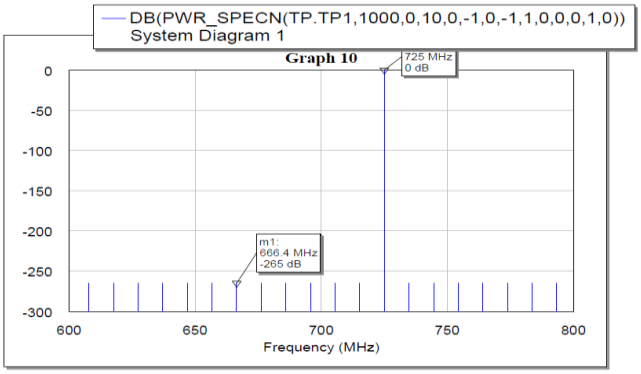

Figure2. Input power spectrum

The fig 2 shows the input power spectrum centered at 725MHz. As seen, at center frequency, the signal get 0dB attenuation and all the signal power of -104dBm is passed throughout the link.

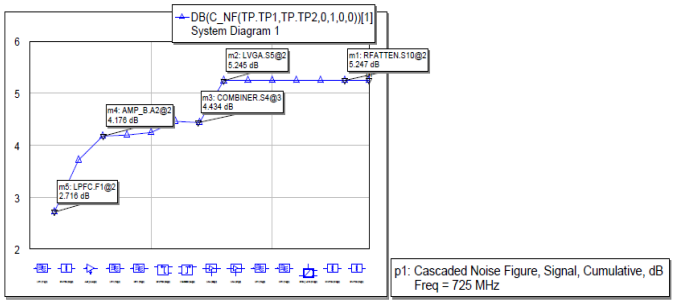

Figure3. Noise figure

Noise figure is explained by the fig 3. The cascaded NF is 5.247 dB.

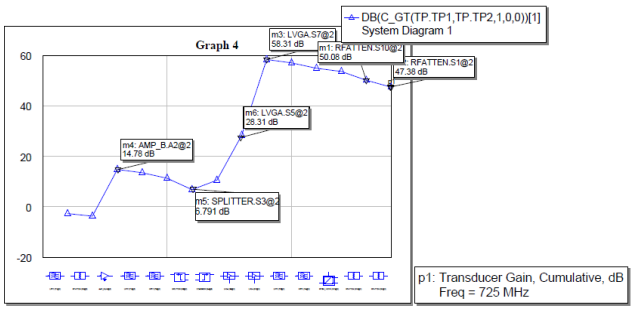

Figure4. Cascaded gain

The cascaded gain of the link is shown in the figure. The system gives 47.38dB

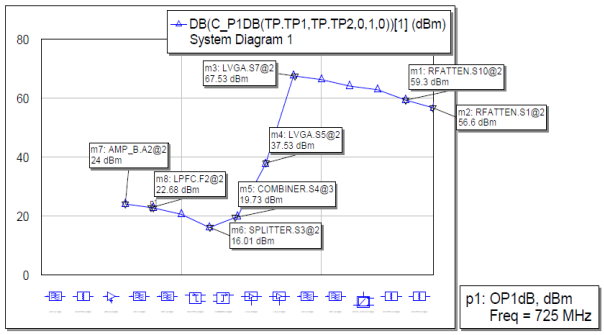

Figure5. Cascaded P1dB

The above figure show the cascaded P1 dB at 56.6dBm

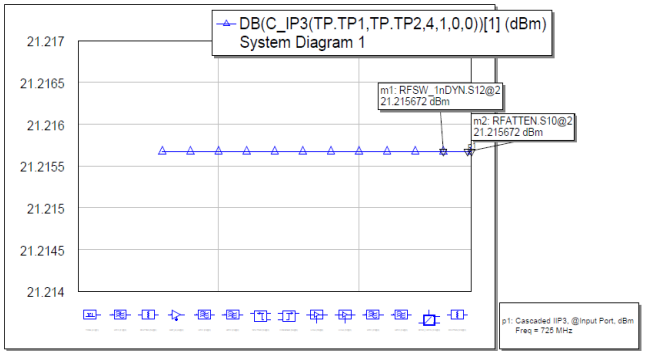

Figure6. Cascaded input IP2

As seen from the figure the cascaded IP3 measured at the input port is 21.2156dB

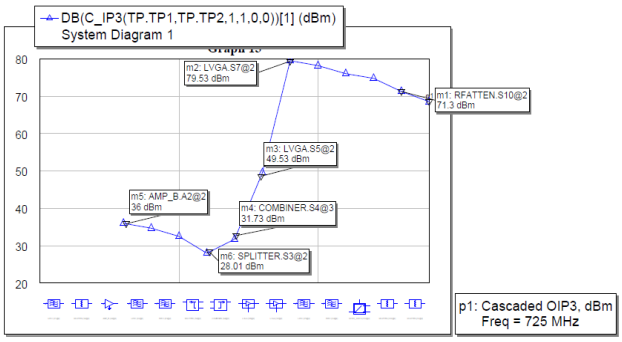

Figure7. Cascaded output IP2

As seen from the figure the cascaded IP3 measured at the output port is 71.3dB

V. CONCLUSION

In this paper the receiver mentioned for the LTE section describes the approach to design the receiver link and explains the important receiver parameters at the system level design. With the simulation in the AWR tool, we obtain a good gain of 47.38Db and noise figure of 5.427dB is achieved with the OIP3 71.3dB of and p1dB of 56.6dbm.

VI. FUTURE SCOPE

The receiver design can be further expanded for different frequencies and can also be used for not only LTE also communication over TETRA. With further different choice of components can provide much better output and this can be modified for further research.

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REFERENCES

1. 3GPP TS 36.101, "EUTRA User Equipment Radio Transmission and Reception", September 2008, vol. 8.3.0.
2. Abeta,S., “Toward LTE commercial launch and future plan for LTE enhancements (LTE-Advanced),” Communication Systems (ICCS), 2010 IEEE International Conference, pp.146-150, 17-19Nov.2010.
3. Sadek, shawkey, Zerkey, “constructing complete radio frequency receiver for LTE TDD Transreceiver” Communications on Applied Electronics (CAE) – ISSN : 2394-4714, Volume 3– No.2, October 2015.
4. D.M Pozar, “Microwave Engineering,” 2nded. New York, Wiley,1998,pp.367-368.
5. Dae-Soon Cho, IL-Kyu Kim, Hyuncheol Park, “Performance of Implemented 4x4 MIMO Receiver for 3G LTE Advanced System”, IEEE, 2015
6. P. Vizmuller. RF Design Guide: Systems, Circuits and Equations. Artech House,1995.