Design and Simulation of Multiplexer using Josephson Junction using OrCAD Capture

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***Abstract*— The work presented here is a summary of the result obtained when Multiplexer was simulated using simulator: OrCAD Capture 16.5. The Multiplexer is made using the universal logic gates formed by Josephson junction. This allows us to focus our attention on solely the output characteristics and related results derived from the Multiplexer. We begin by describing formation of universal gates and more. We conclude by stating the output characteristics are in match with the multiplexer.**

Keywords—Mux, OrCAD, P Spice, Simulation, NOR Gate, Josephson Junction.

I. INTRODUCTION

In our advent into the world of circuit simulation, we have chosen to taken up a subject, which is in the center of many important developments in the modern world. Electronics has seen its boundaries extended with the addition of simulation capabilities. It is our intent to contribute, in our own small way, to this growing pool of knowledge.

Using a simulation technique allows one to analyze electronic circuit's large scale – subject to available computing power. There are a huge number of simulation tools available. In this case study, we focus on OrCAD.

The paper goes on to describe formation of universal NOR gate and Multiplexer obtain using the former made gates. Section 2 describes OrCAD in its various features and its relevance with the electronic simulation space. Section 3 lists out the simulation setup used, and describe the different hardware and software parameters of the simulation workbench. Section 4 and 5 analyze the results obtained, while drawing some conclusions. Finally, the paper end with a look at future steps in the direction and list of works referenced which were helpful in guiding us in our work.

II. OrCAD

A. Introduction

OrCAD® Capture is one of the most widely used schematic design solutions for the creation and documentation of electrical circuits. Fast, easy, and intuitive circuit capture, along with highly integrated flows supporting the engineering process, make OrCAD Capture one of the most popular design environments for today's product creation.

Design of today's electronic products involves more than simply capturing connectivity, building parts, netlisting to PCB and hoping for the best. Component information, variant design and circuit reuse, hierarchal schematics, circuit and signal integrity simulation, and integration into corporate data systems all play a significant role in reducing your development time and project cost, improving product reliability and manufacturability, and helping to achieve first-pass success.

Whether designing a new analog circuit, revising digital schematics for an existing PCB, or implementing hierarchical block design, the OrCAD Capture solution and integrated flows provide everything needed for circuit design, analog/mixed-signal simulation, component optimization and selection, and signal integrity planning.

OrCAD Capture provides core schematic editing capabilities, and much more. It is highly integrated with OrCAD PCB Editor for physical PCB design, OrCAD PSpice® for analog/ mixed-signal circuit simulation, OrCAD PCB SI for signal integrity analysis and planning, and OrCAD CIS (Component Information System) for component optimization, selection, and variant design, greatly extending the schematic design process

B. Schematic Editor

The OrCAD Capture schematic editor builds on the legacy of OrCAD providing fast and easy schematic editing for the simplest to the most complex designs. It combines an intuitive interface with all the features and functionality you need to speed through design tasks and circuit creation.

C. Productivity and ease of Use

The schematic editor provides numerous features and functionality that enhance usability and speed for accomplishing design tasks and publishing design data. For example, the autowire capability automates the often tedious and time-consuming task of wiring signal pins by quickly and automatically adding connection wires for you. Context-sensitive menus, OLE support, custom colorization of wires, nets, and parts, and a tabbed and dockable interface all provide a better user experience.

For larger, more complex designs, OrCAD Capture supports circuit reuse and hierarchical circuit blocks. Such designs are easy to traverse with navigation aids and OrCAD Capture ensures that all connections are maintained accurately throughout the design.

D. Design reuse

The reuse of existing logical (and physical) circuits that you have already tested and proven is one of the best ways to reduce your design time and maximize quality. Having already been placed, routed, and validated on a previous design, the effort you put into the original design is leveraged through OrCAD Capture's design reuse capabilities. Typical reuse examples include power supply modules, RF circuit designs, multi-channel circuits (I/O, drivers, etc.), and memory.

E. PSpice Simulation

The OrCADPSpice analog/mixed-signal circuit simulator solution is seamlessly integrated within OrCAD Capture to boost productivity and allow you to use the same schematic for both simulation exploration and PCB layout, reducing rework and errors. Even if you're not creating a circuit for use in the PCB flow, the integration allows for easy setup, model placement, circuit creation, and simulation, as well as cross-probing of simulation results.

F. PSpice Simulation

Tightly integrated to provide a bi-directional schematic entry and signal integrity flow, OrCAD Capture and the OrCAD PCB SI product allow you to perform circuit topology exploration, constraint development, and signal integrity analysis from the schematic during design entry. The associated Electrical Constraint set (Electrical CSet) as well as the complete topology file is embedded in the schematic database.

III. SIMULATION SETUP

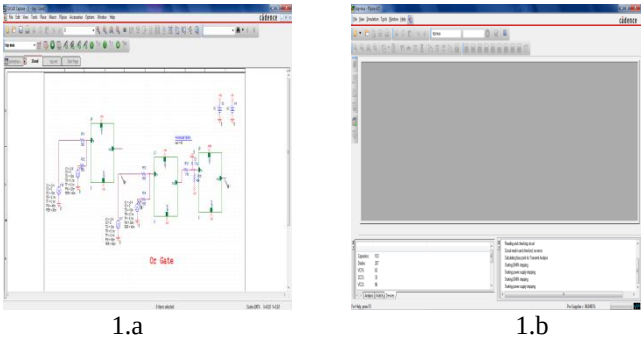
We choose to execute the simulation of the circuits so as to understand and study the various effects of the circuits.

TABLE I
THE HARDWARE/SOFTWARE SETUP

Operating System	Microsoft Windows 7 Home Premium
Processor	Intel Core i3 – 2.40 GHz – 4 Processes
Memory	4GB
Simulated using	1. OrCAD Capture 16.5 2. PSpice AD

Over the course of the many simulations that led to the final ones presented here, we understood that OrCAD Capture is a highly resource intensive simulation package.
Once we gained enough confidence over our circuit model and general proficiency over logic gates implementation by using Josephson Junctions, we moved further to simulate the Multiplexer formed by the logic circuits made earlier. The run configuration we designed allowed us to use the multiple Josephson Junctions available on our design.

We must admit that our software configuration with respect to the real world conditions are fairly limiting. We intended to simulate the Multiplexers using logic gates.
Figure 1 denotes the screenshot while simulating the basic logic gates design. Also for this purposes we have to configure the simulation profiles of the circuit.



1.a 1.b

Figure 1.a – 1.b: OR Logic Gate made using Josephson Junctions; (B) Simulation of (A) in PSpice AD

Figures 1.a & 1.b are illustrations using a computer screenshot taken during the simulation.
Figure 2 denotes the simulation profiles configurations being used during simulation.

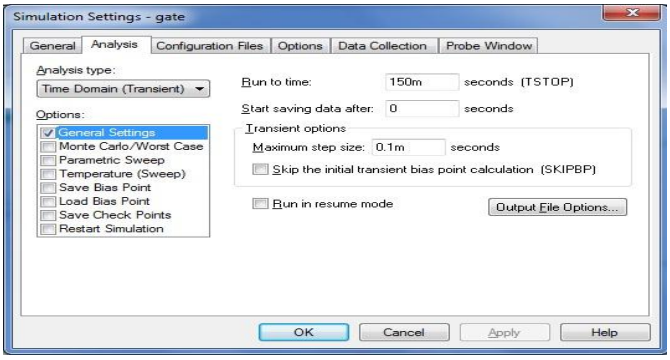


Figure 2:Simulation Profile Settings

IV. RESULTS

A. Design of NOR Gate

Figure 3 shows the universal logic gate NOR gate formed using the Josephson junction. The input a receives the two inputs in form of pulses and the output out can be seen as in figure.

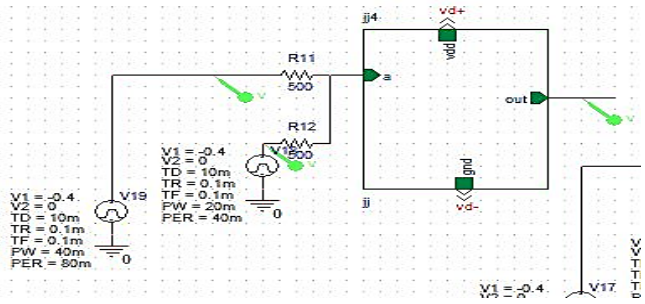


Figure 3: The Design of NOR gate.

The behavior of circuit can be inferred as NOR gate as the output waveform satisfies the logic of NOR gate. The Table II shows the values of NOR gate and its equivalent Boolean logic.

The Boolean logic for NOR gate is

$$\text{Out} = \overline{(A + B)}$$

It can be observed from the table that the output is HIGH only if both the inputs are LOW and output is LOW when either of the input is HIGH.

TABLE II
TRUTH TABLE OF NOR GATE

Inputs		Output
A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

B. Simulation Output of NOR Gate

The below figure 4 shows the simulation outputs for the NOR gate formed using the Josephson junctions.

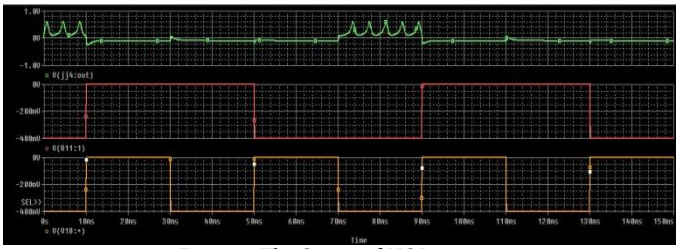


Figure 4: The Output of NOR gate.

C. Design of MUX

Figure 5 shows the Mux formed using the Josephson Junction.

The input a receives the two inputs in form of pulses and the output out can be seen as in figure 5.

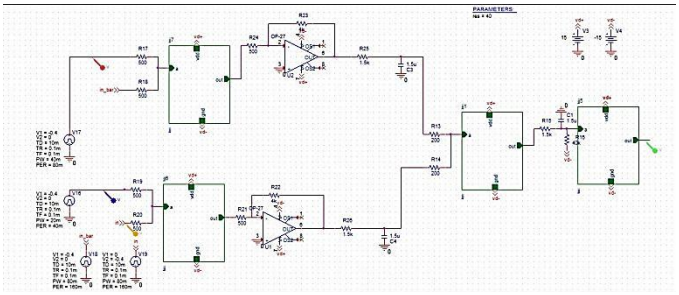


Figure 5: The Design of 2:1 Mux.

The behavior of circuit can be inferred as Multiplexer as the output waveform satisfies the logic of multiplexer. The Table III shows the values of multiplexer and its equivalent Boolean logic is mentioned below.

The Boolean logic for multiplexer is$Out = S.A2 + \overline{S}. A1$

It can be observed from the table that the output corresponds to A1 only if S is LOW and when S is High output corresponds to A2.

TABLE III
TRUTH TABLE OF 2:1 MUX

Inputs			Output
S	A1	A2	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

D. Simulation Output of 2:1 Mux

The below figure 6 shows the simulation outputs for the MUX formed using the Josephson junctions.

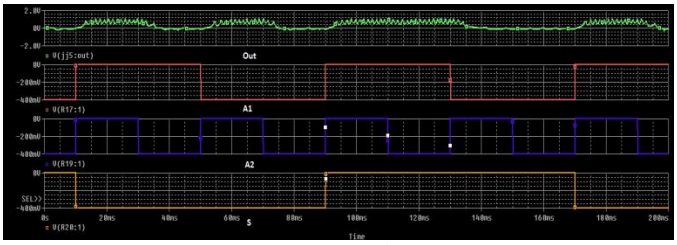


Figure 6: The Output of 2:1 Mux.

That concludes the different parameters we wished to discuss as a part of this paper. We believe that the presented parameters are critical in the evaluation and discussion of any set of digital circuits. We shall now go on to draw out some conclusions on the next section.

V.CONCLUSION

In the previous section, we have made and evaluated the universal NOR gate and 2:1 Mux. Simulation parameters were recorded for them and output graphs were shown.

In conclusion, we believe that Multiplexer has been successfully made as output graph was in accordance to the truth-table.

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