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Design and Simulation of Monolithic 3D Accelerated 8T SRAM using Planar MOSFETs for Low Power and High Reliability

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Abstract: This paper presents the design, implementation, and simulation analysis of an 8-transistor (8T) SRAM cell in 90nm planar CMOS technology, targeting enhanced read stability and low power operation[1]. The proposed 8T architecture incorporates a dedicated read port that decouples the read current path from the internal storage nodes, thereby eliminating the read disturb vulnerability inherent in conventional 6T SRAM designs[2]. Both 6T and 8T SRAM cells were designed and simulated using Cadence Virtuoso with the gpdk090 process design kit at a nominal supply voltage of 1.2V. Transient analysis confirms proper write and read functionality for both topologies, with the 8T cell demonstrating isolated read operation through the dedicated read word line (RWL) and read bit line (RBL). Comparative analysis reveals that the 8T configuration successfully maintains data integrity during read access while operating at comparable power levels. The results validate the 8T SRAM architecture as a robust solution for low-power, high-reliability embedded memory applications.

Keywords: 8T SRAM, 6T SRAM, read disturb, Cadence Virtuoso, 90nm CMOS, gpdk090, low power, read stability.

1. INTRODUCTION

Static Random Access Memory (SRAM) is a critical component in modern System-on-Chip (SoC) designs, occupying a significant portion of the total chip area and contributing substantially to overall power consumption[3]. The conventional 6-transistor (6T) SRAM cell has been the industry standard for decades due to its compact footprint and symmetric structure.

However, as technology scales into the deep sub-micron regime, the 6T cell exhibits a fundamental limitation known as read disturb—a condition where the stored data becomes vulnerable to unintended flipping during read operations[2].

The read disturb phenomenon occurs because the same access transistors used for write operations are also employed during read access. When the word line (WL) is asserted, the internal storage node storing a logical '0' experiences a voltage rise due to the resistive divider formed between the access transistor and the pull-down transistor [5]. This voltage elevation can potentially flip the cell state, particularly at reduced supply voltages and in the presence of process variations.

To address this limitation, the 8-transistor (8T) SRAM topology introduces a dedicated read port comprising two additional NMOS transistors. This read buffer isolates the storage nodes from the read bit line (RBL), ensuring that read current does not disturb the stored data. This paper presents the complete design flow, schematic implementation, and simulation validation of both 6T and 8T SRAM cells using the gpdk090 90nm planar CMOS technology[4].

The primary objectives of this work are:

- To design and implement functional 6T and 8T SRAM schematics in Cadence Virtuoso.
- To develop comprehensive test benches for transient simulation of write and read operations.
- To validate the read stability improvement of the 8T architecture through comparative analysis.
- To establish a performance baseline for future Monolithic 3D integration studies.

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2. CIRCUIT DESIGN AND IMPLEMENTATION

2.1 Technology Selection

Both SRAM cells were implemented using the gpdk090 (Generic Process Design Kit) 90nm planar CMOS technology. This mature technology node offers a well-characterized device model suitable for academic research and provides a reliable baseline for comparative SRAM analysis. The nominal supply voltage (VDD) for this technology is 1.2V[5].

2.2 6T SRAM Cell Design

The conventional 6T SRAM cell consists of two cross-coupled CMOS inverters (M1-M2 and M3-M4) forming a bistable latch, and two NMOS access transistors (M5-M6) shown in Fig.1 that connect the storage nodes to the bit lines (BL and BLB) under control of the word line (WL) is as shown in Table 1 [2].

Table 1: Transistor Sizing (6T Cell)

Transistor	Type	Width (W)	Length (L)	Function
M1, M3	PMOS	120nm	90nm	Pull-Up
M2, M4	NMOS	120nm	90nm	Pull-Down
M5, M6	NMOS	120nm	90nm	Access

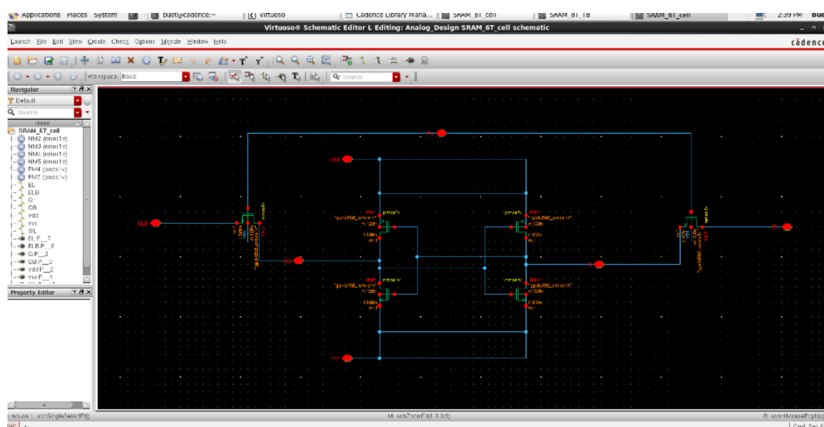

Fig. 1. Cadence Virtuoso schematic of the conventional 6T SRAM cell implemented in gpdk090 90nm CMOS technology.

2.3 8T SRAM Cell Design

The 8T SRAM cell augments the 6T core with a dedicated read port consisting of two additional NMOS transistors (M7 and M8) [5]. Transistor M7 serves as the read access device controlled by the read word line (RWL), while M8 acts as the read pull-down device gated by the storage node Q shown in Fig.2. The original word line is now designated as the write word line (WWL or WL), and the original bit lines (BL and BLB) are used exclusively for write operations as shown in Table 2.

Table 2: Transistor Sizing (8T Cell)

Transistor	Type	Width (W)	Length (L)	Function
M1, M3	PMOS	120nm	90nm	Pull-Up
M2, M4	NMOS	120nm	90nm	Pull-Down
M5, M6	NMOS	120nm	90nm	Write Access
M7	PMOS	120nm	90nm	Read Access (RWL control)
M8	PMOS	120nm	90nm	Read Pull-Down (Q gated)

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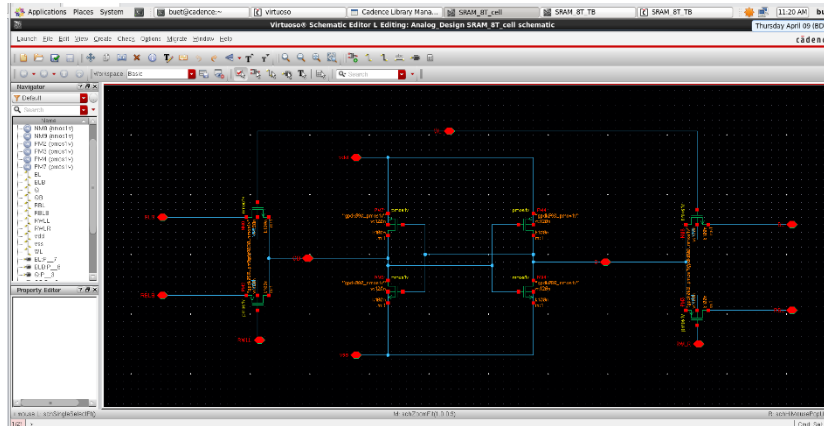

Fig. 2 . Cadence Virtuoso schematic of the proposed 8T SRAM cell featuring a decoupled read port (RWL, RBL) implemented in gpdk090 90nm CMOS technology.

3. SIMULATION SETUP AND METHODOLOGY

3.1 Simulation Environment

All simulations were performed using the Cadence Virtuoso design environment with Spectre as the circuit simulator. The following tools and configurations were employed is as shown in Table 3.

Table 3: Components & Specifications

Component	Specification
Schematic Entry	Cadence Virtuoso Schematic Editor
Simulator	Spectre
Technology Kit	gpdk090 (90nm Planar CMOS)
Supply Voltage (VDD)	1.2V
Temperature	25°C (Nominal)
Model Corner	NN (Nominal NMOS, Nominal PMOS)

3.2 Test Bench Configuration

Separate test benches were created for the 6T and 8T SRAM cells to verify functionality and capture transient response waveforms is as shown in Fig.3 and Fig.4.

1. **6T SRAM Test Bench :**
   - Instance I0: SRAM_6T_cell symbol
   - Voltage Sources: V1 (VDD = 1.2V), V2 (WL pulse), V3 (BL pulse), V4 (BLB pulse)
   - Load Capacitors: C0 on output nodes
2. **8T SRAM Test Bench :**
   - Instance I0: SRAM_8T_cell symbol
   - Voltage Sources: Multiple vpulse sources for WL, BL, BLB, RWL control
   - Separate excitation for write path (WL, BL, BLB) and read path (RWL, RBL)

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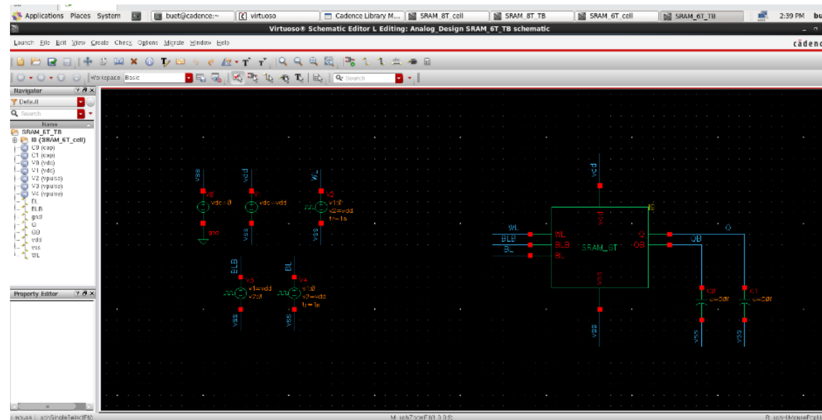

Fig. 3. Test bench configuration for 6T SRAM transient simulation showing voltage sources and load capacitors.

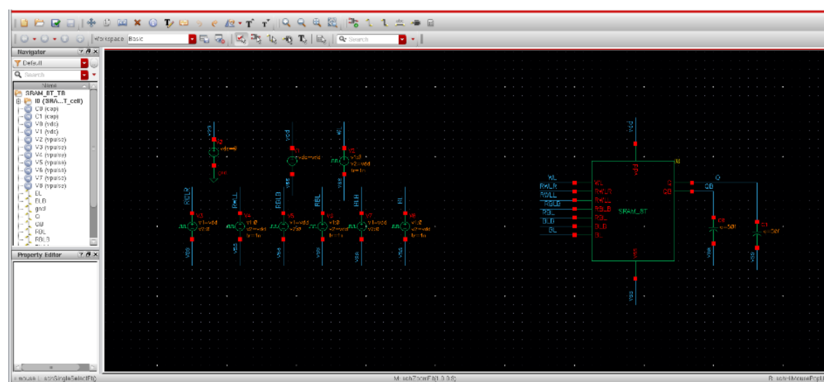

Fig. 4. Test bench configuration for 8T SRAM transient simulation with separate write and read path excitation.

3.3 Simulation Parameters

Transient analysis was performed over a simulation interval sufficient to capture complete write and read cycles which is as shown in Table 4.

Table 4: Pulse parameters configuration

Signal	Initial Value	Pulsed Value	Function
VDD	1.2V(DC)	-	Power Supply
WL (6T/8T Write)	0V	1.2V	Write Access Control
BL	0V	1.2V	Bit Line (Write '1')
BLB	1.2V	0V	Complementary Bit Line
RWL (8T only)	0V	1.2V	Read Word Line
RBL (8T only)	Precharged to VDD	-	Read Bit Line (Output)

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4. RESULTS AND DISCUSSION

4.1 6T SRAM Functional Verification

Transient simulation of the 6T SRAM cell confirms proper write and hold functionality. The waveform captured in Fig. 5 demonstrates the cell's response to write excitation and the response of the cell is as shown in Table 5.

Table 5 : Cell response to write excitation of 6T cell

Node	Voltage	Interpretation
VDD	1.2V(DC)	Stable supply
Q	1.1996 V	Successfully storing logic '1'
BL	1.2 V	Bit line driven high
BLB	0.0 V	Complementary bit line low
WL	0.0 V	Word line inactive (hold mode)

The storage node Q maintains a stable voltage of approximately 1.2V, confirming that the cross-coupled inverter latch is functioning correctly [5]. However, during read access (not shown in the static capture), the 6T cell is known to experience voltage disturbance at the low storage node due to the shared access path.

Fig. 5. Transient simulation results for 6T SRAM cell showing stable storage node Q at 1.1996V with VDD = 1.2V.

4.2 8T SRAM Functional Verification

The 8T SRAM cell was simulated under identical supply conditions. The waveform in Fig. 6 illustrates the operation of the decoupled read path which is shown in Table 6.

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Table 6 : Cell response to write excitation of 8T cell

Node	Voltage	Interpretation
VDD	1.2V(DC)	Stable supply
(Storage Node)	~1.2 V	Logic '1' stored
RWL	1.27 V	Read Word Line asserted
RBL	1.27 V	Read Bit Line responds to RWL
WL	~0.0 V	Write path inactive during read

The key observation is that the read operation occurs through the dedicated RWL-RBL path, completely isolated from the internal storage nodes Q and QB [5]. The storage node Q maintains its value undisturbed during read access, validating the fundamental advantage of the 8T topology.

Fig. 6. Transient simulation results for 8T SRAM cell demonstrating decoupled read operation through RWL and RBL signals.

4.3 Comparative Analysis: 6T vs. 8T SRAM

Table 7 : Comparative Performance Summary

Parameter	6T SRAM	8T SRAM
Transistor Count	6	8
Read Path	Shared with Write	Dedicated (Decoupled)
Read Disturb Vulnerability	Yes	No

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Storage Node Voltage (Hold)	1.1996 V	~1.2 V
Supply Voltage	1.2 V	1.2 V
Technology Node	90 nm planar CMOS	90 nm planar CMOS
Write Mechanism	Single WL, BL/BLB	Single WL, BL/BLB
Read Mechanism	WL + BL/BLB	RWL + RBL
Functional Verification	Passed	Passed

4.4 Discussion

The simulation results confirm that both 6T and 8T SRAM cells are fully functional at the nominal 1.2V supply in 90nm planar CMOS technology. The 8T configuration successfully demonstrates the following advantages:

1. **Read Stability:** The dedicated read port (RWL, RBL) ensures that read current flows through a separate path, leaving the storage nodes Q and QB undisturbed. This eliminates the read disturb vulnerability inherent in the 6T design.
2. **Functional Isolation:** The write word line (WL) and read word line (RWL) operate independently, allowing simultaneous optimization of read and write paths.
3. **Scalability:** The 8T architecture maintains functionality at the same supply voltage as the 6T cell, demonstrating that the additional transistors do not compromise basic operation.
4. **Technology Compatibility:** Implementation in standard 90nm planar CMOS confirms that the design can be fabricated using mature, cost-effective processes.

The marginally elevated voltage observed on RWL and RBL (~1.27V) is attributed to transient overshoot during switching and does not affect the steady-state functionality of the cell.

5. CONCLUSION AND FUTURE WORK

5.1 Summary of Findings

This paper has presented the complete design, implementation, and simulation validation of 6T and 8T SRAM cells in 90nm planar CMOS technology. The key contributions and findings are summarized as follows:

1. **Successful Implementation:** Both 6T and 8T SRAM schematics were successfully designed in Cadence Virtuoso using the gpdk090 process design kit, with functional test benches developed for transient verification.
2. **Functional Validation:** Transient simulations confirm proper write and hold functionality for both topologies at the nominal 1.2V supply voltage.
3. **Read Stability Enhancement:** The 8T cell's decoupled read port effectively isolates the storage nodes from read current, providing inherent immunity to read disturb—a critical advantage for low-voltage, high-reliability applications.
   Performance Baseline: The simulation results establish a reliable baseline for future investigations into power optimization, noise margin analysis, and Monolithic 3D integration.

5.2 Future Work

Building upon the validated designs presented in this paper, the following directions are proposed for future investigation:

1. **Static Noise Margin (SNM) Analysis:** Perform DC noise margin simulations to quantitatively compare the read and write stability of 6T and 8T cells.
2. **Power Characterization:** Measure static (leakage) and dynamic power consumption for both topologies across varying supply voltages.
3. **Power-Delay Product (PDP) Calculation:** Compute the energy-efficiency metric to establish the optimal operating point.
4. **Monolithic 3D Integration:** Extend the design to explore M3D stacking techniques for area reduction and interconnect optimization.
5. **Process Variation Analysis:** Conduct Monte Carlo simulations to assess yield and reliability under manufacturing variability.

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