DESIGN AND SIMULATION OF LOW VOLTAGE LOW POWER COMPARATOR IN 180nM CMOS PROCESS

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Abstract—**A novel design of CMOS dynamic latch Comparator suitable for high speed analog-to-digital converters with High Speed and low power dissipation is presented. The delay analysis of the dynamic comparators will be presented and analytical expressions are derived. By the analysis, a new dynamic comparator is proposed with the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. The design is by adding few transistors; the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. The proposed circuit is designed using 0.18µm CMOS process and simulation is done using Tanner EDA Tools. Simulation results are reported and compared with other comparators using a table, improvements are in result.**

Keywords- ***Double Tail Latched Comparator, Dynamic Latched Comparator, high-speed analog-to-digital converters (ADCs),low-power analog design.***

I. Introduction

A comparator is a device, which compares two currents or voltages and produces the digital output based on the comparison. Comparators are known as 1-bit analog-to digital converter and so they are mostly used in A/D converter. The conversion speed of comparator is limited by the decision making response time of the comparator. As the comparator is one which limits the speed of the converter, its optimization is of utmost importance. Many applications, such as analog to digital converters (ADCs), memory sensing circuits and recently also on chip transceivers are widely using comparators.

In the last years, most of the researchers focus on the comparator with low power consumption, simple thermal management and high efficiency. The growth of the portable electronic devices makes the power consumption is critical issue to circuit designers because the low power and high speed comparators are the main building block in the front end of the radio frequency receiver in the most of the modern telecommunications system

In[1],delay analysis of dynamic comparators has been presented for various architectures. In addition, on the basis of double-tail structure, a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. With the addition of few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification is by considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

Section II provides an overview of the operation of the conventional clocked regenerative comparators in terms of their pros and cons of each topology. Section III describes the modified comparator which is based on structure from [1]. Measurement results are presented in Section IV, followed by conclusions in Section V

II. CLOCKED REGENERATIVE COMPARATOR

A clocked comparator generally consists of two stages. First stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. Clocked regenerative comparators are widely used in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator is shown in fig1.They are widely used in A/D converters because they have high input impedance, rail-to-rail output swing, and no static power consumption.

The operation of the comparator is as follows (see Fig.2).During the reset phase, that means when CLK = 0, *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Outn and Outp to *V*DD to define a start condition and to have a valid logical level during reset. In the decision making (comparison) phase, when CLK = V_{DD}, M_{tail} is on and transistors M_7 and M_8 are off. Output nodes (Out*p*, Out*n*), which had been pre-charged to V_{DD}, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP).

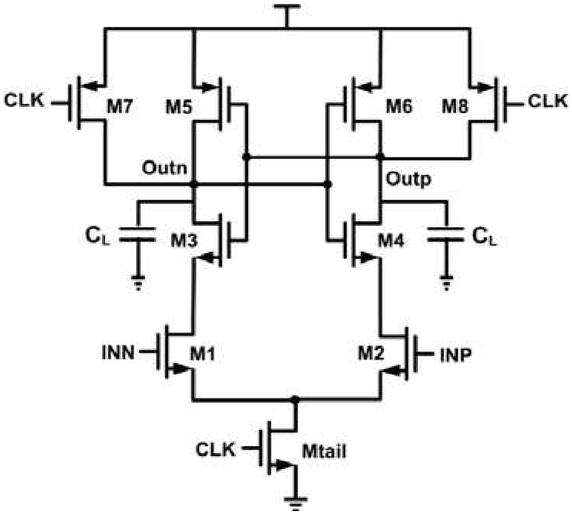

Fig.1.Schematic diagram of the conventional dynamic comparator.

When assume the case where VINP > VINN, Out*p* discharges faster than Outn,transistor M_5will turn on initiating the latch regeneration caused by back-to-back inverters (M_3, M_5 and M_4, M_6). Thus, Out*n* pulls to V_{DD} and Out*p* discharges to ground. If $V_{INP} < V_{INN}$, the circuits works vice versa.

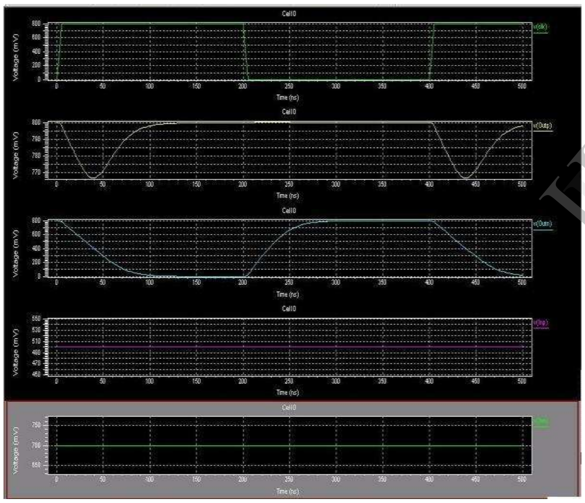

Fig.2.Transient simulations of the conventional dynamic comparator

The disadvantage of conventional dynamic comparator is that due to several stacked transistors, sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate-source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

B. Conventional Double-Tail Dynamic Comparator

A schematic diagram of conventional double-tail comparator is shown in Fig 3.This circuit has less stacking and so they can operate at lower supply voltages compared to the conventional dynamic comparator. Due to the double tail, enables both a large current in the latching stage with wider Mtail2,so fast latching independent of the input common-mode voltage (Vcm), also a small current in the input stage (small Mtail1), so low offset in result.

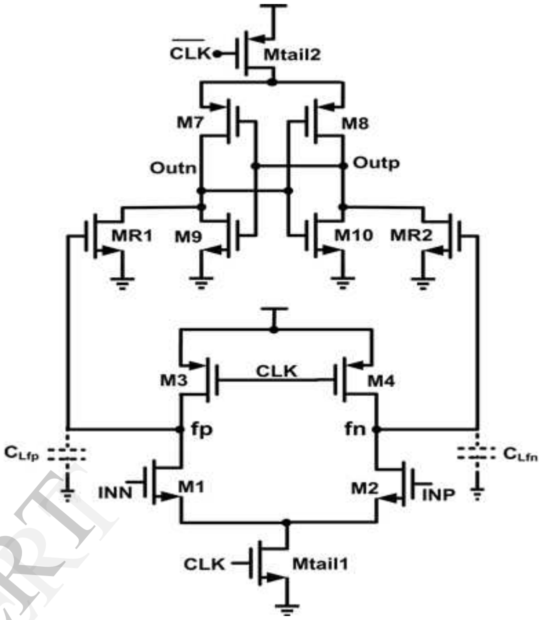

Fig.3.Schematic diagram of the conventional double-tail dynamic comparator.

The operation of this comparator is as follows (see Fig. 4).During reset phase (CLK = 0, M_{tail1}, and M_{tail2} are off),transistors M_3-M_4 pre-charge fn and fp nodes to V_{DD}, which in turn causes transistors M_{R1} and M_{R2} to discharge the outputnodes to ground.

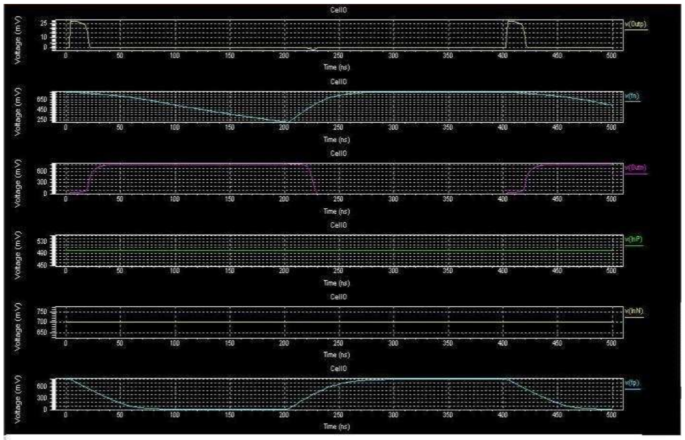

Fig.4.Transient simulations of the conventional double-tail dynamic comparator

During decision-making phase (CLK $=V_{DD}$, M_{tail1} and M_{tail2} turn on), M_3-M_4 turn off and voltages at nodes fn and fp start to drop with the rate defined by $I_{Mtail1}/C_{fn(p)}$ and on top of this, an input-dependent differential voltage $\Delta V_{fn/fp}$ will build up. The intermediate stage formed by M_{R1} and M_{R2} passes $\Delta V_{fn/fp}$ to the cross coupled inverters.

A schematic diagram of a reported double-tail comparator [1] is shown in Fig 5.

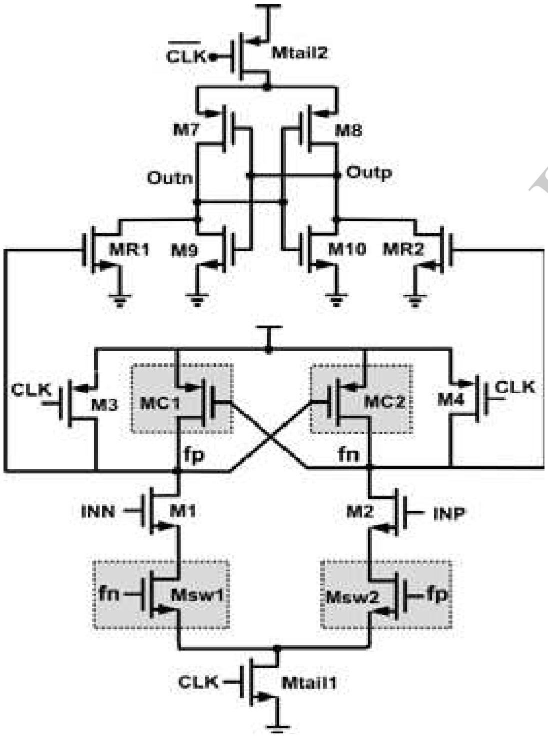

Fig.5.Schematic diagram a double-tail comparator[1]

The operation of the reported double-tail comparator [1] is shown in Fig. 6.The proposed comparator is developed on the basis of its operation. The operation is similar with exception in modified section that will be given in section III.

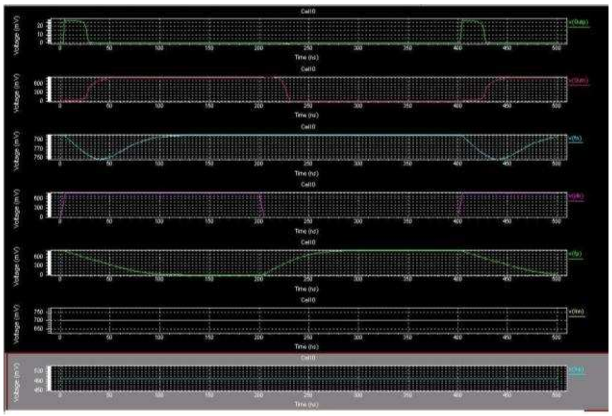

Fig.6.Transient simulations of the proposed comparator

When one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1 , M1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors.

III.PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

The better performance of double-tail architecture in low-voltage application causes the design of the proposed comparator is also in the double-tail topology. The main idea in the design of proposed comparator is to increase $\Delta V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4transistors but in a cross-coupled manner.The operation of the control transistors with the switches emulates the operation of the latch.This can be explained by its operation.

The modified schematic diagram of comparator is shown in Fig.7.The modification of proposed comparator is by using two series connected nMOS transistors in parallel at bottom portion(connected with tail transistor Mtail1).

The operation of the modified double-tail comparator is as follows (see Fig. 8).It also include two phases in its operation. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2 , reset both latch outputs to ground.

During decision-making phase (CLK = VDD, Mtail1,and Mtail2 are on), transistors M3 and M4 turn off. At the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus,fn and fp start to drop with different rates according to the input voltages.

Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the

VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

Conventional double-tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor(M_{c1}) turns on, pulling the other node fp back to the V_{DD}. Therefore by the time passing, the difference between fn and fp ($\Delta V_{fn/fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time. Static power consumption can be avoided by using nMOS switches below the input transistors.

At the beginning of the decision making phase, both fn and fp nodes have been pre-charged to V_{DD} (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. When comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the V_{DD} and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from V_{DD}) but the other switch connected to fn will be closed to allow the complete discharge of fn node.

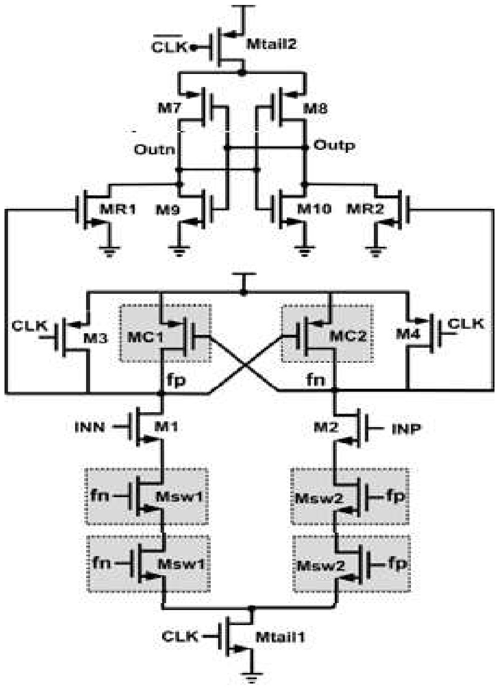

Fig.7.Schematic diagram of the modified comparator

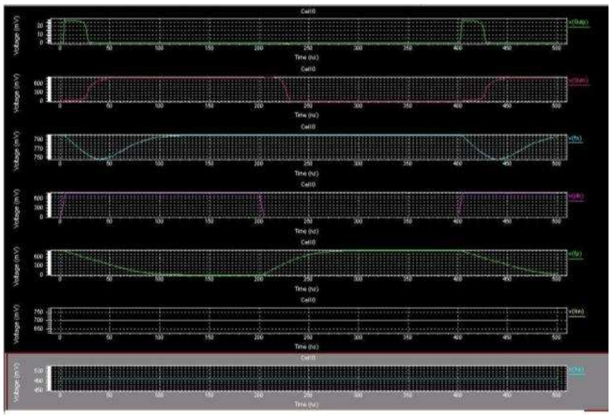

Fig.8.Transient simulations of the modified comparator

IV. MEASUREMENT RESULTS

The modified comparator has been implemented in TSPICE using 180nm CMOS process with 0.8V supply.The width and the length of the transistor used in the design process of the comparator circuit is shown in Table I. Fig. 9 shows the layout of the modified comparator,obtained using micro wind tool. Table II compares the performance of the modified comparators with the conventional dynamic and double-tail comparators.

TABLE I
TRANSISTORS PARAMETERS FOR PMOS AND NMOS

Transistors	Length	Width
NMOS	0.18µ	1.5µ
PMOS	0.18µ	1.5µ

TABLE II
PERFORMANCE COMPARISON

Comparators	Supply voltage(v)	Power(mw)	Delay(ns)
Conventional dynamic comparator	0.8	7	66
Double Tail dynamic comparator	0.8	15	7.5
Proposed comparator	0.8	12	7.4
Modified comparator	0.8	9.5	0.9

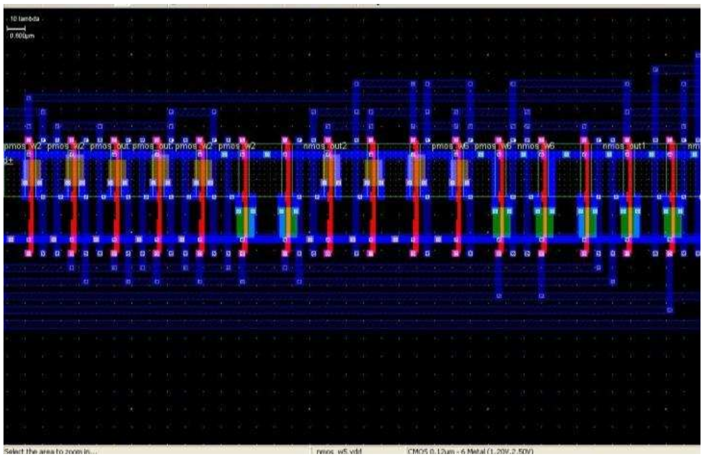

Fig.9.Layout of the modified comparator.

V. CONCLUSION

In this paper, the double-tail topology has an added degree of freedom that enables better optimization of the balance between speed and power. From the simulated result, we concluded that the modified comparator is able to produce higher speed with supply voltage 0.8v, which make them compatible for higher speed ADC application.

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