DESIGN AND SIMULATION OF LOW VOLTAGE LOW POWER COMPARATOR IN 180nM CMOS PROCESS

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Abstract—A novel design of CMOS dynamic latch Comparator suitable for high speed analog-to-digital converters with High Speed and low power dissipation is presented. The delay analysis of the dynamic comparators will be presented and analytical expressions are derived. By the analysis, a new dynamic comparator is proposed with the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. The design is by adding few transistors; the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. The proposed circuit is designed using 0.18µm CMOS process and simulation is done using Tanner EDA Tools. Simulation results are reported and compared with other comparators using a table, improvements are in result.

Keywords- Double Tail Latched Comparator, Dynamic Latched Comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.

II. CLOCKED REGENERATIVE COMPARATOR

A clocked comparator generally consists of two stages. First stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. Clocked regenerative comparators are widely used in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator is shown in Fig.1. They are widely used in A/D converters because they have high input impedance, rail-to-rail output swing, and no static power consumption.

The operation of the comparator is as follows (see Fig.2). During the reset phase, that means when CLK = 0, $M_{tail}$ is off, reset transistors ($M_7$–$M_8$) pull both output nodes $Outn$ and $Outp$ to $VDD$ to define a start condition and to have a valid logical level during reset. In the decision making (comparison) phase, when CLK = $VDD$, $M_{tail}$ is on and transistors $M_7$ and $M_8$ are off. Output nodes ($Outp$, $Outn$), which had been pre-charged to $VDD$, start to discharge with
different discharging rates depending on the corresponding input voltage (INP). M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

B. Conventional Double-Tail Dynamic Comparator

A schematic diagram of conventional double-tail comparator is shown in Fig 3. This circuit has less stacking and so can operate at lower supply voltages compared to the conventional dynamic comparator. Due to the double tail, enables both a large current in the latching stage with wider Mtail2, so fast latching independent of the input common-mode voltage (Vcm), also a small current in the input stage (small Mtail1), so low offset in result.

Fig. 1. Schematic diagram of the conventional dynamic comparator.

When assume the case where \( V\text{INP} > V\text{INN} \), Outp discharges faster than Outn, transistor M5 will turn on initiating the latch regeneration caused by back-to-back inverters (M5, M3 and M4, M6). Thus, Outn pulls to \( V\text{DD} \) and Outp discharges to ground. If \( V\text{INP} < V\text{INN} \), the circuits works vice versa.

Fig. 2. Transient simulations of the conventional dynamic comparator

The disadvantage of conventional dynamic comparator is that due to several stacked transistors, sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate-source voltage of

Fig. 3. Schematic diagram of the conventional double-tail dynamic comparator.

The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M5-M6 pre-charge fn and fp nodes to \( V\text{DD} \), which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground.
During decision-making phase (CLK = VDD, Mtail and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by I_{Mtail}/C_{chip}. And on top of this, an input-dependent differential voltage ΔV_{fn/fp} will build up. The intermediate stage formed by MR1 and MR2 passes ΔV_{fn/fp} to the cross-coupled inverters.

A schematic diagram of a reported double-tail comparator [1] is shown in Fig 5.

The operation of the reported double-tail comparator [1] is shown in Fig. 6. The proposed comparator is developed on the basis of its operation. The operation is similar with exception in modified section that will be given in section III.

When one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors.

III. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

The better performance of double-tail architecture in low-voltage application causes the design of the proposed comparator is also in the double-tail topology. The main idea in the design of proposed comparator is to increase ΔV_{fn/fp} in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner. The operation of the control transistors with the switches emulates the operation of the latch. This can be explained by its operation.

The modified schematic diagram of comparator is shown in Fig. 7. The modification of proposed comparator is by using two series connected nMOS transistors in parallel at bottom portion (connected with tail transistor Mtail1).

The operation of the modified double-tail comparator is as follows (see Fig. 8). It also includes two phases in its operation. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.

During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. At the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages.

Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the
VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

Conventional double-tail dynamic comparator, in which $\Delta V_{f_n/f_p}$ is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor(Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp ($\Delta V_{f_n/f_p}$) increases in an exponential manner, leading to the reduction of latch regeneration time. Static power consumption can be avoided by using nMOS switches below the input transistors.

At the beginning of the decision making phase, both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. When comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node.

Fig.7. Schematic diagram of the modified comparator

**IV. MEASUREMENT RESULTS**

The modified comparator has been implemented in TSPICE using 180nm CMOS process with 0.8V supply. The width and the length of the transistor used in the design process of the comparator circuit is shown in Table I. Fig. 9 shows the layout of the modified comparator, obtained using micro wind tool. Table II compares the performance of the modified comparators with the conventional dynamic and double-tail comparators.

**TABLE I**

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Length</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.18μ</td>
<td>1.5μ</td>
</tr>
<tr>
<td>PMOS</td>
<td>0.18μ</td>
<td>1.5μ</td>
</tr>
</tbody>
</table>

**TABLE II PERFORMANCE COMPARISON**

<table>
<thead>
<tr>
<th>Comparators</th>
<th>Supply voltage(V)</th>
<th>Power(mw)</th>
<th>Delay(ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional dynamic comparator</td>
<td>0.8</td>
<td>7</td>
<td>66</td>
</tr>
<tr>
<td>Double Tail dynamic comparator</td>
<td>0.8</td>
<td>15</td>
<td>7.5</td>
</tr>
<tr>
<td>Proposed comparator</td>
<td>0.8</td>
<td>12</td>
<td>7.4</td>
</tr>
<tr>
<td>Modified comparator</td>
<td>0.8</td>
<td>9.5</td>
<td>0.9</td>
</tr>
</tbody>
</table>
V. CONCLUSION

In this paper, the double-tail topology has an added degree of freedom that enables better optimization of the balance between speed and power. From the simulated result, we concluded that the modified comparator is able to produce higher speed with supply voltage 0.8v, which make them compatible for higher speed ADC application.

REFERENCES


