International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 4 Issue 04, April-2015

Design and Simulation of FPGA Based Digital Controller for Single Phase Boost PFC Converter

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***Abstract*—This paper present a design of the digital controller for continuous conduction mode Boost converter with power factor correction (PFC) on Xilinx FPGA. It is designed to fulfil the international energy standards on input current harmonic distortion by reducing total harmonic distortion (THD) and improving the power factor of power supplies. In Proposed digital controller both outer loop, proportional-integral voltage compensator and inner loop, Average current compensator are implemented in Xilinx block sets in MATLAB/SIMULINK software integrated with Xilinx System Generator. A model of 650W FPGA-controlled boost PFC converter with 98~120 V in the ac input and 390V in the dc output has been simulated in MATLB/SIMULINK using Xilinx System Generator(XSG) environment.**

I. INTRODUCTION

In recent years, most of the electronics and electrical appliances such as desktops, VFD, SMPS, UPS, and laptops work on D.C supply. So as to supply DC-applications from the AC-grid with low harmonic content of the input current, high efficiency and power factor correction (PFC), front end bridge rectifiers with boost PFC converter, are widely used to meet international energy standards and programs, such as the IEC 1000-3-2 and ENERGY STAR's 80 PLUS program[1-2].

In this regard, due to advancement in field programmable gate array(FPGA),microcontrollers and digital signal processors technologies, including expansion of the processing capacity, design flexibility, easiness for system integration and cost reduction, the digital control is becoming more suitable for applications in power converters operating at high frequency over the analog control[4]. The FPGA is a programmable digital logic device by software. Thus, it can perform any logic function such as digital interface, controllers, numeric processors and decoders in a single IC. Two of the main characteristics of the FPGAs are the great versatility and the capacity of execute different tasks in parallel. These characteristics give to FPGAs a great advantage over DSPs in some of the applications on power electronics.

Recently, there are some researches on the digital control of ac-dc PFC converter based on FPGAs [5-12]. A new duty cycle determination algorithm was proposed in [5]. The algorithm includes two terms, the current term and the voltage term, which can be calculated in parallel. A predictive control for PFC was proposed in [6, 7], in which the zero cross detector and sine wave look-up table are used. Digital charge control was presented to implement PFC based on a FPGA [8]. A design of a synchronous state machine to control a PFC boost converter with FPGA was propose in [9]. FPGA was applied to the dual boost PFC converter was proposed in [10, 11]. In high power applications, continuous conduction mode (CCM) is often used due to lower conduction losses and reduced EMI filtering requirements. Compared to peak current control or hysteresis current control, average current control is commonly used for boost PFC operating in CCM mode because of its higher power factor and less sensitive to switching noise. A FPGA based average current-mode controller for CCM boosted converter was implemented on DE2-70 FPGA kit in [12].external three ADCs are used to interface the boost converter with FPGA kit.

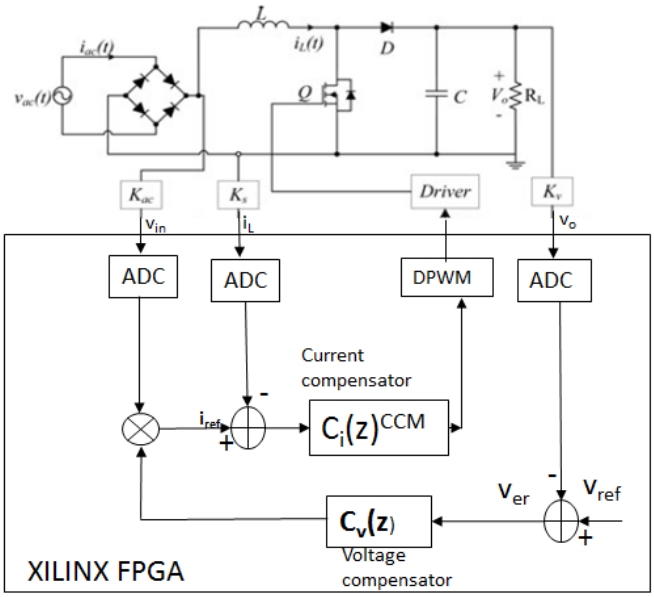


Fig. 1. Block diagram of FPGA based digital controller of Boost PFC converter

In this paper, the design of FPGA controller for the CCM boost PFC converter is proposed, Fig. 1 illustrated the control block diagram and topology of the boost PFC in details. The small-signal models of inner current loop and outer voltage loop are derived for the design of current and voltage compensators. Simulink is used for designing various block of digital controller and for simulation purpose. Xilinx system Generator 14.5 is used to design Xilinx Block set. System Generator for DSP

provides the capability to model and implement high performance DSP systems in field-programmable gate arrays using Simulink. System Generator converts a Simulink model of Xilinx blocks into an efficient hardware implementation that combines synthesisable VHDL and intellectual property blocks that have been hand-crafted to run efficiently in FPGAs.

II. CONTROLLER DESIGN

The control system includes a proportional-integral voltage controller with anti-windup action, which regulates the converter's output voltage and an average current controller based on the model of the converter, which aims to make the converter's input current follow the sinusoidal waveform of the input voltage, providing high power factor and low total harmonic distortion.

The voltage controller has a slow dynamics and is executed once in each half cycle of the input voltage, that is, with frequency equal to 60 Hz. The current controller, on the other side, has a fast dynamics and is executed once in each switching cycle of the converter, that is, with frequency equal to 500 kHz.

The goal of the PI voltage controller is to maintain the output voltage of the converter constant and equal to the designed value, with steady-state null error. This function must be performed even when the converter is subjected to variations in the input voltage and/or in the supplied output load. The PI controller was chosen due to its simplicity and good results. The voltage error, that is, the difference between the reference and the actual output voltage of the converter, is the input value of the voltage controller. The fixed current reference, that is, the constant value that must be multiplied by the input voltage, in order to constitute the reference to be followed by the input current of the converter, is the output value of the voltage controller.

A. *Boost Converter Modelling in CCM*

To characterize the dynamic properties of the boost PFC converter under CCM operation, it is necessary to know the effects of duty cycle d on inductor current i_L. Although the boost PFC does not have a static quiescent operating point due to the low frequency input voltage, a linearized plant model can be found applying averaging techniques [3][13][14].so, in terms of the dynamic CCM operation, it can be shown that through averaging, the linearized small-signal continuous model of the CCM boost PFC control-to-output transfer function G_i^{CCM} is given by (1) as presented in [3], In (1), the output voltage is V_o, boost inductance is L.

$$G_i^{CCM}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_o}{sL}. \quad (1)$$

B. *Design of Current compensator*

Characterizing the response of the open-loop boost PFC converter requires writing the gain T_i^{ccm} the system, graphically represented by the system block of Fig.2 and mathematically written as in (2)

$$T_i^{CCM} = G_i^{CCM}\, C_i^{CCM}\, K_{ADC}\, K_s G_{delay}(s) \quad (2)$$

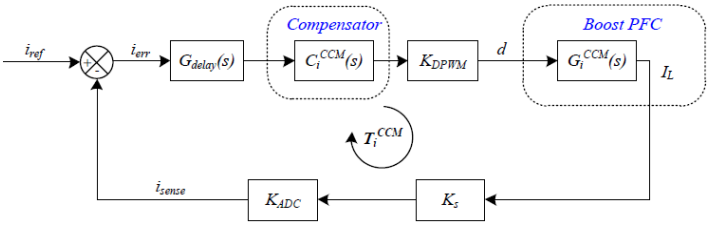


Fig.2 System block diagram of CCM boost PFC converter.

The system consists of the sensor gain products, as well as the transfer function products of the boost PFC converter inductor current and current compensator. The gains are: ADC gain K_{ADC}, current sensor network gain K_s, boost PFC CCM inductor current power stage transfer function G_i^{CCM}, and the CCM current compensator transfer function C_i^{CCM}. Additionally, a delay term $G_{delay}(s)$ is incorporated to account for the computation and ADC sampling delays, and is considered as half the single sampling period delay Ts.
The system is adequately compensated by average current control [3]. The inner current loop is a fast loop with a bandwidth generally selected to be within 1/10th to 1/6th the switching frequency f_s [14]. With f_s = 130kHz, this translates to a range of 13 kHz to 24 kHz.

III. SIMULATION RESULTS

This section shows the simulation results of the operation of the CCM boost PFC converter when subjected to variations in the input voltage and in the output load, in order to evaluate the proposed control laws. In these simulations, both the current compensator and the voltage compensator are implemented.

The Single phase boost PFC converter is designed with the following specifications: ac input voltage range from 98V to 120V, dc output voltage equal to 390 V, output power up to 650W, line frequency (f) equal to 60 Hz, switching frequency (f_s) equal to 130kHz, inductor (L) equal to 2mH and dc link capacitor (C) equal to 300uF.

The CCM current compensator is designed in MATLAB SISO tool to achieve the desired response characteristics, and the designed continuous-time transfer function of the average current compensator is given by

$$C_i^{ccm}(s) = \frac{0.94(s+2.03*10^4)}{s} \quad (3)$$

Since (3) is in the continuous frequency domain, the compensator must be converted to a discrete format, as a continuous-domain compensator cannot be implemented in a digital device without conversion to a discrete format. Discretization was performed using the bilinear transformation with a sample frequency of 130 kHz and transfer function is given by

$$C_i^{ccm}(z) = \frac{0.9742z-0.8331}{z-1} \quad (4)$$

The current compensator is implemented using the Xilinx block set, the compensator is designed based on the direct form-2 structure of transfer function (4) as shown in Fig.3.

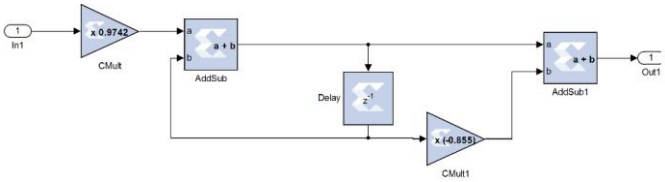


Fig.3 XSG Implementation of current compensator

For the outer loop, the voltage compensator is designed as in (5)

$$cv^{ccm}(s) = 0.9 + \frac{1.5}{s} \qquad (5)$$

Discretization was performed using the bilinear transformation and implemented using Xilinx blocks as shown in Fig. 4

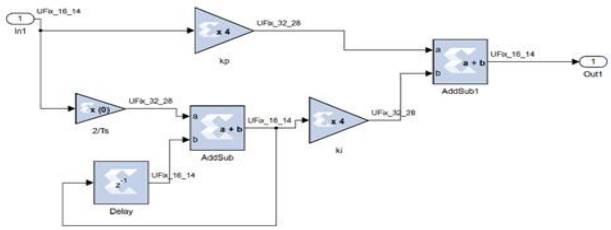


Fig.4 XSG Implementation of voltage compensator

To validate the proposed methodology, extensive dynamic simulations are carried out in

1. MATLAB/SIMULINK environment using power system toolbox for power circuitry in floating point representation.

2. XSG environment using Xilinx block set tools for control circuit in fixed point representation.

The overall block diagram with closed loop control using proposed Xilinx FPGA based digital controller with CCM boost PFC converter is shown in Fig.5 which outlined the communication between FPGA based digital controller and rest of power circuit.

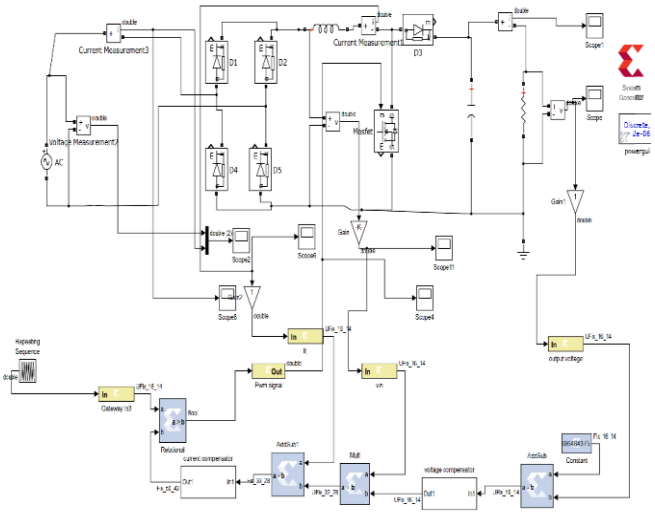
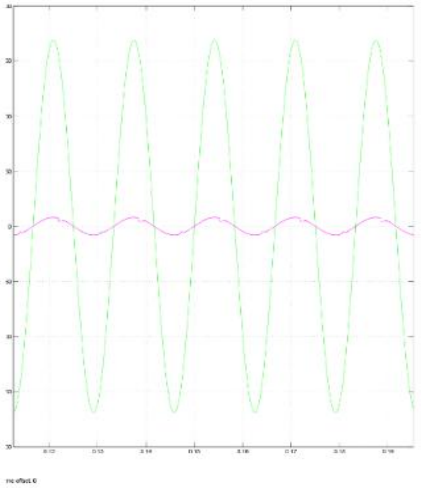
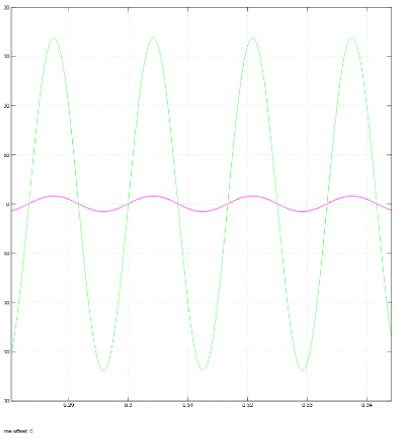


Fig. 5 Simulation circuit diagram in MATLAB/SIMULINK and Xilinx System Generator environment.

The simulated results of input current and input voltage at different loads are depicted in Fig. 6. The input current can follow the input voltage under such condition, the power factor is 0.993 and total harmonic distortion (THD) below 3%...The proposed digital controller can achieve high power factor under the steady state.

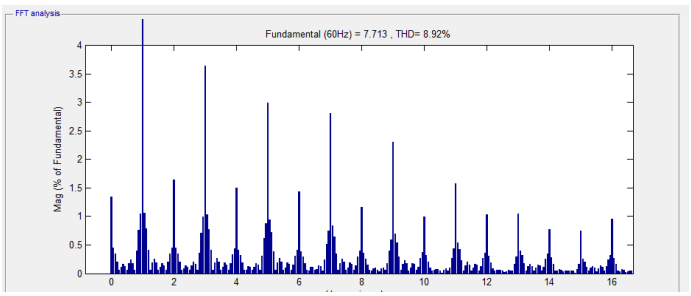


6. (A) simulated Result at 150W

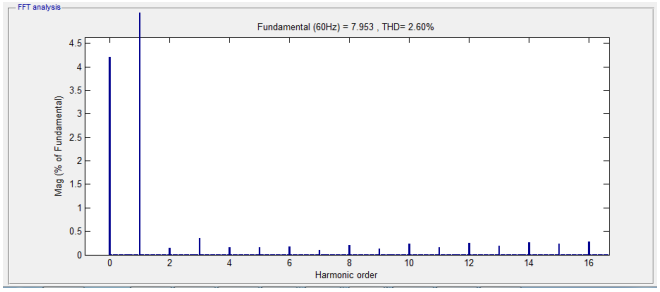


6. (B) simulated Result at 650W

Fig. 6 Input current and input voltage at different loads.



(a)THD at 150W



(b)THD at 650W

Fig. 7 THD at different loads.

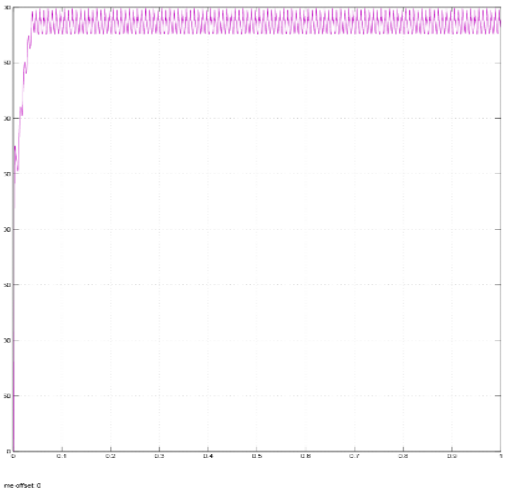


Fig. 8 Regulated output voltage

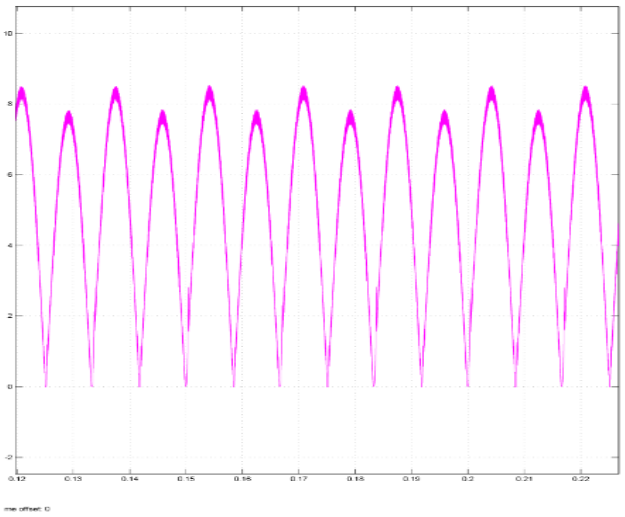


Fig. 9 inductor current at different loads

TABLE.1MEASURED POWER FACTOR AND THD AT DIFFERENT LOAD LEVELS

P_{out} (W)	***150***	***200***	***300***	***400***	***500***	***650***
Power factor	0.89	0.92	0.928	0.953	0.989	0.98
THD (%)	8.7	6.8	4.3	3.9	2.9	2.6

IV. CONCLUSION

This work presents a favorable simulation result in the digital implementation of a FPGA based controller for single-phase boost PFC converter. Modeling and control of the CCM boost PFC current loop to achieve sinusoidal input current under digital average current mode control with voltage regulation by outer voltage loop was described, along with simulation results demonstrating its performance. Simulations of digital controller for CCM boost PFC converter have been done on the platform of MATLAB Simulink environment and Xilinx System generator. Both voltage and current compensators have been generated from Xilinx System generator to control Boost PFC converter. The FPGA based digital controller can be synthesis using Xilinx ISE design tools resulted in the above simulation results for a Spartan3 as target FPGA.

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