Design and Realization of Multiple Valued Logic Gates using Carbon Nanotube FETs

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***Abstract*— Emerging technologies namely Nano scale technologies generally use multiple valued logic (MVL) circuits for improving the speed and information density. Using carbon nanotube field effect transistors, (CNTFETs) the MVL gates are made which use N-type CNTFETs without utilizing any resistor. Thus this work helps both ternary and also quaternary logic gates exploiting the threshold voltages of both P and N type transistors. This work improves in the various power such as propagation, static, switching etc. Along with helping in the improvement of power consumption this project also heads on to the improvement in the efficiency and also improving the area with a bit of propagation delay. The pseudo-NCNTFET MVL logic captures area smaller than other logic circuit but the delay in both the cases seems to be almost same. But in case of the NCNTFET MVL logic the power consumption and the power delay product are larger than the other complementary logic circuits. Leakages and increase in yield are also discussed in the project for the multi valued logic family.**

Keywords*— Multiple valued logic Gates (MVL); carbon nanotube field effect transistor (CNTFET); logic design;

I. INTRODUCTION

According to Moore's law, the number of transistors of an integrated circuit increases exponentially by almost doubling every two years. Scaling of MOSFET technology has been carried out in order to meet the density and sustain the IC predicted by Moore's law. Since the year 2006, the gate length of a MOSFET device has entered the deep submicron/nano regime at 65-nm feature size. As the physical gate length is reduced to below 65-nm, several device-level effects, such as large parametric variations and exponential increase in leakage current, have substantially affected the I-V characteristics of traditional MOSFETs. The scaling of CMOS technology has brought advantages in integrated circuits. Because of the physical limits of the CMOS technology; many new devices such as multiple-valued logic (MVL) operations have been proposed to implement Nano scale circuits. Multiple-valued logic includes the implementation of ternary and quaternary logic, which allows more than two levels of logic for various applications. Compared to binary logic, the multiple-valued logic has many advantages; like for example each wire can transmit more information reducing the complexity of the circuit; hence the area occupied can be reduced. But, multiple-valued logic has disadvantages of lower noise margin in CMOS implementation.

There are many devices that have been proposed for multiple-valued design, for example single electron tunneling devices for modeling memory cells have been proposed using multiple valued logic. The carbon nano tube field effect transistors (CNTFET's) have been considered because of their unique mechanical and electrical properties.
Compared to the silicon based CMOS, the CNTFET have many advantages like sub threshold operation and high mobility charge carriers. The CNTFET provide better power delay product (PDP) benefits over CMOS at 16nm technology, however before fabrication, several challenges must be overcome for these performance benefits. Fabrication of CNFET based on transferred aligned single-walled carbon nanotubes is followed by electrode pattering. To lower the probability of a shortening defect, many fault tolerant techniques have been employed such as metallic CNT tolerant SRAM architecture and metallic CNT modeling and analysis.

In this paper pseudo NCNTFET based multiple valued logic designs have been proposed and presents several figures of merit, such as propagation delay, switching power and static power consumption. The proposed pseudo CNTFET designs are the compared with resistor loaded and complementary CNTFET multiple-valued logic designs.

II. MULTIPLE VALUED LOGIC

Multivalued circuits such as ternary and quaternary circuits have the following advantages over their binary counterparts:
(a) Since in MVL each wire can transmit more information than the binary counterpart, the number of connections inside the chip can be reduced
(b) Since each MVL element can process more information than a binary element, the complexity of circuits can be decreased[1].

III. CARBON-NANO-TUBE FET's

Carbon nano tubes are made up of sheets of graphene that are rolled into tubes. Carbon-nano-tubes are considered to be promising new devices. Carbon nano tubes(CNTs) offer unique mechanical and electronic properties: To control the ability to conduct as either metal or semiconductor depending on chirality. Since the operation principle and device structure are similar to CMOS devices, CMOS fabrication

process and infrastructure can be reused. CNFET has the best experimentally demonstrated device current carrying ability till date. In addition to the electrical properties carbon nanotube FETs are less sensitive to many process parameter variations compared to conventional MOSFETs.

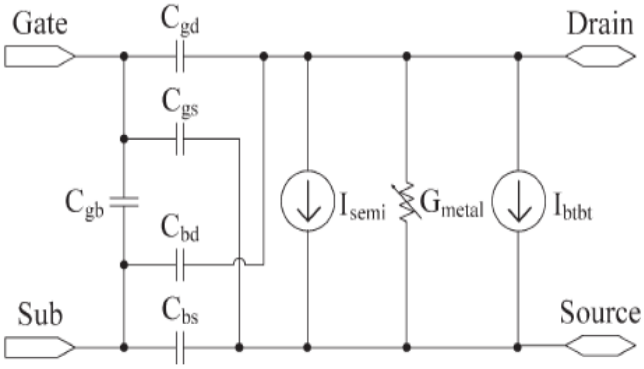
By adjusting the chirality, the appropriate threshold voltage for the CNT can be obtained. The threshold equation for the CNFET is as shown below

$$V_{TH} = \frac{0.42}{D_{CNT}(nm)}$$

Where Dcnt is the diameter of the carbon nano tube. For a CNFET with (n,m) as the chirality and lattice "a" (the carbon-carbon atom distance) the diameter can be calculated as shown

$$D_{CNT} = \frac{a\sqrt{n^2 + mn + m^2}}{\pi}$$

Because of the high mobility of the charge carriers in the CNTFET and also the reduced sub threshold slopes make CNTFET a more suitable design for post CMOS device. The structure of the CNTFET is as shown in fig 1, which illustrates the MOSFET like structure of CNFET and CNFET structure with four tubes



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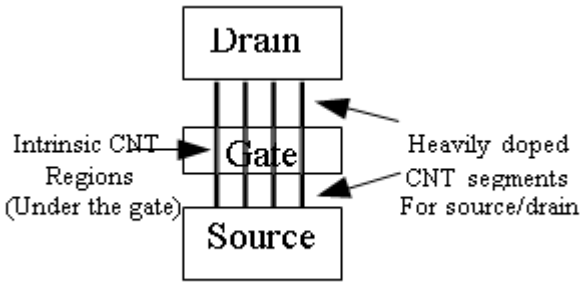
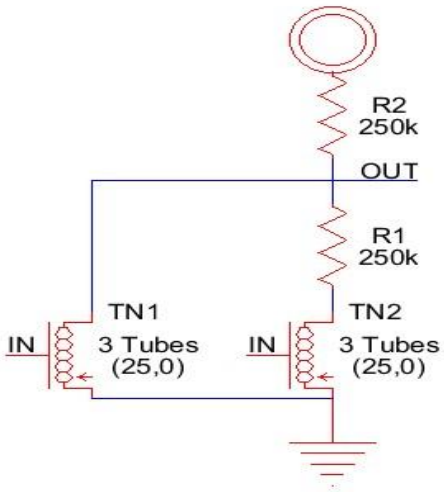


(b)

Fig. 1.(a) MOSFET like CNFET (b) CNFET structure with four CNTs in the channel

II. RESISTOR LOADED AND COMPLEMENTARY CNTFET MODELS

Multiple valued logic gates such as ternary gates have been designed using CNTFET's, and these designs have the feature that the threshold voltage can be controlled by different diameters of the carbon Nano tubes. The ternary and quaternary designs of the resistor loaded model and the complementary CNTFET model; the standard inverter, the positive ternary inverter, the negative ternary inverter and the standard quaternary inverter are show in fig 2 and fig 3 respectively



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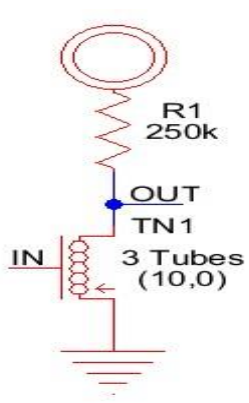

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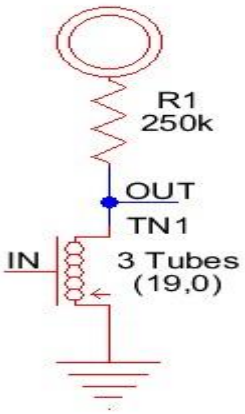

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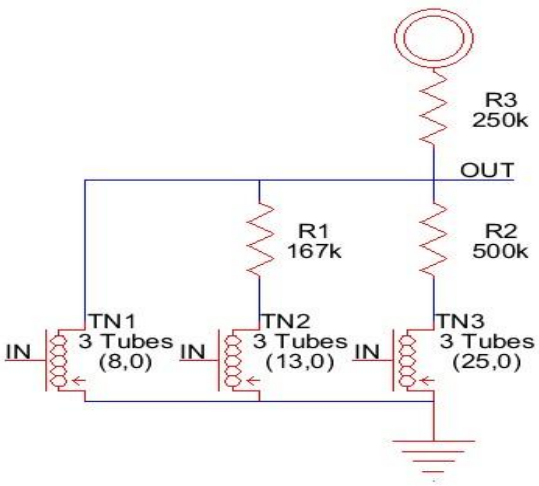


Fig.2 Resistor-loaded CNTFET MVL gates: (a) Standard ternary inverter (STI); (b) positive ternary inverter (PTI); (c) negative ternary inverter (NTI); and (d) standard quaternary inverter (SQI).

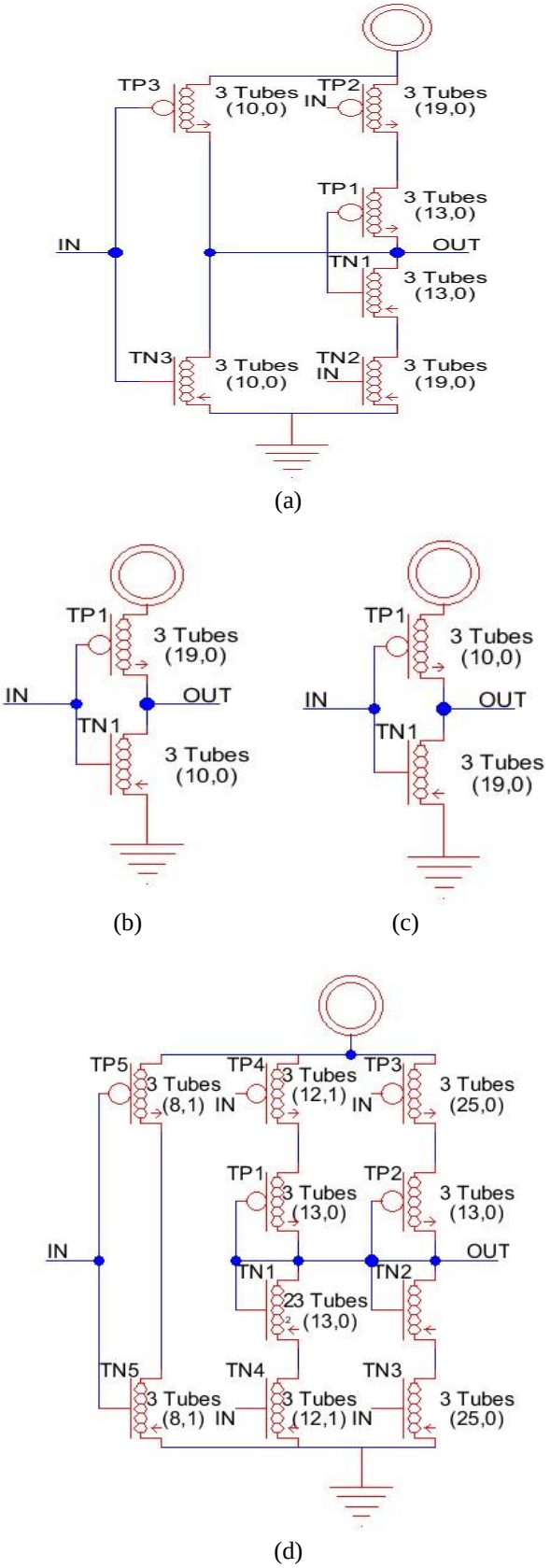
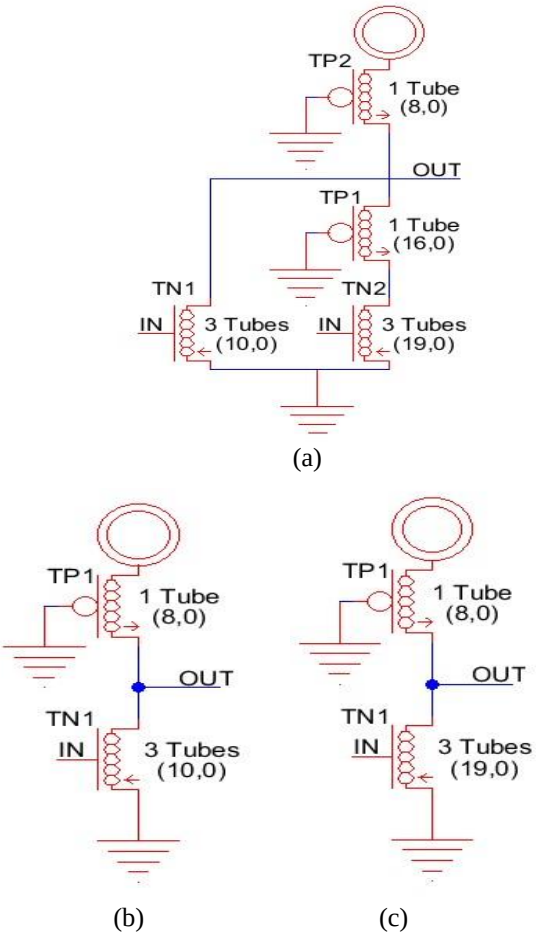


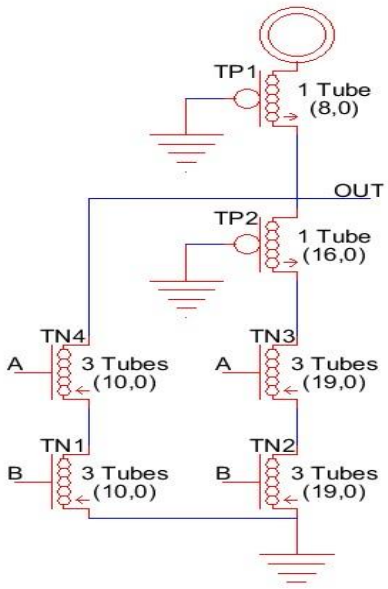
Fig. 3. Complementary CNTFET MVL gates:
(a) standard ternary inverter (STI); (b) positive ternary inverter (PTI); (c) negative ternary inverter (NTI); and (d) standard quaternary inverter (SQI)

III. PSEUDO CNTFET TERNARY AND QUATERNARYLOGIC GATES

The proposed pseudo NCNTFET design replaces the resistor used in paper [4] with a P type CNTFET, while the ground of the P type CNTFET is grounded. The threshold voltage control in this proposed design is accomplished by changing the chirality and the number of carbon Nano tubes in each CNTFET. This design shows the similarities in threshold control of the N type and P type CNTFET and correct operation of multiple valued logic (ternary and quaternary logic) gates.

The pseudo NCNTFET multiple valued logic gates; the STI (c), PTI (positive ternary inverter) and NTI (negative ternary inverter) are as shown in fig 4 and the truth table for the same is shown below.





(d)

Fig. 4. Pseudo-NCNTFET MVL gates: (a) standard ternary inverter (STI) and (b) positive ternary inverter (PTI) (c) negative ternary inverter (NTI) and (d) ternary NMIN operator.

The voltage transfer characteristics for the pseudo NCNTFET ternary gates are shown in fig 5 and the transient simulation for shown in fig 6.

Table 1. Truth table for three ternary inverters

Input	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

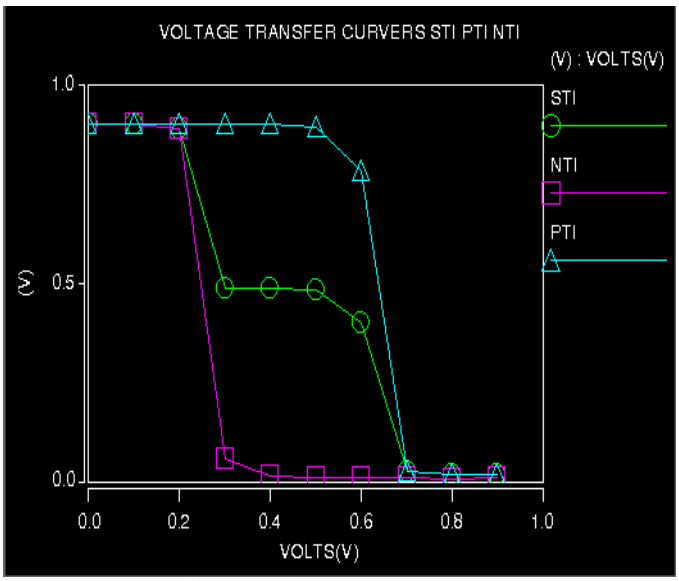


Fig. 5. Voltage transfer diagram for the pseudo-NCNTFET ternary inverters (STI, PTI and NTI).

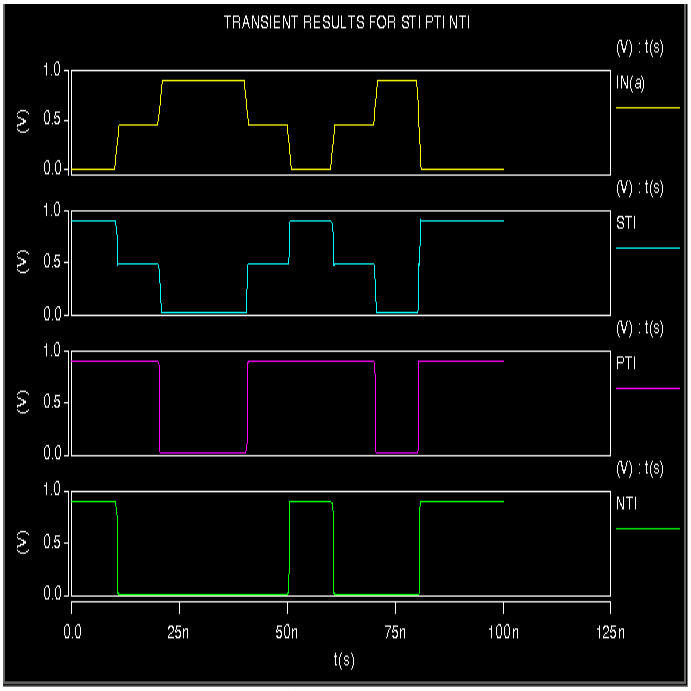
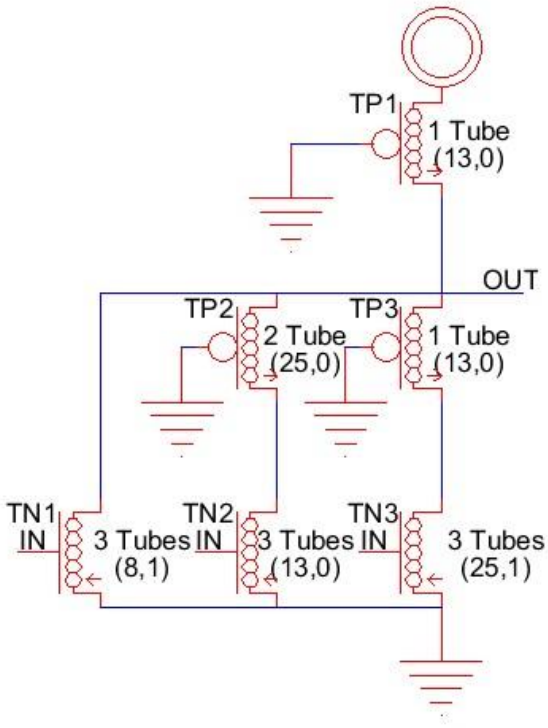


Fig. 6. Transient simulation of the pseudo-NCNTFET ternary inverters.

The pseudo CNTFET quaternary designs; the standard quaternary inverter and the NMIN operator designs have been shown in fig 8 and their respective truth table has been presented.



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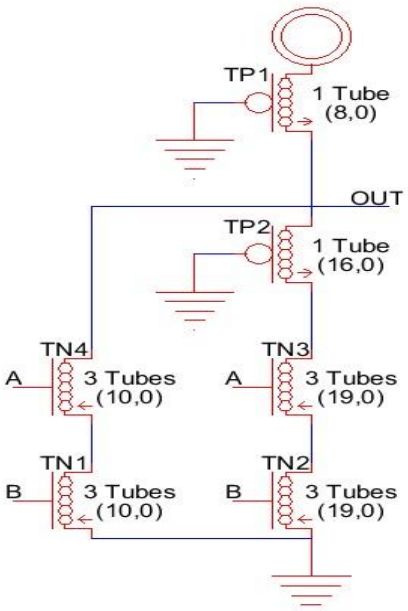

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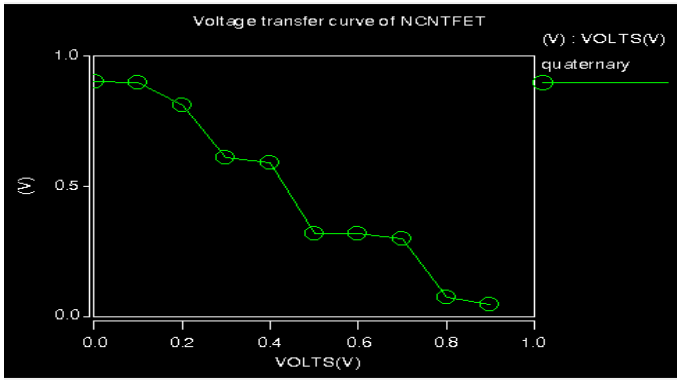
Fig 7. Pseudo-NCNTFET quaternary logic gates: (a) an inverter and (b) an NMIN operator.

Table 2 shows truth table of standard quaternary inverter followed by Fig 8 shows the voltage transfer diagram and the transient result of Pseudo NCNTFET quarternary logic gates

Table 2 Standard Quaternary inverter truth table

IN	OUT
0	3
1	2
2	1
3	0



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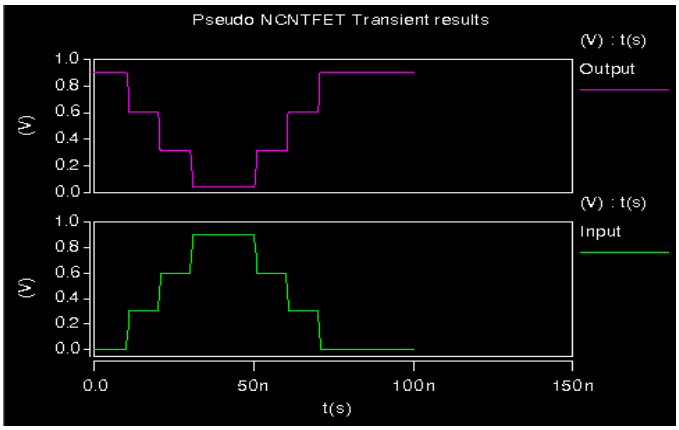

(b)

Fig 8 Pseudo NCNTFET (a) Voltage transfer diagram (b) Transient Results

Table 3 shows the truth table of a quaternary NMIN operator and the following transient results of Pseudo NCNTFET quaternary NMIN operator are shown in fig 9

Table 3 Quaternary NMIN truth table

A	B	OUT	A	B	OUT
0	0	3	2	0	3
0	1	3	2	1	2
0	2	3	2	2	1
0	3	3	2	3	1
1	0	3	3	0	3
1	1	2	3	1	2
1	2	2	3	2	1
1	3	2	3	3	0

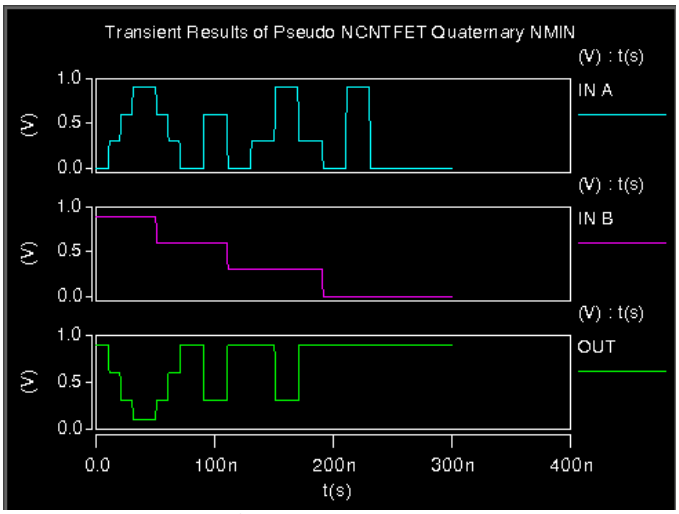

Fig 9 Transient results of Pseudo NCNTFET Quaternary inverter NMIN operator

IV. COMPARATIVE RESULTS

The comparison of various figures of merit for the pseudo NCNTFET multiple valued logic gates with the resistor loaded model is done for power, delay and power dealy product as shown below

Table 4 showing comparative results of STI(Standard ternary inverter) of resistor loaded model, complementary model and pseudo NCNTFET model

	Power	Delay	Power Delay Product
Resistor	4.6068E-06	4.5042E-09	2.03E-17
Complementary	1.1575E-08	4.5289E-09	5.24E-17
Pseudo NCNTFET	6.0854E-07	4.4735E-09	2.72E-15

Table 5 showing comparative results of NTI(Negative ternary inverter) of resistor loaded model, complementary model and pseudo NCNTFET model

	Power	Delay	Power Delay Product
Resistor	4.3946E-06	4.4948E-09	1.98E-14
Complementary	1.1890E-08	4.5302E-09	5.39E-17
Pseudo NCNTFET	6.0854E-07	4.4735E-09	2.72E-15

Table 6 showing comparative results of NTI(Negative ternary inverter) of resistor loaded model, complementary model and pseudo NCNTFET model

	Power	Delay	Power Delay Product
Resistor	2.0761E-06	4.5041E-09	9.35E-15
Complemetary	1.0100E-08	4.5069E-09	4.55E-17
Pseudo NCNTFET	6.0854E-07	4.4735E-09	2.72E-15

Table 7 showing comparative results of SQI(Standard Quaternary inverter) of resistor loaded model, complementary model and pseudo NCNTFET model

	Power	Delay	Power Delay Product
Resistor	2.8648E-06	8.1634E-12	2.34E-17
Complementary	4.3462E-07	2.8845E-12	1.25E-18
Pseudo NCNTFET	8.8998E-07	2.6055E-11	2.32E-17

V. CONCLUSION

In this paper we have presented a new family of Multiple valued logic gates, the Pseudo NCNTFET. The proposed design exploits the threshold voltage control by proper adjustment of chirality and the number of CNT's, and still ensuring correct operation of both MVL i.e ternary and quaternary logic.

Simulation results have been shown using HSPICE. From the comparative results it is evident that, the proposed Pseudo NCNFET logic design have advantages over resistor loaded models in terms of area and power with similar propagation delay. Compared to the complementary design, the proposed Pseudo NCNTFET shows a greater reduction in circuit area with a similar propagation delay but with a larger static power consumption.

The future work will address the effects of chirality variation and impact of multiple tubes.

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