

# Design and Performance Evaluation of Error Detection and Correction using Concatenated BCH and LDPC coding Scheme for Data Streams in Satellite Communication

Girish Kumar N G,  
Research Scholar

Department of Electronics and Communication  
Regional Research Centre,  
Visvesvaraya Technological University  
Belagavi, India

Dr. M N Sree Ranga Raju,  
Professor

Department of Electronics and Communication  
Bangalore Institute of Technology  
Bangalore, India

**Abstract**— Continued Research & Development is of paramount importance in the area of error-revising code turns into a vital interest for the perseverance these days in DVB-S2 and flash memory. LDPC codes are proposed for their exceptional error rectifying capability. Then again, the error floor marvel of LDPC codes may not meet the substantial low error rate requirements of flash memory applications. Along these lines, concatenation of BCH and LDPC codes results in greater harmony between magnificent error remedying capability and low error rate turns into an option coding structure. In this work, concatenated coding scheme is proposed. By looking into the past concatenated coding scheme, our outline enhances the error reducing capability in the waterfall region while keeps low error floor.

**Keyword:** *Low-density parity-check code, BCH code, concatenated code, flash memory, error floor.*

## I. INTRODUCTION

As of late, usage of flash memory in second era satellites like DVB-S2 frameworks and usage of flash memories to store huge amount of data captured by the satellite systems turns into a cutting edge exploration. In particular, the usage of single-level cell flash memory utilizes traditionally Bose-Chaudhuri Hocquenghem (BCH) codes to ensure the uprightness of information, yet the same method may not meet the error insurance for multiple cell flash memory. In this manner, analysts started to look into alternative in error adjusting codes, for example, Low Density Parity Check (LDPC) codes, [1], [2] to upgrade the error adjustment capability for satellite Applications.

LDPC codes have exceptional error rectifying capacity in the waterfall locale. Be that as it may, their error floor sensation limits the use of LDPC codes for satellite media applications that regularly oblige to a greater degree with respect to low error rates. The concatenated coding framework that serially links BCH with LDPC codes is being proposed as an alternative. Our proposed new outline has better error correcting capability in the waterfall region [3].

The rest of the paper is composed as takes after. Section 2 briefs the concatenated codes. The proposed code choice

technique is then introduced in Section 3. Simulated results are presented in Section 4. Section 5 conclusion with future enhancement of this work.

## II. CONCATENATED CODES

Concatenated codes are widely used to increase the efficiency of error control coding. For example DVB-S2 second generation satellite systems, It is good to use highly efficient LDPC codes concatenated with BCH codes to achieve very low error rate which is much necessary for its applications and same coding scheme will also add advantage in the usage of multilevel flash memories for storing the high definition data as only LDPC will leave errors in the waterfall region. Fig 1 illustrates the concatenated scheme. Here the outer code is based on hard decision whereas inner code based on soft decision.

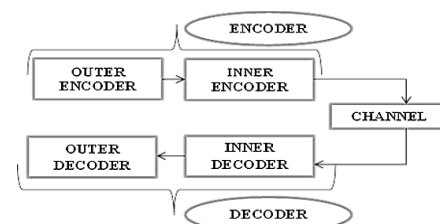


Fig 1. Concatenated codes

### A. BCH codes:

Numerous error revising strategies are exists, one of them is direct block code and the least difficult block codes are Hamming codes. They are fit for remedying stand out irregular error and in this way are not for all intents and purposes helpful, unless a straightforward error control circuit is needed. More advanced error remedying codes are the Bose, Chaudhuri and Hocquenghem (BCH) codes that are a speculation of the Hamming codes for numerous error rectifications. The (Bose-Chaudhuri-Hocquenghem) BCH codes shape a substantial class of capable irregular error remedying cyclic codes having fit for various error revisions. BCH codes work over limited fields or Galois fields and its equipment usage can conceivable on parallel Galois Field (2<sup>m</sup>) [4]. As innovation is changing quickly and the information transmission is being digitize all over the place, a

little error event amid information exchange can degenerate the whole secure data simply like in bank. It is important to recognize such error and right it to get unique data at the receiver.

1. Encoding of BCH codes:

These codes are summed up type of Hamming codes that permits various error redresses. They shape a class of effective arbitrary error redressing cyclic codes which gives a determination of bigger block lengths, code rates and error revising capacity.

BCH codes are characterized by the following parameters

For any positive integer's m where  $m \geq 3$  and t where  $t < 2^{m-1}$  there exist a binary BCH code where [4]:

- Block Length:  $n=2^m-1$
- Number of Parity-Check digits:  $r=n-k \leq mt$
- Minimum distance:  $d_{min} \geq 2t+1$

The Alphabet of a BCH code for  $n=2^m-1$  is represented as the set of elements of an appropriate Galois field,  $GF(2^m)$  where primitive element is  $\alpha$ .

The generator polynomial of the t error correcting BCH code is the Least Common Multiple of  $M_1(x), M_2(x), \dots, M_{2t}(x)$

i.e.,  

$$g(x) = LCM\{M_1(x), M_2(x), \dots, M_{2t}(x)\} \quad (1)$$

Where,  

$$M(x) \text{ Minimal polynomial of } \alpha^i, i=1,2,\dots,2t \quad (2)$$

Since the minimal polynomials for even power of  $\alpha$  are same as for the odd power of  $\alpha$ , then the generator matrix reduces to

$$g(x) = LCM\{M_1(x), M_3(x), \dots, M_{2t-1}(x)\} \quad (3)$$

Then for a given message  $m(x)$  the code polynomial is given by:

In non-systematic form:  

$$C(x) = g(x)m(x) \quad (4)$$

In systematic form:  

$$C(x) = P(x) + x^{n-k}m(x) \quad (5)$$

Where  

$$P(x) = \text{modulo of } \left( \frac{x^{n-k}m(x)}{g(x)} \right) \quad (6)$$

2. Decoding of BCH codes:

Berlekamp Algorithm:

- B. Find out the syndrome  $S=(S_1, S_2, \dots, S_{2t})$  from the received polynomial  $r(x)$
- C. Compute the error Location polynomial  $\sigma(x)$  from the syndrome segments  $S_1, S_2, \dots, S_{2t}$  utilizing the iterative method
- D. Focus the error area numbers.
- E. At that point focus the error polynomial  $e(x)$ .
- F. add  $e(x)$  to the received polynomial  $r(x)$  to get the codeword

For effortlessness it has been utilized thin sense BCH code with settled code rate (0.7) and variable codeword length (n) and variable message length (k) to assess the execution of such code to see the dynamic parameters. Fig.1 represents the aftereffect of BER when utilizing just BCH codes.

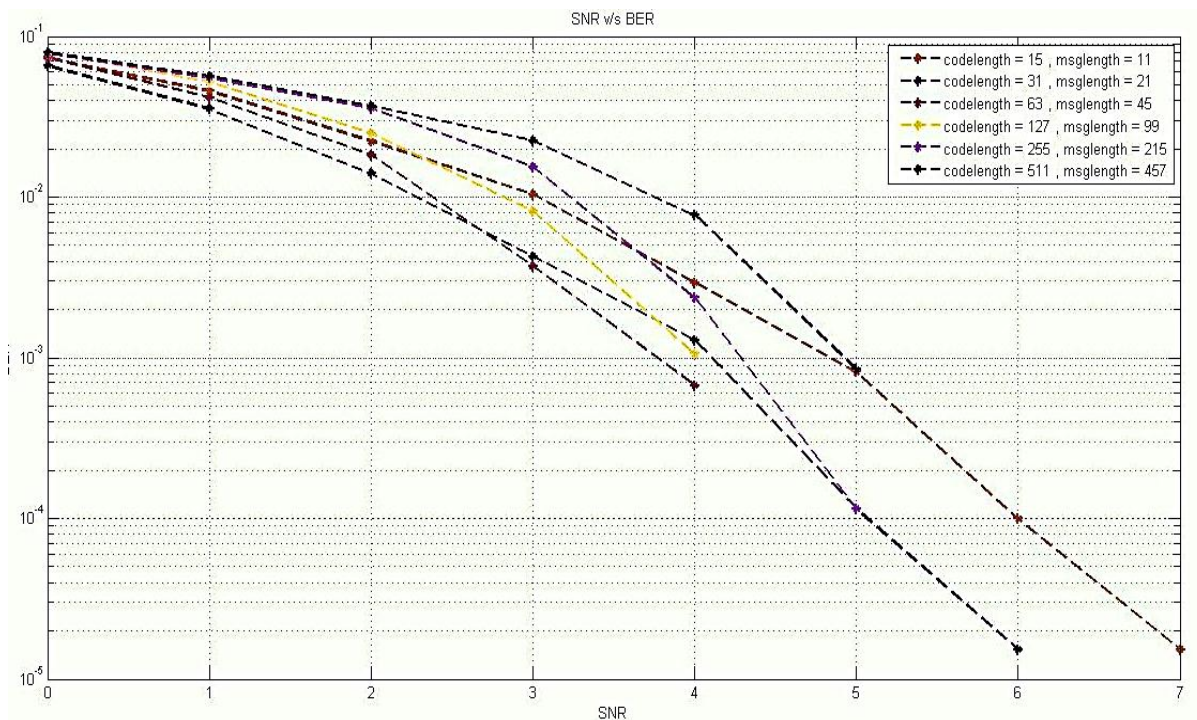


Fig 2. BCH encoding and decoding for Different codewords

B. LDPC codes:

1. Code Structure:

An LDPC code is defined as the null space of the  $(n-k) \times k$  parity check matrix where  $n$  is the block length and  $k$  is the information binary bits. Such matrix consists of  $L$  1's in each row and  $Y$  1's in each column. Where  $Y < L$  and both  $Y$  and  $L$  are small compared to block length  $n$ . the below matrix illustrates the  $(7,3)$  LDPC code parity check matrix with above conditions [4].

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

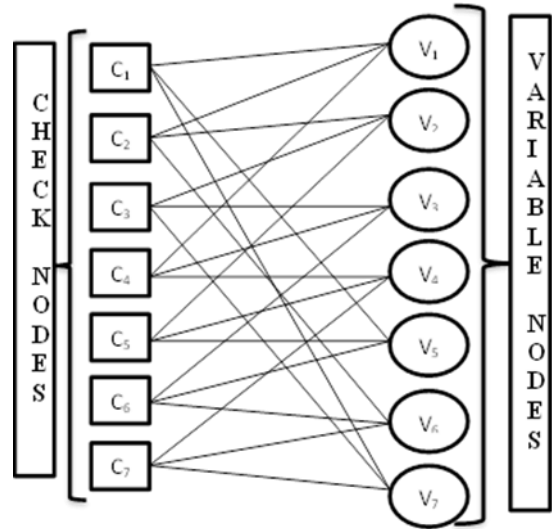


Fig 3. Tanner Graph of (7, 3) LDPC code

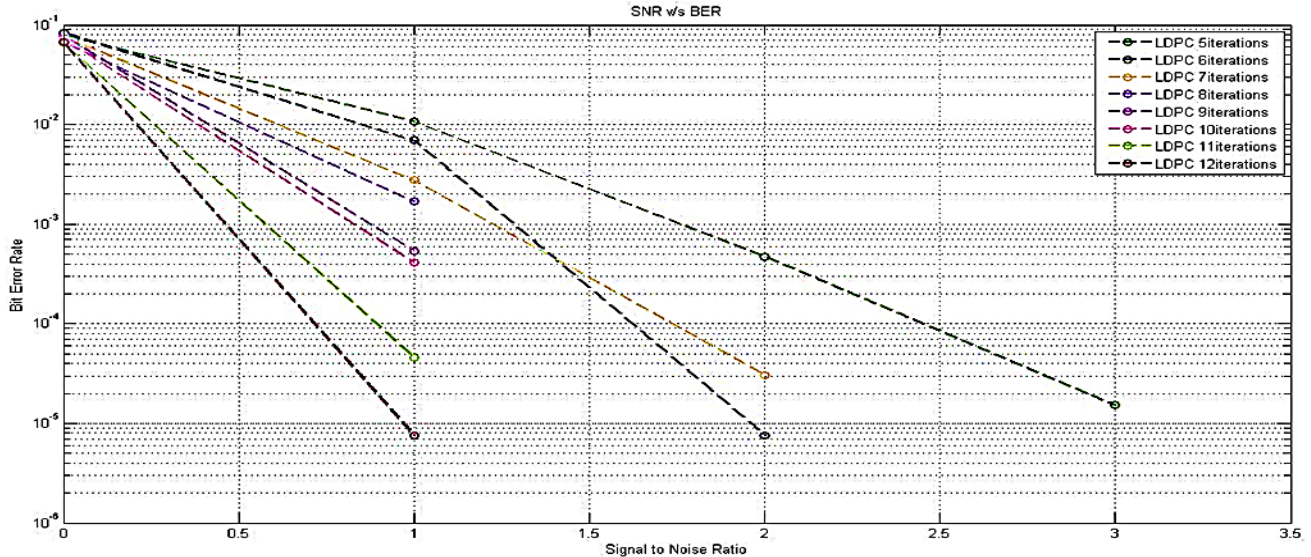


Fig 4. Performance of LDPC codes for various iterations

2. Encoding using LDPC codes:

To perform the encoding the parity check matrix is first converted into a systematic form and then the generator matrix is obtained by:

$$H = [P, I_{n-k}] \tag{7}$$

$$G = [I_k, P^T] \tag{8}$$

This resultant generator matrix is then used to encode.

3. Decoding using LDPC codes:

In this research work sum product algorithm is used for decoding. It exchanges soft information iteratively between variable and check nodes. Here the messages which are getting exchanged are Log Likelihood Ratios. Each variable node of degree  $A_v$  calculates an update of message  $k$  according to [5]:

$$\gamma_k = \gamma_{ch} + \sum_{i=0}^{A_v-1} \gamma_i - \gamma_k^{old} \tag{9}$$

$\gamma_{ch}$  - Channels of LLR  
 $\gamma_i$  - LLR of incident edges

Fig 4 shows simulation result of LDPC code. The parity check matrix used here with dimension of  $(32400 \times 64800)$ , six ones in the first row, seven ones in the (2 to 32400) rows, eight ones in the columns of (1 to 12960) and three ones in the columns (1261 to 32400), while columns (32401 to 64800) form a lower triangular matrix.

It can be observed that using LDPC code only can achieve good performance. It needs only 1 dB signal to noise ratio to achieve  $10^{-5}$  BER with 5 iterations and it can be decreased much more by increasing number of iteration, but the large increase here will introduce delay time which make such system unsuitable for real time applications.



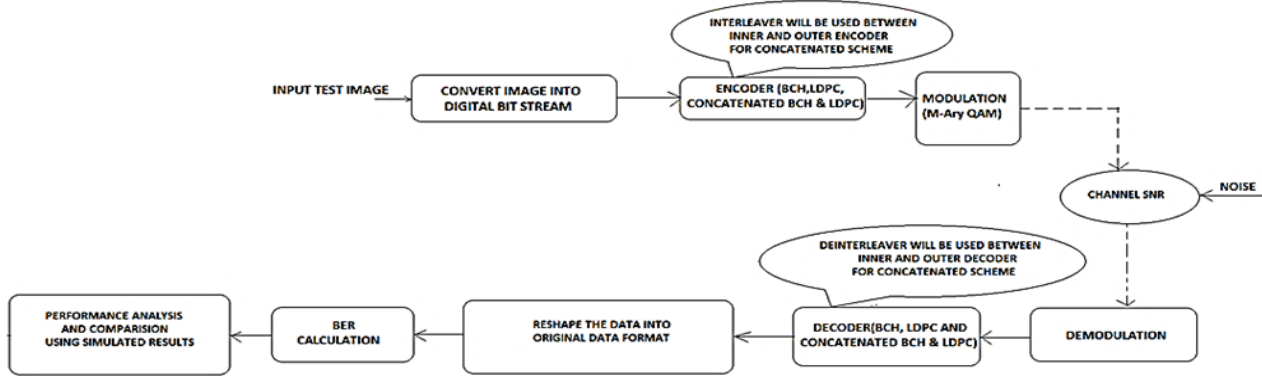


Fig 5. Proposed Model of Concatenated BCH and LDPC code with interleaver

### III. PROPOSED MODEL

As we seen earlier to get a better BER in LDPC more number of iterations should be introduced which makes delay time. So to overcome this issue a concatenated Coding scheme is proposed [6], [7], [8], [9], [10] which concatenates BCH and LDPC as shown in the fig 5.

#### A. Concatenated BCH and LDPC Encoding and Decoding:

In this coding scheme the outer encoder is BCH encoder and Inner Encoder is LDPC encoder. That is one block of data is first encoded by outer BCH encoder and then encoded BCH codeword is partitioned into 'X' equal sized segments, and each segment is encoded by the inner LDPC encoder. Let  $N_{BCH}$  and  $N_{LDPC}$  be the code rate of outer BCH code and inner LDPC code respectively. Then the overall code rate is given by:

$$N_t = N_{BCH} * N_{LDPC} \quad (10)$$

If all the inner code word from LDPC decoder is decoded properly then it is not necessary to used BCH decoder for decoding. Because of LDPC code mis-correction at the waterfall region BCH decoder is used to detect the error practically.

So each  $M_{BCH}$  symbol will be processed by forward error correction encoder to generate  $K_{LDPC}$  symbol codeword. The  $K_{BCH} - M_{BCH}$  parity check symbol of the systematic BCH encoder shall be added after  $M_{BCH}$  symbol and the  $K_{LDPC} - M_{LDPC}$  parity symbol of LDPC encoder are inserted after  $M_{LDPC}$

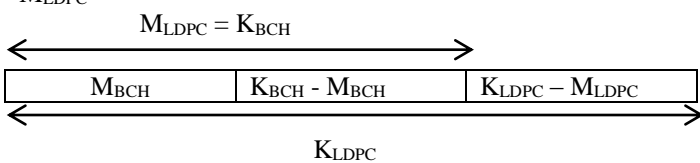


Fig 6. Format of data after encoding

The length of code word for BCH code is  $n=63$ , while the message  $k=45$  only so the code rate is high (0.71) so it will not lead to reduced spectral efficiency but in return allows to reduce the number of iterations which can get good performance suitable to real time applications as shown in Fig.8 which illustrates the results of proposed system.

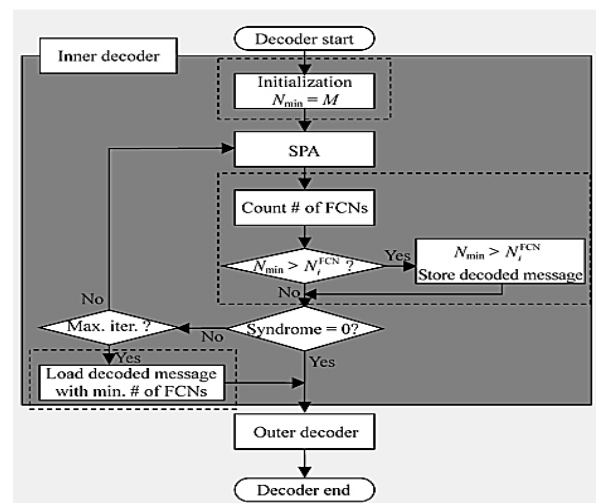


Fig 7. Flowchart for concatenated LDPC and BCH decoder

It is clear that such system achieve nearly to zero BER very near to 0 dB with only 6 iterations, so the curve has become very sharp as seen in Fig 5 which indicate more than 1 dB gain in contrast with the curve of LDPC only so that our system is success to get very low BER with low delay time.

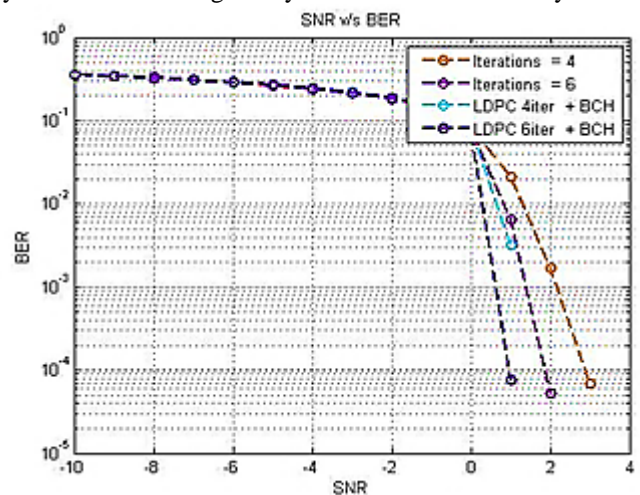


Fig 8. The performance of the proposed scheme

## IV. RESULTS AND CONCLUSION

In this paper it has been examined the execution in terms of BER of BCH and LDPC codes exclusively to pick the suitable parameters that can be utilized for concatenation of BCH (external code) and LDPC (internal code). According to the simulated results obtained for individual BCH only and LDPC only codes, we observe that for BCH coding system to achieve BER of  $10^{-5}$  the SNR should be maximum, it means that the signal strength should be very high. The second issue is if at all to achieve better results in BCH, the code rate should be changed instantaneously. When we observe LDPC codes to achieve BER of  $10^{-5}$  we need to increase the number of iterations at the decoding stage as we see from the fig 4: 12 iterations are needed to achieve BER of  $10^{-5}$ . Increase in iterations will increase execution time. So to overcome these drawbacks we need to propose a coding scheme which can show zero BER under low SNR. Concatenation of BCH and LDPC codes is proposed and the outcomes of this coding scheme demonstrates that such a framework is effective channel code to accomplish low BER which is suitable for satellite applications and multi cell flash memories. Such framework resulted in close to zero BER and outfits the framework with LDPC just alone in more than 1 dB at low SNR which is essential requirement for deep space communications. Thus the simulated results obtained from our work are imperative and confronts most sort of the channel codes.

## REFERENCES

- [1]. R. G. Gallager, "Low density parity check codes," IRE Transactions on Information Theory, IT-8, pp. 21-28, January 1962.
- [2]. D. J. C. Mackay, "Good error-correcting codes based on very sparse matrices," IEEE Transactions on Information Theory, vol. IT-45, no. 2, pp.399-431, March 1999.
- [3]. D. J. C. Mackay and R. M. Neal, "Near Shannon limit performance of low density parity check codes," IEE Electron Letters, vol.32, no. 18, pp. 1645-1646, Aug. 1996.
- [4]. S.Lin and D.Costello, "Error control coding Fundamentals and applications," Prentice Hall, 2nd edition, 2004.
- [5]. Pin-Han Chen, Jian-Jia Weng, Chung-Hsuan Wang, and Po-Ning Chen, " BCH Code Selection and Iterative Decoding for BCH and LDPC Concatenated Coding System", IEEE Communications Letters, Vol. 17, No. 5, May 2013
- [6]. Shin-Lin Shieh "Concatenated BCH and LDPC Coding Scheme With Iterative Decoding Algorithm for Flash Memory" IEEE Communications Letters, VOL. 19, NO. 3, pp. 327-330, March 2015
- [7]. Saba Farheen N.S, Asiya Hazreena, Jose Alex Mathew, Ghouse Ahamed4, Performance Evaluation of LDPC Codes Over Various Channels, Advanced Research in Electrical and Electronic Engineering Print ISSN: 2349-5804; Online ISSN: 2349-5812 Volume 1, Number 1 (2014) pp. 8-11
- [8]. N.Xie, W.Xu, T.Zhang, E.Haratsch, and J.Moon, "Concatenated low density parity check and BCH coding system for magnetic recording read channel with 4 kB sector format," IEEE Transactions on Magnetics, vol. 44, no. 12, pp. 4784-4789, December 2008.
- [9]. Sina Vafi, Huu Dung Pham, "Serially Concatenated Codes with Euclidean Geometry LDPC and Convolutional Codes", IEEE, ICCS 978-1-4673-2054-2, 2012.
- [10]. Tom Richardson, "Error Floors of LDPC Codes", IEEE Trans. Inform. Theory, Vol.47m no. 2, pp. 1426-1435, Feb. 2013

GIRISH KUMAR N G Currently working as Assistant Professor in Bangalore Institute of Technology, Visvesvaraya Technological University, Karnataka, India. Has more than 7 years of teaching experience in Electronics and Communication Engineering. Received the B.E. degree in Electronics and Communication Engineering from Visvesvaraya Technological University, Karnataka, India in 2005. Received the Master of Science Degree in Intelligent Systems in School Of Computing, from University of Sunderland, United Kingdom. Presently he is pursuing his final year M.Sc Engg through Research, with specialization in Electronics and Communication in RRC, Visvesvaraya Technological University, Belagavi, Karnataka, India.

Dr. M N SREERANGARAJU received BE Degree in 1985 from Bangalore University and M.Tech in 1991 from University of Mysore both in Electronics Engineering, and PhD(Telecommunication Engg) from VMU, Salem, TN, India in 2011. Professor of Electronics and Communication Engineering at Bangalore Institute of Technology (BIT), Bengaluru, India has been in Teaching UG and PG Students of Electronics and Telecommunication Engineering students for nearly Thirty Years. He has organized several National level conferences and workshops in this tenure. He has published his Research papers in Prestigious IEEE Conferences held in USA, China, Malaysia and Egypt. He also has served has Session Chair for several National and International Conferences held in India and abroad. He also has served as editor of several journals and Magazine. He holds life member of ISTE, MVLSI, and IMAPS and also member of IEEE. His research interests include mobile and wireless communications and networks, personnel communication services and high speed communication routing protocols and wireless channel modeling.