Design and Performance Analysis of Multipliers using Different Logic Styles

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Abstract-A multiplier is one of the chief hardware blocks in most digital and high concert systems such as microprocessors, digital signal processors, etc. In this paper 4x4 as well as 8x8 Array, Wallace and Vedic multipliers structural design is being designed. Among these three types of multipliers Vedic multiplier base on Vedic arithmetic using Urddha-Tiryabhyam sutra are proved to be the most efficient in terms of lower power consumption. In MOSFET by applying a shrinking technology below 100nm becomes a key challenge for power chip management so to overcome these limitations the CNTFET are introduced, and due to this comparison of multipliers are made between MOSFET 32nm and CNTFET 32nm technology. The CNFET-based multipliers have higher speed, and low power dissipation and it nearly reduces 99% PDP (power-delay product) as compared to the MOSFET. And still to reduce the power consumption the low power technique such as MTCMOS is used and all the three different designs of 4x4 as well as 8x8 multipliers are designed using the Multi-Threshold Voltage CMOS (MTCMOS) it proved to be best among all the implementations. And it nearly reduces 50% of power compare to normal multipliers (i.e. without applying technique). The functionality of all the three designs is based on 32nm Berkeley Predictive Technology Model (BPTM) are calculated at 1v supply voltage and simulating them with hi-spice software.

Keywords - array, Wallace, Vedic multipliers, low power using MTCMOS technique, MOSFET, CNTFET, VLSI.

I. INTRODUCTION

Digital Multipliers are used in all fields like electronics and communication, Digital Signal Processing (DSP), digital Image Processing (IP) telecommunication and broadband communication industries. The multipliers are vital fundamental Arithmetic functional units in many transform, the concert of these transforms strongly depends on the multiplication “Ref.[1-4]”. Multipliers based on emerging technologies like CNFET are more robust and highly efficient than the conventional MOSFET-based multipliers “Ref.[13-16]”. The first array multiplier is designed but it has more digital logic gates and consumes higher power “Ref.[1-4]. So to overcome this issues Wallace multiplier is designed and it is faster than a simple array multiplier because of its non linearity but Wallace trees are often avoided by designers and compare to other multiplier like array, the Wallace multiplier Vedic multiplier is quicker and consumes lesser power “Ref.[5-9]”. Power conservation is a key concern in the VLSI circuit design so here low power technique Multi-Threshold Voltage CMOS (MTCMOS) is applied so efficient power management is achieved “Ref.[17-20]”.

In this paper, analysis and comparison of multipliers using different design techniques are performed. The various three different multipliers are implemented using MOSFET, CNTFET and low power MTCMOS logic style and their comparative analysis are based on power and the PDP (Power delay product) this paper is organized as follows. The Section II brief describes the transistor nanotechnology. Section III structures the 4x4 and 8x8 Array multiplier. Section IV details the 4x4 and 8x8 Wallace multiplier. Section V deals with high speed 4x4 as well 8x8 Vedic multiplier. Section VI comprises the introduction of MTCMOS technique. Section VII presents Comparative analysis of multipliers. Section VIII describes the Conclusion. References are certainly at the end of the paper.

II. TRANSISTOR NANOTECHNOLOGY

The concert benchmarking for nanoscale devices and circuits, contain both CMOS and carbon nanotube field effect transistors (CNFETs). For CMOS technology, it becomes harder to improve device performance by reducing the physical gate length so (CNFET) is the most gifted technology to extend or complement traditional silicon technology due to three reasons: First, the working standard and the device construction are similar to CMOS devices; We can reuse the recognized CMOS design infrastructure next, we can reuse CMOS manufacture process. And the mainly essential reason is that CNFET has the best experimentally verified device’s current carrying ability to date. We now compare CNFET circuit performance with CMOS circuits benchmarked with the standard digital library cells, including INV, NAND, NOR, ADDER, MULTIPLIER, MUX, LATCH, DFF, and so on. Compared to silicon technology, CNFET shows improved device performance (based on the intrinsic CV/I gate delay metric (6x for nFET and 14x for pFET) than a MOSFET device at the 32 nm node, with device non-idealities. This outsized speed improvement is extensively degraded (~5x degradation) by interlock capacitance in a real circuit environment. Growing the number of CNTs per device is the most valuable way to progress the circuit speed. Compared to CMOS circuits, CNFET circuits with 1 to 10 CNTs per device is about 2x to 10x faster, the energy
consumption per cycle is about 7× to 2× lower, and the energy-delay product (EDP) is about 15× to 20× lower, considering the realistic layout pattern and the interconnect capacitance. “Ref. [13-16]”.

“Fig.1,” Complete CNFET device model is implemented with hierarchical three levels. Level 1, CNFET_L1, models the intrinsic behavior of CNFET. The second level, CNFET_L2, includes the device non idealities. The first two levels deal with only one CNT under the gate. The top level, CNFET_L3, models the interface between the CNFET device and CNFET circuits. This level deals with multiple CNTs per device and includes the parasitic gate capacitance and screening due to adjacent CNTs.

III. ARRAY MULTIPLIER

Array multiplier is well known due to its regular structure. For m*n Array Multiplier, it needs m*n AND gates, n HAs, (m-2)*n FAs, (total (m-1)*n Adders).Multiplier circuit is based on adding and alter algorithm. Each partial result is generated by the multiplication of the multiplicand with one multiplier bit. The partial result is altered according to their bit commands and then added. The addition can achieve with normal carry save adder. N-1 adders are essential where N is the multiplier length. “Ref. [1-4]”

A. 4X4 ARRAY MULTIPLIER

Consider the multiplication of two unsigned n-bit numbers, where X = Xn...X2...X0 is the multiplicand and Y =Yn...Y2...Y0 is the multiplier. We have 4-bit multiplier and 4-bit multiplicand. We can generate 4-rows of partial products as shown in the "Fig. (2)".In a digital method an array multiplier involves the parallel multiplication, which is done in the following three steps:

1. Creation of partial result (PP) bits.
2. The addition of partial result (PP) bits into two Rows.
3. The calculation of final product generally using a carry propagate adder (CPA). “Ref. [2]”

“Fig.2,” 4x4 Multiplications

B. 8X8 ARRAY MULTIPLIER

The multiplier is a complex adder array structure. The performance and characteristics of multiplier depend on the algorithm in which they are operated. Bit array multiplier has regular and simple structure to explain. For 8*8 Array Multiplier, it needs 8*8 AND gates, 8 HAs, (8-2)*8 FAs, (total (8-1)*8 Adders).Fig. 4 Shows the architecture of standard 8x8-array multiplier, where HA and FA are the half and full adders respectively. The advantage of the bit-array multiplier is its ease of design for a pipelined architecture. “Ref. [3]”

“Fig.3,” 4X4 array multiplier

IV. WALLACE TREE MULTIPLIER

Wallace tree multiplier is a tree based multiplier. When evaluate to the other multipliers Wallace tree multiplier is the high rapid multiplier. “Ref. [10]” The summing of the partial result bits in parallel using a tree of carry save adder became commonly known as the “Wallace Tree”. Three step processes is used to multiply the numbers.

“Fig.4,” Architecture of 8X8 array multiplier
The Wallace tree has three steps:
1. Partial result creation Stage
2. Partial result decreases Stage
3. Partial result Addition Stage

A. 4X4 WALLACE MULTIPLIER

The total process of Wallace tree multiplication can be explained as: For a n x n multiplication there is n² partial result that have to be summed. The 1st step in the algorithm involves grouping the partial products into sets of 3. For example, if there are n ' rows of partial results, 3*[n/3] rows are grouped and the remaining n mod 3 rows are passed to the next stage. Therefore, three rows of partial products are grouped together in stage 1. These 3 rows are then summed using full adders and if there are 2 dots in particular column half adders are used.

B. 8X8 WALLACE TREE ARCHITECTURE

In the conventional 8 bit Wallace tree multiplier architecture number of addition operations is required. Using carry save adder, three partial result terms can be a point to structure the carry and sum. The sum signal is used by the full adder of the subsequent level. The carry signal is used by the adder occupied in the generation of the next output bit with a resulting overall delay proportional to log 3/2 N, for N number of rows.

V. VEDIC MULTIPLIER

Vedic multipliers are based on Vedic Sutras. Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the Urddhav-Tiryakbyham Sutra is one of the most highly preferred algorithms for performing multiplication.

A. Urdhav-Tiryagbyham rule

It is the common sutra suitable for all types of multiplication, which means “vertically and crosswise” and it makes nearly all the numeric calculations quicker and easier. The main benefit of using this algorithm in contrast with the existing multiplication techniques, is the fact that it utilizes simply logical “AND” operations, half adders and full adders to entire the multiplication operation. Also, the partial results required for multiplication are generated in parallel and a priori to the actual addition thus saving a lot of processing time. “Ref. [5]”

Vedic multipliers are based on Vedic Sutras. Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the Urddhav-Tiryakbyham Sutra is one of the most highly preferred algorithms for performing multiplication.
process goes on likewise. If there is more than one line in one step, all the results have added to the previous carry. In every step, slightest essential bit act as the result digit and all other digits act as carry for the next step. As compared to Array Multiplier and Wallace multiplier Proposed Vedic Multiplier is efficient in terms of delay and speed and power.

B. 4X4 VEDIC MULTIPLIER

The multiplication of 2x2, 4x4 and 8x8 Vedic Multiplier are generated using “Urdhav-Triyakbhyam” (Vertically and crosswise) sutra for Multiplying binary numbers. The general block diagram of 4x4 bit Vedic multiplier consists of four square shapes 2x2 bit Vedic multiplier first 2x2 bit Vedic multiplier has inputs as A1A0 and B1B0 and the middle block inputs are A3, A2 & B1B0 and A1A0 & B3 B2 and the final 2x2 bit Vedic multiplier inputs is A3 A2 and B3 B2. The output for the multiplication outcome will be of 8 bits (s7 s6 s5 s4 s3 s2 s1 s0). The 4x4 bit Vedic multiplier is consists of four 2x2 bit Vedic multipliers and two 4-bit Adders and one half adder and one 2-bit adder are required. “Ref. [5]”

\[
P = A \times B = (AH-AL) \times (BH-BL) = AH \times BH + (AH \times BL + AL \times BH) + AL \times BL
\]

Thus 8x8 bit Vedic multiplier unit can be easily formed by using four 4x4 bits Vedic multiplier modules and two 8-bit Adders and one half adder and one 4-bit adder. “Ref. [5-9]”

C. 8X8 VEDIC MULTIPLIER

The 4X4 Multiplier unit is the fundamental structure of 8X8 Vedic Multiplier. Analyzing 8X8 multiplications, inputs are a7-a0 and b7-b0 and the multiplication’s 16 bit output will be s15-s0. Let’s split A and B into two sections, say the 8 bit multiplicand A can be formed into a pair of 4 bits AH-AL. Likewise multipicand B can be formed into BH-BL. The 16 bit product can be written as

\[
P = A \times B = (AH-AL) \times (BH-BL) = AH \times BH + (AH \times BL + AL \times BH) + AL \times BL
\]

VI. MTCMOS TECHNIQUE

Power consumption is a major concern in the VLSI circuit design, high power consumption leads to reduction in battery life like movable phones, laptops etc. and affects the reliability of the system. To employ long standby periods by dropping the leakage current is highly significant to provide longevity for the succession. The extremely suggested circuit technique for the outflow current decline is the Multi-Threshold Voltage CMOS (MTCMOS). In MTCMOS technology, capable power managing is obtained by allowing the circuit to function in two modes: 1) energetic Mode 2) Sleep Mode. The power gating technique is one kind of multi-threshold voltage CMOS (MTCMOS) technique where a sleep transistor is added between control supply and ground it turns off the plans by cutting off their supply voltage. This method uses further transistors (sleep), which are inserted in the chain between the power supply and pull-up network (PMOS) and/or between pull-down (NMOS) network and ground to cut the standby leakage currents. The sleep transistors are turned on when the circuit are in energetic mode and turned off when circuits are in standby mode. “Ref. [17-20]”
VII.COMPARISON AND SIMULATION RESULTS.

Implementation of 4x4 as well as 8x8 bit three different types of multipliers using MOSFET, CNFET, and using MTCMOS technique using 32nm the Berkeley Predictive Technology Model (BPTM) has been carried out on H-spice tool. Power consumption and Power Delay Product (PDP) comparisons for 4x4 as well as 8x8 bit for three different types of multipliers i.e. Array multiplier, Wallace multiplier, Vedic multipliers are stimulated at 1v voltage. Here the comparison of multipliers is made between MOSFET AND CNFET 32nm technologies. “Ref. [21-22]”

TABULATIONS:

Table 1. Analysis of 4x4 multipliers cell between MOSFET 32nm and CNTFET 32nm technology

<table>
<thead>
<tr>
<th>4x4 multipliers</th>
<th>MOSFET 32nm Power delay product (w/s)</th>
<th>CNTFET 32nm Power delay product (w/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array multiplier</td>
<td>2.7784 E-15</td>
<td>6.9754 E-18</td>
</tr>
<tr>
<td>Wallace multiplier</td>
<td>1.0828 E-15</td>
<td>2.7769 E-18</td>
</tr>
<tr>
<td>Vedic multiplier</td>
<td>5.6090 E-16</td>
<td>1.6694 E-18</td>
</tr>
</tbody>
</table>

Table 2. Analysis of 8x8 multipliers cell between MOSFET 32nm and CNTFET 32nm technology

<table>
<thead>
<tr>
<th>8x8 multipliers</th>
<th>MOSFET 32nm Power delay product (w/s)</th>
<th>CNTFET 32nm Power delay product (w/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array multiplier</td>
<td>1.4363 E-13</td>
<td>5.7745 E-15</td>
</tr>
<tr>
<td>Wallace multiplier</td>
<td>1.6161 E-14</td>
<td>3.5517 E-17</td>
</tr>
<tr>
<td>Vedic multiplier</td>
<td>4.8615 E-15</td>
<td>1.2926 E-17</td>
</tr>
</tbody>
</table>

Table 3. Analysis of 4X4 multipliers cell between MOSFET 32nm technology and MOSFET 32nm with MTCMOS technique

<table>
<thead>
<tr>
<th>4x4 multiplier</th>
<th>MOSFET 32nm Power consumption (µw)</th>
<th>MOSFET32nm With MTCMOS technique power consumption (µw)</th>
<th>Power Gain in percentage%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array multiplier</td>
<td>6.0053 E-06</td>
<td>3.6129 E-06</td>
<td>39.83%</td>
</tr>
<tr>
<td>Wallace multiplier</td>
<td>4.3040 E-06</td>
<td>2.7137 E-06</td>
<td>36.94%</td>
</tr>
<tr>
<td>Vedic multiplier</td>
<td>3.6134 E-06</td>
<td>2.3856 E-06</td>
<td>33.97%</td>
</tr>
</tbody>
</table>

Table 4. Analysis of 8X8 multipliers cell between MOSFET 32nm technology and MOSFET 32nm with MTCMOS technique

<table>
<thead>
<tr>
<th>8x8 multiplier</th>
<th>MOSFET 32nm Power consumption (µw)</th>
<th>MOSFET32nm With MTCMOS technique power consumption (µw)</th>
<th>Power Gain in percentage%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array multiplier</td>
<td>3.4611 E-05</td>
<td>1.9663 E-05</td>
<td>43.18%</td>
</tr>
<tr>
<td>Wallace multiplier</td>
<td>3.2522 E-05</td>
<td>1.8670 E-05</td>
<td>42.59%</td>
</tr>
<tr>
<td>Vedic multiplier</td>
<td>2.0419 E-05</td>
<td>1.2909 E-05</td>
<td>36.77%</td>
</tr>
</tbody>
</table>
Table 5. Analysis of 4X4 multipliers cell between CNFET 32nm technology and CNFET 32nm with MTCMOS technique

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>4X4 multiplier</th>
<th>32nm Power consumption (µw)</th>
<th>With MTCMOS technique power consumption (µw)</th>
<th>Power Gain in percentage%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array</td>
<td>4X4 multiplier</td>
<td>2.9532 E-07</td>
<td>1.6873 E-07</td>
<td>42.86%</td>
</tr>
<tr>
<td>Wallace</td>
<td>8X8 multiplier</td>
<td>2.1006 E-07</td>
<td>1.2355 E-07</td>
<td>41.18%</td>
</tr>
<tr>
<td>Vedic</td>
<td>Vedic multiplier</td>
<td>1.7996 E-07</td>
<td>1.0693 E-07</td>
<td>40.58%</td>
</tr>
</tbody>
</table>

Table 6. Analysis of 8X8 multipliers cell between CNFET 32nm technology and CNFET 32nm with MTCMOS technique

<table>
<thead>
<tr>
<th>Multiplier</th>
<th>8X8 multiplier</th>
<th>32nm Power consumption (µw)</th>
<th>With MTCMOS technique power consumption (µw)</th>
<th>Power Gain in percentage%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array</td>
<td>8X8 multiplier</td>
<td>1.5618 E-06</td>
<td>8.4861 E-07</td>
<td>45.66%</td>
</tr>
<tr>
<td>Wallace</td>
<td>8X8 multiplier</td>
<td>1.4428 E-06</td>
<td>8.3770 E-07</td>
<td>41.93%</td>
</tr>
<tr>
<td>Vedic</td>
<td>Vedic multiplier</td>
<td>9.2553 E-07</td>
<td>5.5156 E-07</td>
<td>40.40%</td>
</tr>
</tbody>
</table>

SIMULATIONS OUTPUTS:

The multipliers are analyzed in terms of power, propagation delay and power delay product in both 32nm MOSFET technology and 32nm CNFET technology with an operating voltage of 1v using H-spice to provide parametric performance in variances which present accurate result. Here all the 4x4 multipliers as well as 8x8 multipliers are simulated and binary values are provided in different combinations. To make comparisons between different multipliers a common input was given to all the multipliers to get the accurate result and the output waveform will also be same for all the multipliers.
V(a0),v(a1),v(a2),v(a3),v(b0),v(b1)v(b2),v(b3) are the inputs and v(s0), v(s1), v(s2),v(s3),v(s4),v(s5),v(s6),v(s7) outputs of all 8x8 multipliers with MTMOS technique.

"Fig.15," transient analysis of 8x8 multipliers with MTMOS technique

V(a0),v(a1),v(a2),v(a3),v(a4),v(a5),v(a6),v(a7),v(b0),v(b1)v(b2),v(b3),v(b4),v(b5),v(b6) V(b7) are the inputs and v(s0), v(s1), v(s2), v(s3), v(s4), v(s5), v(s6), v(s7)v(s8), v(s9), v(s10), v(s11), v(s12), v(s13),v(s14),v(s15) outputs of all 8x8 multipliers with MTMOS technique.

VIII. CONCLUSION.

In the VLSI design the power and delay are great concerns while designing a multiplier. Here the three different types of multipliers are simulated and compared using 32nm Berkeley Predictive Technology Model (BPTM) between MOSFET 32nm and CNFET 32nm technology. Designing a multiplier using CNFET reduces 99% of power compared to MOSFET. Among all the three different multipliers the Vedic multiplier proves to be the best compared with the array and Wallace multiplier. Still in order to reduce the power consumption the low power technique using MTMOS technique is applied to all the multiplier it proves to be more efficient in terms of power reduction and it nearly reduces 50% of power compares to normal multipliers (i.e. Without applying technique). It is concluded that Vedic multiplier are best compared to all the multipliers and the CNFET technologies are very promising for realizing robust circuits such as multipliers in future scaled technology.

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