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Design and Performance Analysis of Low Power Comparators for High Speed ADC

M. Damodhar Rao
Associate Professor
Department of Electronics and Communication Engineering
Seshadri Rao Gudlavalleru Engineering College,
Gudlavalleru, Andhra Pradesh, India

N. Harika, P. Naga Vijaya Durga,
M. Siva Sai Kumar, M. Jayinya
UG Students,
Department of Electronics and Communication Engineering
Seshadri Rao Gudlavalleru Engineering College,
Gudlavalleru, Andhra Pradesh, India

***Abstract* - This project presents the design and performance analysis of a low power, high speed comparator for use in ADCs. The comparator is a crucial building block in ADC, directly impacting the converter's overall speed and accuracy. The design utilizes a two-stage architecture: a pre-amplifier stage for high gain and reduced kickback noise, followed by a regenerative latch for rapid signal amplification and decision making. The project explores various design techniques, including dynamic biasing and offset cancellation, to improve performance. The results demonstrate a significant reduction in power consumption and propagation delay compared to conventional designs, making it suitable for high-speed, low power ADC applications.**

Keywords - Dynamic comparator, preamplifier, high speed, latch, low power, ADC

I. INTRODUCTION

Comparators are really important in analog and mixed-signal circuits. They play a role in analog-to-digital converters, data acquisition systems and high-speed communication circuits. The performance of a comparator affects how fast and power efficient these systems are. Traditional static comparators are simple and robust but have some big problems: they use a lot of power when they are not doing anything and they are slow. They can be affected by noise and offset.

Dynamic comparators are different. They only use power when they are comparing things, so they are faster and use less power. They have their own problems including input-referred offset, thermal noise and kickback effects, which can make them less accurate and reliable in applications that need high precision. To solve these problems people have started using dynamic comparators with asymmetric transistor paths. This helps the comparator make decisions faster and reduces kickback noise. It also minimizes input offset and thermal noise, making asymmetric dynamic comparators really good for high resolution and high-speed analog-to-digital converters.

The goal of this project is to design a dynamic comparator that balances speed, accuracy and power consumption. The comparator we designed is really good at keeping input-referred offset low, reducing noise, operating at high speeds and dealing with variations in the manufacturing process. This makes it perfect for applications that need to be low power, high speed and precise such as analog-to-digital converters and other high-speed circuits.

Dynamic Comparator:

A dynamic comparator is a type of voltage comparator that works in a time-controlled way, performing comparisons during a specific clock phase. Unlike static comparators, dynamic comparators do not consume a lot of power when they are not being used because they do not have a continuous current flow. Dynamic comparators have two phases: a precharge phase and an evaluation phase. In the precharge phase the internal nodes of the comparator are charged to a known voltage. Then in the evaluation phase the comparator quickly decides what the digital output should be based on the input voltage.

They are also better at dealing with noise, making them very useful for high speed and high-resolution applications. For example dynamic comparators are used in successive-approximation-register and flash analog-to-digital converters where fast, precise and low power operation is required. Modern analog-to-digital converters are used in different fields, including biomedical implants and portable electronics. As the demand for battery-powered devices continues to grow, it is becoming increasingly important to find ways to make these devices use less power. One way to do this is to use optimized comparator circuits.

Dynamic comparators use a latch mechanism to make decisions and need a clock or strobe signal to start the comparison. High-performance comparators usually have two stages: a

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preamplifier stage and a regenerative latch stage. The preamplifier makes the signal stronger and reduces noise. The latch then quickly amplifies the signal to produce a valid output. One of the challenges of dynamic comparators is kickback noise, which can corrupt the input signal and cause errors. To fix this problem some dynamic comparators use a double-stage architecture with a preamplifier that drives the latch input, reducing kickback noise and making the comparator more accurate.

II. LITERATURE SURVEY

The basics of comparators and how they can be improved with latch-based regeneration have been studied extensively. However prior work mainly focuses on understanding the architecture rather than finding ways to reduce the power used by the preamplifier stage. The design guidelines do not directly address how to optimize the power used by the internal nodes of dynamic comparators.

Chevella et al. [4] were able to make a low-power comparator by using a reduced supply voltage. Their technique mainly relies on reducing the voltage and optimizing the biasing, which can affect the noise margin and make the comparator more sensitive to variations in the manufacturing process. On the other hand, the proposed method reduces the power used by the preamplifier output without aggressively reducing the supply voltage, making it more robust in 90 nm CMOS.

Kobayashi et al. [5] focused on current-mode latch sensing and reducing the power used by the input buffer. Their approach does not directly reduce the dynamic power used by the preamplifier stage of the comparator. Moreover current-mode designs can be more complex and use more area than the proposed voltage-mode preamplifier optimization.

Razavi's StrongARM latch comparator [6] is very fast and uses no static power. However it has a lot of kickback noise and input-referred offset because it does not have a preamplifier stage. The proposed method specifically targets the preamplifier output swing to reduce power and also improves the isolation from latch-induced kickback.

Schinkel et al. [7] proposed a double-tail comparator to improve low-voltage operation and speed. Their design adds more internal nodes and clocked devices, which increases the dynamic power due to higher parasitic capacitances. The proposed method reduces power by minimizing the voltage swing at the preamplifier output rather than adding more clocked transistors.

Harpe et al. [10] and Bindra et al. [11] reported energy-efficient comparators using dynamic biasing and noise reduction techniques. However dynamic bias schemes often require control circuitry and careful timing calibration. The proposed method avoids bias control blocks and achieves power savings through structural modification of the preamplifier output swing.

Tang et al. [12] proposed a floating inverter based comparator that improves energy efficiency. Floating nodes are more prone to leakage and charge sharing in scaled technologies like 90 nm CMOS. The proposed method maintains node biasing while reducing dynamic switching power and improving reliability across different operating conditions.

III. EXISTING METHOD

Modified Dynamic Comparator Circuit Description:

The modified dynamic comparator employs a two-stage architecture consisting of a differential preamplifier followed by a latch-based comparator stage. The first stage, referred to as the preamplifier, is implemented as a source-grounded differential amplifier with an active load. Its primary function is to amplify the differential input signal and enhance the sensitivity of the comparator, enabling reliable detection of small input voltage differences. In addition, the preamplifier provides isolation between the input and the regenerative latch stage, thereby reducing kickback noise generated by the latch during regeneration. This isolation helps minimize input-referred offset voltage and improves overall comparison accuracy.

To further mitigate the kickback effect, additional intermediate circuitry is introduced between the preamplifier and the latch. Kickback noise arises due to large voltage swings at the latch regeneration nodes, which couple back to the input through parasitic gate-drain capacitances. The added circuitry limits this coupling and also creates a controlled charge imbalance in the latch during the transition from reset to evaluation mode, which accelerates the regeneration process.

The latch itself operates as a dynamic storage element that temporarily stores charge in the gate oxide capacitances of the inverter transistors. Through positive feedback, the latch rapidly amplifies the small differential voltage from the preamplifier and resolves the comparison. The output stage consists of the latch followed by a buffer inverter that converts the latch outputs into full-swing digital levels (logic '1' or logic '0'). The differential amplifier comprises two PMOS transistors (M3, M4) and two NMOS transistors (M1, M2), while the latch provides complementary outputs, out+ and out−.

The modified dynamic comparator architecture shown in Fig. 1 introduces eight additional transistors to the conventional dynamic comparator: four PMOS devices (M26, M27, M30, and M31) and four NMOS devices (M28, M29, M32, and M33).

During the reset phase, when the clock signal (clk) is high, the outputs of the differential amplifier are discharged and the latch outputs are precharged to VDD, thereby initializing the internal nodes. During the evaluation phase, when clk is low, the

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Vol. 15 Issue 04 , April - 2026

preamplifier outputs (P+ and P−) begin charging. The additional PMOS transistors connected to the input nodes (Vin1 and Vin2) assist in charging P+ and P−, enabling faster preamplifier output development.

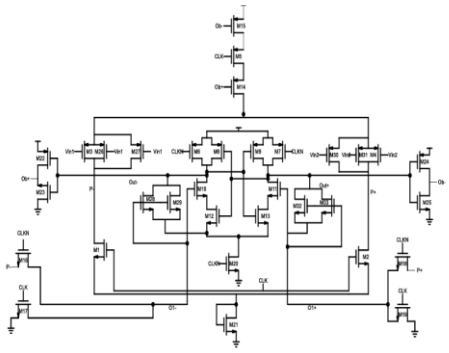

Fig. 1: Schematic of Modified Dynamic Comparator

To further control unnecessary internal charging, a multiplexer is inserted between the preamplifier outputs and the latch inputs. This multiplexer allows the latch to receive the preamplifier output only when the differential voltage exceeds the threshold voltage of the latch input transistors (M10 and M11). By doing so, excessive charging of the gate oxide capacitances of M10 and M11 is avoided, which contributes to reduced dynamic power consumption.

In the conventional dynamic comparator, the preamplifier output nodes continue to charge until the latch completes regeneration, leading to unnecessary dynamic power consumption. In contrast, the proposed modification accelerates latch regeneration, which in turn cuts off the supply to the preamplifier stage earlier. Consequently, the voltage swing at the preamplifier output nodes is reduced, and redundant charging is minimized. This early termination of preamplifier activity significantly lowers dynamic power dissipation while preserving high-speed operation.

IV. PROPOSED METHOD

The proposed optimized dynamic comparator architecture shown in Fig. 2 further enhances the power efficiency of the modified comparator by explicitly suppressing unnecessary switching activity at the preamplifier output nodes while preserving high-speed operation. Similar to the existing architecture, the comparator employs a two-stage structure consisting of a differential preamplifier followed by a regenerative latch. However, in the proposed method, the charging path of the preamplifier outputs (P+ and P−) is actively controlled such that once the latch begins regeneration, the supply to the preamplifier stage is effectively isolated.

This early cut-off mechanism prevents the preamplifier output nodes from charging to the full voltage swing, thereby reducing the dynamic energy consumed in charging and discharging the associated parasitic capacitances. As a result, redundant power dissipation that normally occurs after the latch has already resolved the comparison is significantly minimized.

In the proposed architecture, the latch regeneration is intentionally accelerated by optimizing the discharge paths and reducing the effective capacitance seen at the latch input nodes. This ensures that the latch reaches a valid logic level faster than in the existing modified comparator. Once the latch output begins transitioning, the preamplifier is disconnected from the supply through controlled gating transistors, effectively freezing the preamplifier output nodes at a lower voltage swing. This approach directly reduces the dominant dynamic power component, given by $P_{Eyn} = CV^2f$, by lowering the effective voltage swing at the internal nodes without compromising the sensitivity of the preamplifier during the initial comparison phase.

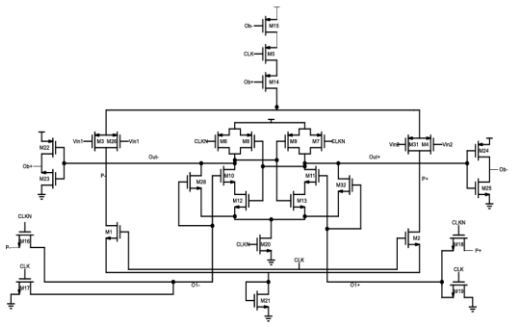

Fig. 2: Optimized Modified Dynamic Comparator

Furthermore, the proposed design carefully balances the power-speed trade-off by minimizing additional parasitic capacitances and avoiding excessive clocked devices. Unlike the existing modified comparator, which still allows near full-swing charging at the preamplifier outputs until latch resolution, the optimized architecture ensures that the preamplifier contributes energy only during the critical decision window. This selective activation not only improves energy efficiency but also reduces internal node stress and mitigates kickback noise coupling from the latch to the input. Consequently, the proposed comparator achieves lower dynamic power consumption, improved power-delay product, and robust high-speed performance, making it particularly suitable for low-power, high-speed ADC applications in 90 nm CMOS technology.

V. WORKING OF THE SYSTEM

The proposed system is designed and analyzed using Cadence Virtuoso, a widely used platform for CMOS circuit design and simulation. Initially, a new library is created and linked to the appropriate TSMC technology file to ensure accurate device modeling. The schematic is then developed by placing PMOS and NMOS transistors along with power sources such as VDD and GND from the NCSU Analog Parts library. All components

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are interconnected using wires, and input/output pins are assigned to define the circuit behavior.

Next, the circuit is simulated using the Spectre simulator in the Analog Design Environment (ADE L), where model libraries and input stimuli are configured. Transient analysis is performed to observe the time-domain response, allowing measurement of important parameters such as rise time, fall time, and propagation delay. DC analysis is also carried out by sweeping the input voltage from 0 V to 1.5 V to obtain the Voltage Transfer Characteristics (VTC).

Hardware Requirements:

• **Computer System –** Used to run design and simulation tools efficiently.

• **Minimum 4 GB RAM (8 GB recommended) –** Ensures smooth execution of Cadence simulations without lag.

• **Intel i3 / Equivalent Processor –** Provides the necessary processing power for circuit design tasks.

• **50 GB Free Disk Space –** Required to store libraries, design files, and simulation results.

• **Display Monitor –** Used to view schematics, waveforms, and simulation outputs.

Software Requirements:

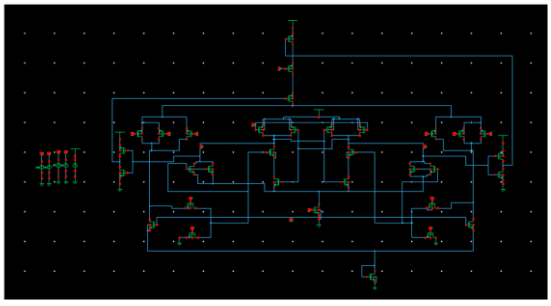
• **Virtuoso –** Used for designing schematics, layouts, and performing simulations.

• **Spectre Simulator –** Performs accurate analog circuit simulations like transient and DC analysis.

• **TSMC Technology File –** Provides device models and parameters required for realistic circuit behavior.

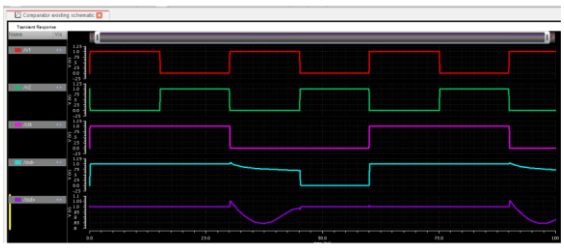
• **Linux/Unix Operating System –** Offers a stable environment for running Cadence design tools.

VI. RESULTS



Schematic of Existing method

Fig. 3: Schematic of Existing Method



Waveform of Existing method

Fig. 4: Waveform of Existing Method

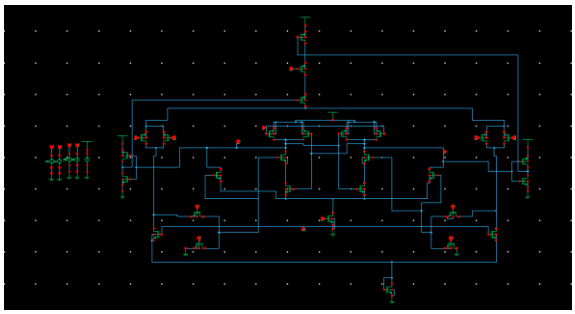


Fig. 5: Schematic of Proposed Method

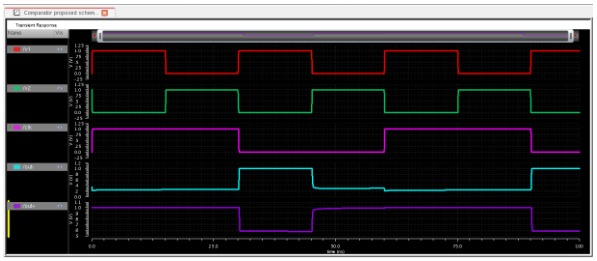


Fig. 6: Waveform of Proposed Method

Table I: Area, Delay and Power Results

	MOS Count	Delay (s)	Power (µW)
Existing	33	44.93n	3.168
Proposed	29	30.69p	2.936

VII. DISCUSSION AND FUTURE SCOPE

The dynamic comparator designed in this project focuses on reducing power consumption and improving speed. However, there are several areas where further improvements can be made in the future.

In future work, the comparator design can be implemented using lower technology nodes such as 45 nm or 28 nm CMOS technology to further reduce power consumption and increase speed. The circuit can also be optimized to reduce kickback noise and input offset voltage, which affect the accuracy of the comparator.

The proposed comparator can be integrated into a complete Analog-to-Digital Converter (ADC) system such as a Flash ADC or Successive Approximation Register (SAR) ADC to evaluate its performance in real-time applications. Layout design and physical verification can also be performed to analyze area, parasitic effects, and real-time performance.

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In addition, advanced techniques such as offset calibration, noise reduction techniques, and power gating methods can be implemented to further improve comparator performance. The comparator can also be designed for ultra-low voltage operation for battery-powered and portable electronic applications.

VIII. CONCLUSION

In this work, the conventional dynamic comparator and the modified dynamic comparator were presented and evaluated through detailed simulations and waveform analysis. By comparing the differential amplifier outputs of both architectures, it is observed that the modified dynamic comparator exhibits significantly lower dynamic power consumption. The proposed approach enables substantial energy savings during real-time operation without compromising the fundamental dynamic behavior and speed of the comparator. The simulation results clearly demonstrate the effectiveness of the proposed modification in reducing unnecessary switching activity and power dissipation.

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