

Design and Performance Analysis of Digital Integrator of a Multi-channel Microwave Radiometer

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Abstract

Integrate and dump filter in a microwave radiometer performs the function of extracting the radiometric signals in presence of additive white Gaussian noise. Such integrate and dump filter can be implemented using both analog and digital means. However, the digital implementation of this filter has numerous advantages over its analog counterpart, such as the ability to dump instantaneously without any overshoot, drift free operation at the quiescent point, and the use of latest high speed off-the-shelf digital integrated circuits to perform multiplication and accumulation with greater accuracy and repeatability. In this paper design details of digital integrator of a multi-channel microwave radiometer are given. Performance of the designed integrator is evaluated for different anti-aliasing low-pass filter bandwidths and optimum integration factors are determined to achieve best signal-to-noise ratio. Simulations of designed digital integrator are carried out for hardware implementation. Performance degradation effects associated with integrator parameters like quantization bits, pre-detection bandwidth, sampling rate, accumulator length are discussed.

Keywords-integrate and dump; digital integrator; microwave radiometer; signal-to-noise ratio; digital receiver

1. Introduction

A microwave radiometer, onboard a spacecraft, measures the energy of atmospheric and terrestrial radiations at sub-millimeter to centimeter wavelengths. By understanding the physical processes associated with energy emission at these wavelengths, scientists can calculate a variety of surface and atmospheric parameters from these measurements, including air temperature, sea surface temperature, salinity, soil moisture, sea ice, precipitation, the total amount of water vapor and the total amount of liquid water in the atmospheric column directly above or below the instrument. Development of ultra-high resolution microwave radiometers involves challenges like implementation of high bandwidth receiver section. Conventional analog microwave receivers consist of amplifiers, filters and down-

converters (IQ demodulators) to convert the analog signals to base-band. Conversion of these analog signals to digital samples is done at base-band by analog-to-digital (A/D) converters and further digital processing is done at lower frequency. This processing philosophy works well for a single or dual channel system where the number of analog channels or receivers is limited by the polarization or frequency of operation of the sensor. However, in the case of a multi-channel radiometer, where the number of receivers or analog channels is determined by the number of antenna elements, it is highly impractical to implement an analog receiver consisting of IQ demodulator for each channel (antenna element) owing to unmanageable mass, power and volume. The most elegant and viable option is the digital receiver. The generic block schematic of a digital receiver is shown in Fig.1[1].

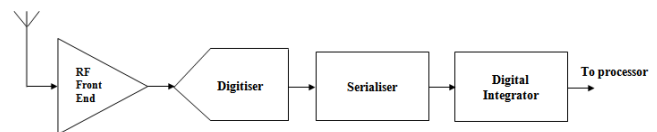


Figure 1. Block Schematic of a Digital Receiver.

The generic RF/IF digital receiver consists of a radio frequency (RF) Front-end consisting of cascaded low noise amplifiers (LNA's) to achieve high gain and a band pass filter (BPF), having bandwidth >50 MHz, centered at desired microwave frequency. The BPF is followed by an analog to digital converter with high vertical resolution. The ADC is a mixed signal ASIC with in-built serializers. The serialized data is digitally integrated over optimum number of samples using integrate and dump filter to improve the receiver SNR and the integrated data is sent to processor for further digital processing. Digital implementation of receiver offers advantages like programmability, accuracy, better stability, repeatability etc.

The digital implementation of integrate and dump filter requires the input signal to be sampled. To eliminate aliasing, the input signal is filtered using an anti-aliasing low pass pre-filter prior to sampling. This band limiting of input signal causes inter symbol

interference which degrades the performance of the receiver. In this paper, performance of an analog filter is compared with a digital filter with different bandwidths and optimum integration factors are determined to achieve best signal-to-noise ratio of the designed digital integrate and dump filter. Simulations are carried out to determine the frequency response of filters and select the optimum averaging factors for desired dwell time.

2. Design of integrator

Integrate and dump filter of a microwave radiometer can be designed using both analog and digital means. For a scanning radiometer, the dwell times (integration times) for the various channels are computed by taking into account the nominal values for the orbital height, scan rate, foot print size etc. The proposed integrator is designed for a three channel microwave radiometer having following integration times:

| | | |
|-------------|---|------|
| Channel - 1 | : | 8 ms |
| Channel - 2 | : | 2 ms |
| Channel - 3 | : | 1 ms |

A. Analog integrator

An analog integrator can be designed using an operational amplifier. Basic integrator circuit using an operational amplifier is shown in Fig.2 below and the corresponding equation of the circuit is given in (1).

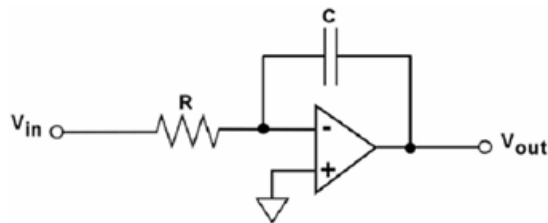


Figure 2. An Analog Integrator using Op-Amp.

$$V_{out}(t) = -\frac{1}{RC} \int V_{in}(t) dt \quad (1)$$

Simulations in MATLAB are carried out to determine the frequency response of above analog filter for different

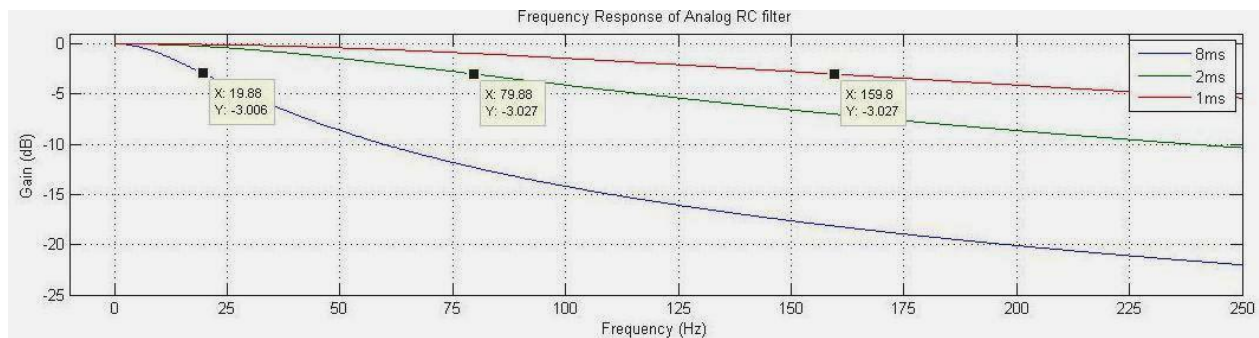


Figure 3. Frequency Response of Analog Integrator

channels of radiometer with 8ms, 2ms and 1ms integration times. Simulation results are shown in Fig.3 and tabulated in Table – 1 below.

Table 1. Analog Filter Frequency Response

| Channel | Integration Time / RC Filter Time Constant (ms) | -3dB Frequency (Hz) |
|---------|---|---------------------|
| 1 | 8 | 20 |
| 2 | 2 | 80 |
| 3 | 1 | 160 |

Even though the integrator circuit may be realized using above op-amp circuit, it has some inherent disadvantages.

Disadvantages of Analog Integrator:

- Offset Error: Op-amp gives some offset signal at its output even though there is no input signal. This offset creates error in the actual output of the op-amp when signal is present at its input.
- Leakage Current: All transistors / MOSFET devices have inherent leakage current. This leakage current tends to interfere with the actual output and corrupts the signal.
- Long Term Stability: Over a long period of operation offset and leakage current of an op-amp tends to change which causes variations in output.
- Temperature Drift: Temperature variations also cause variations in offset and leakage current of op-amp.

Due to these disadvantages an analog integrator is not preferable. Further an analog integrator is impractical for a multi-channel radiometer due to high power, mass and volume. A digital “equivalent” implementation offers some advantages over analog circuitry including the ability to be dumped in an extremely short time with no overshoot freedom from drift, and the use of digital ICs or a computer for processing[2].

B. Digital integrator

Integration in time domain is equivalent to a filter in frequency domain. The time domain equation of an analog integrator and its equivalent in frequency domain are shown (2):

$$V_{out}(t) = -\frac{1}{RC} \int V_{in}(t) dt \iff V_{out} = -\frac{V_{in}}{j\omega RC} \quad (2)$$

Time Domain Frequency Domain

The frequency domain equation represents a filter with following specifications:

- Magnitude: -20dB/decade
- Phase: 90° phase shift for all frequencies

This filter is easy to implement in a digital signal processor.

3. Determination of optimum averaging factors for digital integration

A. Sum and dump algorithm

The digital filter is designed primarily to provide the necessary dynamic loop behaviour for optimum control of the noise injection process. The concept used to reduce the variance of the data in the post loop processor is well known sample mean algorithm [3][4]. This process will hereafter be denoted as a “sum- and- dump” algorithm due to its close similarity to the integrated and dump circuit used in analog matched filter and estimation system. Indeed mathematically the behaviour of the sum and dump algorithm on a discrete time basis is virtually identical to the behaviour of the integrated and dump filter on a continuous time basis.

The steady state frequency response of a discrete time sum and dump filter, denoted as $H_N(f)$, is given in (3):

$$H_N(f) = \frac{\sin(N\omega T_o/2)}{N \sin(\omega T_o/2)} e^{-j(N-1)\omega T_o/2} \quad (3)$$

The equivalent one-sided noise bandwidth B_N can be expressed as

$$B_N = \int_0^{0.5 f_{os}} [H_N(f)]^2 df \quad (4)$$

where, $f_{os} = 1 / T_o$

Substituting $H_N(f)$ from (3), the value of this integral is

$$B_N = \frac{2^{-[\log_2 N+1]}}{T_o} \quad (5)$$

$$= \frac{1}{2NT_o} \quad (6)$$

Let $\tau = NT_o =$ total time interval for averaging. Substituting these values of τ in (6), the one sided equivalent noise bandwidth is:

$$B_N = \frac{1}{2\tau} \quad (7)$$

This result is exactly the same as for the continuous time integrate and dump filter with τ as the integration time. Thus, the sum and dump algorithm for a discrete time signal functions exactly the same as the integrate and dump filter for a continuous time signal provided that the summation interval in the discrete time case is equal to the integration interval in the continuous time case. This would imply optimum sampling at the Nyquist rate for the discrete time system.

B. Implementation of sum and dump algorithm

The digital implementation inherently requires that the input waveform be sampled and “folding” of the noise spectrum will greatly reduce the filter effectiveness unless a low-pass pre-filter is used to limit the input bandwidth.

The front-end receiver output in radiometer has a low pass filter with the following characteristics: 5 KHz cut off (-3 dB) and 20 dB / decade roll off. Block schematic of digital implementation of integrate and dump filter is shown in Fig.4.

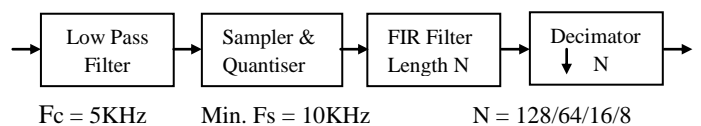


Figure 4. Digital implementation of Integrate and Dump Filter

The output of the low pass filter is first sampled, digitized and then integrated with a FIR digital filter. The output of this filter is appropriately down sampled (decimated) after the filtering operation depending on the integration time requirement of that particular channel.

C. Digital filter frequency response

This chain was simulated using MATLAB to arrive at optimum averaging factors for different channels of the radiometer. Simulation results are shown in Fig.5, 6 and 7 and tabulated in Table – 2, 3 and 4 below.

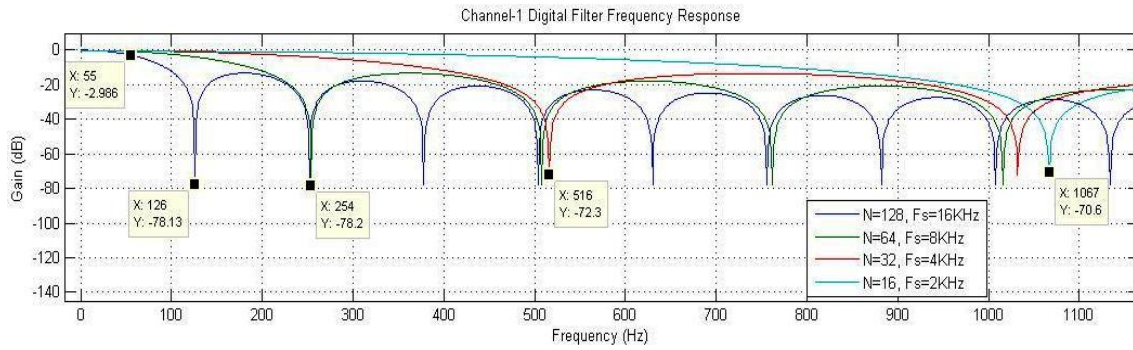


Figure 5. Channel-1 Digital Filter Frequency Response

Table 2. Channel-1 Digital Filter Frequency Response

| No. of samples integrated | Sampling rate (KHz) | Magnitude (dB) at 20Hz (equivalent to -3dB freq. of analog filter) | Freq. at -3dB (Hz) | Magnitude (dB) At lowest point |
|---------------------------|---------------------|--|--------------------|--------------------------------|
| 128 | 16 | -0.431 | 55 | -78.13 at 126Hz |
| 64 | 8 | -0.225 | 110 | -78.2 at 254 Hz |
| 32 | 4 | -0.297 | 219 | -72.3 at 516 Hz |
| 16 | 2 | -0.565 | 429 | -70.6 at 1067 Hz |

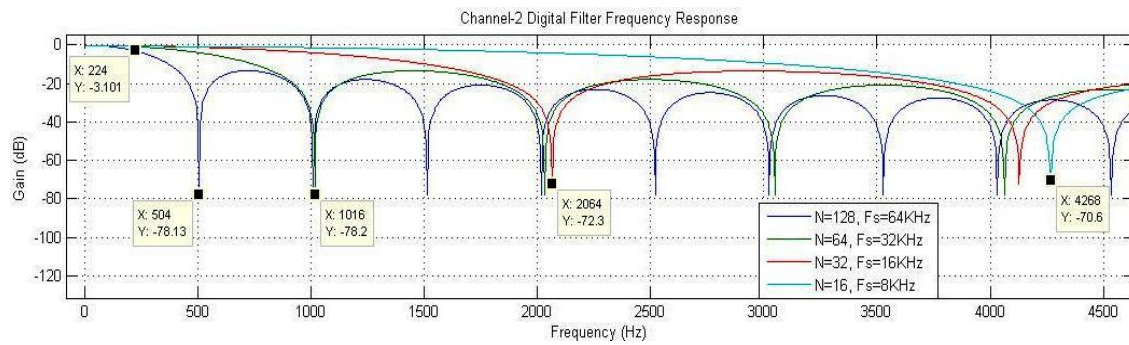


Figure 6. Channel-2 Digital Filter Frequency Response

Table 3. Channel-2 Digital Filter Frequency Response

| No. of samples integrated | Sampling rate (KHz) | Magnitude (dB) at 80Hz (equivalent to -3dB freq. of analog filter) | Freq. at -3dB (Hz) | Magnitude (dB) At lowest point |
|---------------------------|---------------------|--|--------------------|--------------------------------|
| 128 | 64 | -0.431 | 221 | -78.13 at 504Hz |
| 64 | 32 | -0.225 | 440 | -78.2 at 1016 Hz |
| 32 | 16 | -0.297 | 876 | -72.3 at 2064 Hz |
| 16 | 8 | -0.565 | 1716 | -70.6 at 4268 Hz |

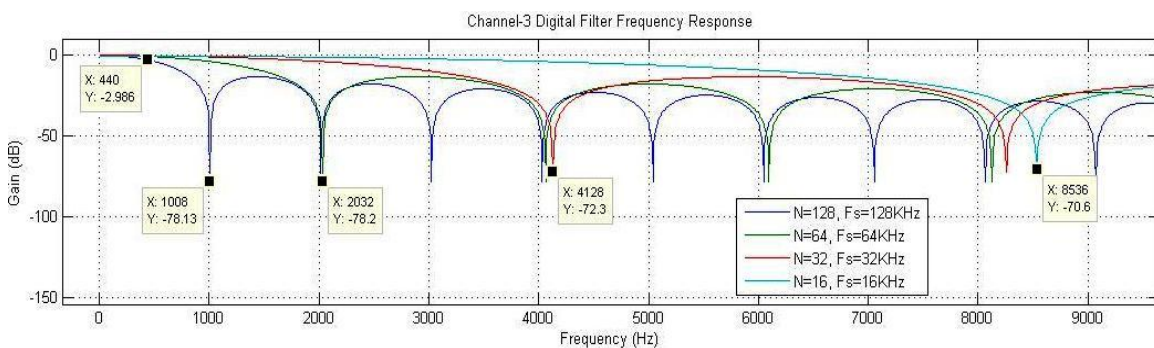


Figure 7. Channel-3 Digital Filter Frequency Response

Table 4. Channel-3 Digital Filter Frequency Response

| No. of samples integrated | Sampling rate (KHz) | Magnitude (dB) at 160Hz (equivalent to -3dB freq. of analog filter) | Freq. at -3dB (Hz) | Magnitude (dB) At lowest point |
|---------------------------|---------------------|---|--------------------|--------------------------------|
| 128 | 128 | -0.431 | 441 | -78.13 at 1008 Hz |
| 64 | 64 | -0.225 | 880 | -78.2 at 2032 Hz |
| 32 | 32 | -0.297 | 1752 | -72.3 at 4128 Hz |
| 16 | 16 | -0.565 | 3432 | -70.6 at 8536 Hz |

D. Comparison of analog and digital filter response

Comparing the performance of digital filters with analog filters in Tables – 1, 2, 3 and 4, it is observed that the performance of digital filters is better than analog filter. The -3dB frequency for each digital filter is much higher than the corresponding analog filter for the respective channels.

The bandwidth of the filter preceding the digital integrator is 5 KHz so according to Nyquist criterion the minimum sampling rate can be 10 KHz, therefore, the 2 KHz, 4 KHz and 8 KHz sampling rates cannot be used for channel-1. Similarly, 8 KHz sampling rate cannot be used for channel-2. For channel-3 all sampling rates are above the Nyquist sampling rate of 10 KHz and hence all can be used.

Hence, the minimum sampling rate for all the channels is 16 KHz and the optimum averaging factors corresponding to 16 KHz sampling rate for channel-1, channel-2 and channel-3 are 128, 32 and 16 respectively.

4. Hardware implementation of designed three channel digital integrator

The above designed three channel digital integrator is simulated in VHDL for hardware implementation using Xilinx Virtex XCV600 FPGA. Fig.8 below shows the basic building blocks for 3-channel digital integrator.

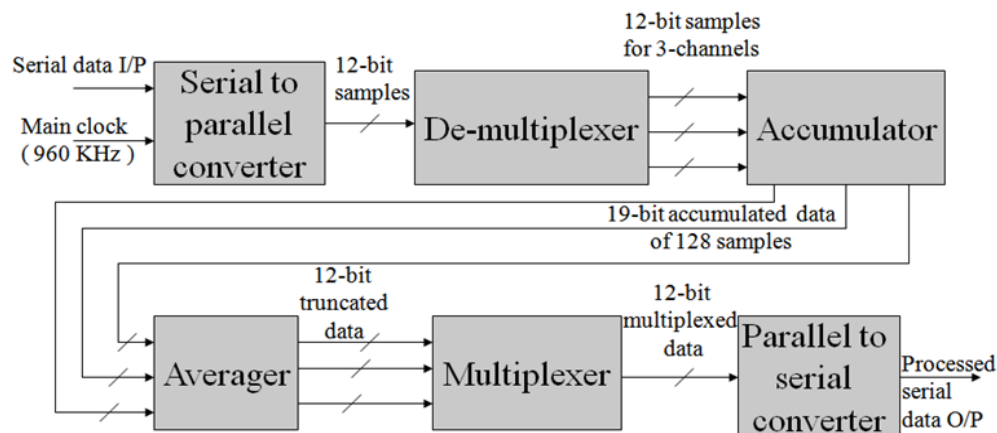
The video amplifier outputs of RF front end are

interfaced with the Sample and Hold Amplifier inputs to hold the signal during the conversion process.

The sampled video data is digitized using high precision, 12 bit resolution, successive approximation type Analog to Digital Converter (ADC). This 12 bit digitized data of each channel is converted to serial form by a parallel to serial converter and sent to the digital integrator module.

The digital integrator module, as shown above, consists of a serial to parallel converter, a de-multiplexer, a 12-bit accumulator/adder, an averager, 3-channel multiplexer and a parallel to serial converter. The averaging factor of 16, 32 and 128 are taken for integration of the channels 1, 2 and 3 respectively corresponding to sampling rate 16 KHz. For channel-1 where the averaging factor is 128 the basic block consists of a 19-bit adder and a 19-bit buffer. Initially the buffer is cleared and during each cycle the incoming 12-bit word and the previous accumulated output are added and after each summation the output is stored back in the same accumulator buffer. This cycle is repeated 128 times. After all the summation the output result is rounded to a 12-bit word. Truncating the 19 bit accumulated data into 12 bit word is achieved by discarding 7 LSBs. The 12-bit processed data is then serialized.

For the other requirements of averaging by 32 and 16, a similar approach is adopted. However for these two cases the length of the adder and the output buffer are chosen appropriately to ensure adequate growth of the intermediate results.

**Figure 8. 3-Channel Digital Integrator Block Schematic**

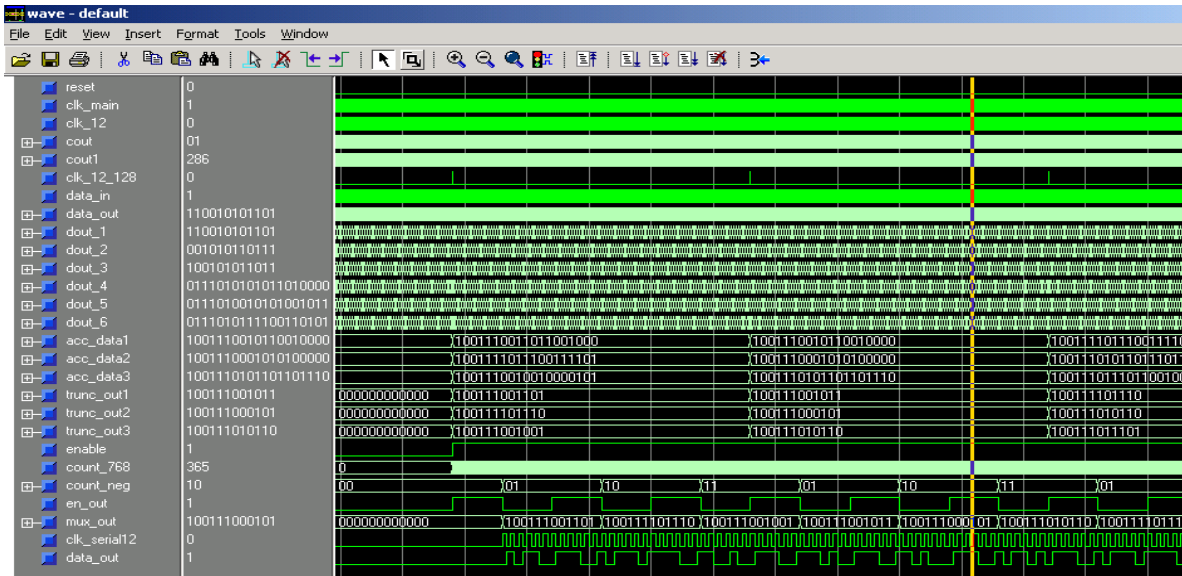


Figure 9. Digital Integrator VHDL Simulation Results

A. Simulation results

ISE text editor, schematics editor and constraints editor is used for VHDL programming of the integrator. ModelSim Simulator from Model Technology, Inc is used as simulation tool.

Screen shot of simulation results of above digital integrator for 128 samples is shown in Fig.9.

B. Synthesis report

Xilinx synthesis tool (XST) is used to synthesis above VHDL program for the digital integrator and implementation in Xilinx Virtex XCV600 FPGA. The synthesis report is shown in Fig.6 below. Synthesis report gives details of the FPGA resources used. Results show that only 3.2% of overall FPGA resources are utilized by above program. Hence, the VHDL code is optimised for most efficient utilization of FPGA resources.

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Device utilization summary:
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Selected Device : v600hq240-4

Number of Slices:           340 out of 6912   4%
Number of Slice Flip Flops:  375 out of 13824  2%
Number of 4 input LUTs:     391 out of 13824  2%
Number of bonded IOBs:      3 out of 170     1%
Number of GCLKs:            1 out of 4       25%
=====

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Figure 10. Synthesis Report for Xilinx Virtex XCV600 FPGA.

5. Conclusion

The digital integration and control module of a microwave radiometer carries out the functions of analog processing of the received video signals, digitization of the video signals and integrating the digitized video signals using digital domain approach. An analytical and simulation model of analog and digital integrators has been developed to compare their frequency response and to arrive at optimum averaging factors for the digital integration of different channels of a multi-channel radiometer. Simulation results showed that performance of digital integrator is much better than analog integrator over wide frequency band.

6. Acknowledgment

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7. References

- [1] MEGHA-TROPIQUES-MADRAS Payload Preliminary Design Review Document - March 2006
- [2] F. D. Natali, "Comparison of Analog and Digital Integrate-and-Dump Filters," Proc. IEEE, Vol. 157, pp. 1766 – 1768, October 1969
- [3] William D Stanley, "Preliminary Development of Digital Signal Processing in Microwave Radiometer". NASA Contractor Report – 3327
- [4] R. Sadr and W.G. Hurt, "Detection of Signals by the Digital Integrate-and-Dump Filter with Offset Sampling," TDA progress report 42-91, Vol. July – Sept 1987, Jet Propulsion Laboratory, California