Published by :
http://www.ijert.org
International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

Design and Performance Analysis of 18nm FINFET-based 8T SRAM

Vemula Panduranga,
Associate Professor, Dept. of ECE,
CMR College of Engineering & Technology,
Medchal, Hyderabad, Telangana, India.

Ogirala Pragnya Babu,
UG student, Dept. of ECE,
CMR College of Engineering & Technology,
Medchal, Hyderabad, Telangana, India.

***Abstract*— SRAMs are quicker and more dependable memories that are frequently utilized in digital processors for high-speed operation. The transistor count and the technology attached to the SRAM matters for designing and its performance analysis. In this paper the design analysis and the performance analysis like read - write and Hold operations are shown**

Keywords*— *SRAM, FINFET, read, write, leakage current, leakage power.

I. INTRODUCTION

Semiconductor memory units, which can store enormous amounts of digital data, are at the core of all digital gadgets. The amount of memory required for a specific system is determined by depending on the type of application Applications like because high-speed gaming needs a big quantity of memory to collaborate with electronic gadgets, are in high demand and are a need in today's world. Multimedia applications, such as mobile phones, PDAs, and laptop computers, require a huge number of memory accesses to function.

SRAM (Static Random Access Memory) is the quickest memory, but it is most costly and takes up a lot of processing space. SRAM of 256kb is comparable to 1Mb of DRAM. As process technology advances, more and more transistors are crammed into a single processing chip. This is helpful because, as device dimensions reduce, users may experiment with smaller size gadgets that have several functionalities. However, a growth in the number of transistors on the chip surface is also responsible in increase in power dissipation.

The current scenario shows that the number of transistors necessary for storing digital information is more than that required for performing logic operations. Growing desire for enormous amounts of data storage, Memory arrays have pushed manufacturing technology forward. Volatile memories and non-volatile memories are the two forms of memories. Volatile memories can only store data for as long as power is given to them, but non-volatile memories do not require constant power to preserve their data. The two types of memories are volatile memories and non-volatile memories. Non-volatile memories do not require continual power to keep their data, whereas volatile memories can only store data for as long as power is applied to them.

SRAM cell arrays are the quickest of all memory arrays, however, On the contrary, it is somewhat more expensive than any other unit. Semico Research, a market research firm, forecasts that by 2017, almost 70% of SoC die area will be occupied. Using SRAM As a result, in order to lower the power, Most researchers are concerned with dissipation and expense. concentrating on developing a low-power on-chip memory array. The random process has an impact on SRAM cell operation. This problem becomes apparent in Nano-scaled systems. As a result, technology degrades cell stability. Scaling process parameters such as supply voltage are reduced (VDD). The cell's stability suffers as its variability rises.

II. PROPOSED 8T SRAM CELL IN FINFET 18NM

Most widely used differential ended 8T SRAM cell requires more chip area compared to conventional 6T SRAM cell since it uses two separate ports for performing read and write operation. Differential ended dual bit lines allow for simultaneous access to 8T bit cell read and write ports, although this produces read disturbance since SRAM cell current reduces while read and writes. At low voltages single ended structure improves the stability of SRAM cell but gives poor noise immunity. Differential ended single port SRAM is more noise resistant than single ended type.

Fig1: Proposed 8T SRAM architecture

This cell consists of eight transistors, word line (WL), a bit line (BL) and a bit line bar(/BL). The transistors M1, M2, M3, M4 are combined to form a latch where the actual bit data is stored. M7& m* are the access transistors or

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 11 Issue 05, May-2022

pass transistors to which the bit and bit bar lines are connected. The transistors M5 &M6 are connected to the bit lines for fast accessing of SRAM cell.

Read, write and hold operations are performed in any SRAM cell. when the word line (WL) is high, then the access transistors get's ON and the Read and Write operations can be done; i.e reading the stored bit information and overwriting the desired bit into the SRAM cell is done by keeping the Word line (WL) high. If the word line is low then the SRAM cell is said to be I hold position, where there will be no change in the data of SRAM

A. *Read Operation*

The read operation is done on an SRAM cell to know or read the stored data bit in that particular cell.
To perform the read operation, the Bit line (BL) and Bit bar lines(/BL) are pre charged to vdd or vdd/2.The output of the read operation of the SRAM cell is taken from the sense amplifier. This sense amplifier acts as a comparator circuit and gives a one bit as an output. The values of the bit line (BL) and bit line bar(/BL) are compared by the sense amplifier and the out is read by the user. The sense amplifier output is given as 0 or 1, if bit line (BL) greater than bit line bar (/BL) then, the output is 1. Or if the bit line bar (/BL) greater than bit line (BL) the output is 0

So the read operation is done by comparing the voltage differences between the bit lines and Q, Q bar.
Consider the Q containing bit high i.e Q=1 and Q bar =0 and both the bit lines are pre charged i.e BL, BL/=1. Now there will be a voltage difference between the bit line bar and the Q bar, then the bit line bar(/BL) becomes zero, i.e (/BL=0) and there is no voltage difference between the bit line and Q, so bit line (BL=1).The values of the bit line (BL) and bit line bar(/BL) are compared by the sense amplifier and the out is read by the user. The sense amplifier output is given as 0 or 1, if bit line (BL) greater than bit line bar (/BL) then, the output is 1. Or if the bit line bar (/BL) greater than bit line (BL) the output is 0

Hence from the above considerations Q contain '1' and the output at the sense amplifier is also 1.so the data in the SRAM cell is read successfully.in this way the read operation is done

B. *Write Operation*

Write operation is performed to overwrite or change the data present in the SRAM cell.

The sources of transistors M5 & M6 from the architecture are connected to ground for the fast discharging of the bit lines in read operation.

The write operation is done by discharging the bit lines and the data to be stored in the SRAM cell is given through these bit lines. The data which is given through the bit lines pushes into the latch circuit where the data is present this data is overwritten with the input data through the bit line.
Consider the Q contain bit '0' and /Q containing bit '1' and the bit line the data to be written (BL=0) and the bit line bar (/BL=1). now the data from the bit line Is pushed into the latch to 'Q 'and the data from the bit line bar also pushed to the '/Q' this process is process is continued till the data at Q is changed. So new the data at q will be overwritten with the data at the bit line, so the data at Q =1 and /Q=0. Hence the write operation is done.

C. *Hold Operation*

The hold operation is used to store the data bits in the SRAM cell even the input power is in OFF condition. when the word line (WL) is '0' then the SRAM is said to be in Hold condition.
So that the data is not disturbed and there will be no loss in the
Stored data.

III. SIMULTION RESULTS & PERFORMANCE ANALYSIS

1.Read operation:
The simulation results of the SRAM read operation in through software is given below

Fig 2: read operation output

The above figure shows the simulation output for the read operation of proposed 8t SRAM cell.
It consists of word line, which is kept high. And '/net26' represents the Q; '/net 25' represents the Q bar and '/b' and '/b_' represents the bit and bit bar lines of the SRAM respectively

2.Write operation:
The simulation results of the SRAM write operation through cadence software is given below

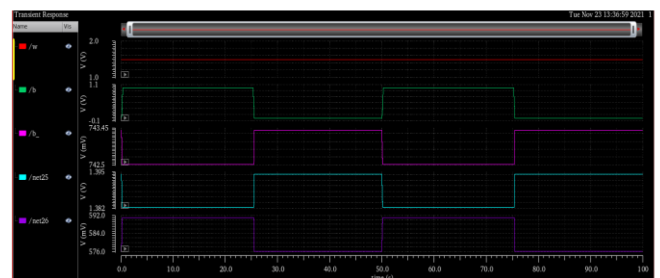

Fig 3 : write operation simulation output

The above figure shows the simulation output for the write operation of proposed 8t SRAM cell.
It consists of word line(/W), which is kept high. And '/net26' represents the Q ; '/net 25' represents the Q bar and '/b' and '/b_' represents the bit and bit bar lines of the SRAM respectively

(This work is licensed under a Creative Commons Attribution 4.0 International License.)

The performance of the SRAM is based on different parameters like speed, leakage power, read and write delays, power.

The below are the few parameters of the proposed 18nm - FINFET based 8t SRAM cell.

PARAMETERS	Proposed 8t SRAM cell
Dynamic power(W)	2.47e -3
Leakage power(W)	2.19e -5
Delay-read operation(ps)	19.61
Delay-write operation(ps)	20.17

Table 1: Parameters of proposed 8t SRAM cell

The above table represents the performance parameters of the proposed 8t SRAM cell, which include the dynamic power, leakage current or leakage power and read and write delays of the proposed SRAM cell.

The leakage power is defined as, the power consumed by the MOS transistors even when there is no power supply. This leakage power is reduced in the proposed 8t SRAM cell. The read and write delays are also reduced, and makes the SRAM cell faster compared to any other architecture or other technologies. Using the FINFET technology, the gate channel length of the transistors is small compared to other attached technologies.so due to this advantage the area occupied by the transistors will be less and hence the proposed 8t SRAM cell consumes lesser area.

Hence the above is the performance analysis of the proposed 8T SRAM cell.

IV. CONCLUSION

An 8T SRAM attached with the FINFET technology has been proposed. The proposed SRAM 8T cell has achieved improved read stability, write stability and leakage power and dynamic power. By using the N- metric curve we can conclude the above parameters and the performance analysis of the proposed 8T SRAM is done.

V. REFERENCES

[1] T. Karnik, T. De, and S. Borkar, “Statistical design for variation tolerance: key tocontinued Moore’s law,” in Proc. Int. Conf. Integrated Circuit Design andTechnology, 2004. pp. 175-176.

[2] J. W. Tschanz, et al., “Adaptive body bias for reducing impacts of die-to-die andwithin-die parameter variations on microprocessor frequency and leakage,” IEEEJ. Solid-State Circuits, vol. 37, no. 11, pp. 1396-1402, Nov. 2002.

[3] Sung-Mo Kang and Yusuf Leblebici “CMOS Digital IntegratedCircuits”,TATAMcGRAW-HILL EDITION 2003.

[4] Budhaditya Majumdar, Sumana Basu, “Low Power Single Bit line 6T SRAM Cell With High Read Stability”, IEEE 2011 International Conference on Recent Trends in Information Systems

[5] K. Khare, N. Khare, V. Kulhade and P. Deshpande, “VLSI Design And Analysis Of Low Power 6T SRAM Cell Using Cadence Tool”, leSE, lohorBahru, Malaysia, 2008.

[6] S. P. Cheng, S. Y. Huang "A Low-Power SRAM Design Using Quiet Bitline Architecture” Proc. of IEEE Int‟l Workshop on Memory Technology Design and Testing, 2005

[7] Andrei Pavlov, and Manoj Sachdev, “CMOS SARM Design and Parametric Test in NAno-Scaled Technology: Process-Aware SRAM Design and Test,” Springer, 2008.

[8] Irina Vazir, Prabhjot S. Balaggan, Sumandeep Kaur, and Cailan Shen, “SRAM IP for DSP/SOC Projects,” San Jose State University

[9] G. F. Cardinale, et al. "Demonstration of pattern transfer into sub-100 nm polysilicon line/space features patterned with extreme ultraviolet lithography." Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena 17.6 (1999): 2970-2974

[10] P. Raikwal, V. Neema, & A. Verma, (2017, April). ”High speed 8T SRAM cell design with improved read stability at 180nm technology”. In Electronics, Communication and Aerospace Technology (ICECA), 2017 International conference of (Vol. 2, pp. 563-568). IEEE

[11]] A. Islam, and M. Hasan. "A technique to mitigate impact of process, voltage and temperature variations on design metrics of SRAM Cell." Microelectronics Reliability 52.2 (2012): 405-411.

[12] C. Binjie, et al. "Impact of intrinsic parameter fluctuations in decanano MOSFETs on yield and functionality of SRAM cells." Solid-State Electronics 49.5 (2005): 740-746.

[13] S. Abhijit, S. Ghosh, and M. Bayoumi. "A novel 90nm 8T SRAM cell with enhanced stability." Integrated Circuit Design and Technology, 2007. ICICDT'07. IEEE International Conference on. IEEE, 2007.

(This work is licensed under a Creative Commons Attribution 4.0 International License.)