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Design and Layout of 1.8V Two Stage CMOS Operational Amplifier (Unbuffered)

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***Abstract*:- Operational amplifiers(Op-amp) are the most versatile and widely used component of electronicdevices. In this work design implementation and layout of a CMOS two stage op-amp has been presented which operates at 1.8 V power supply at 0.18µ (i.e., 180 nm) technology and whose input is dependent on Bias Current. Performance of any circuit depends upon speed, power and gain. This op-amp has very low standby power consumption with a high driving capability and operates at low voltage so that the circuit operates at low power. The op-amp provides a gain of 60dB and 20 V/µS slew rate for a 800fF compensation capacitor and 2 pF load Capacitor. The power dissipation for 1.8V supply voltage at 27°C temperature under other nominal conditions is 0.3mW. The Physical representation of the circuit known as layout isdesigned. The schematic is designed using Cadence virtuoso - schematic editor tool, layout is designed using Cadence virtuoso - layout editor tool and verification is done using Cadence virtuoso – Assure**

Keywords — CMOS, operational amplifier(Op-amp),gain, slew rate, layout

I. INTRODUCTION

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The op-amp is one of the most useful devices in analog electronic circuitry.An op-amp is a 3-terminal device and are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc[1] .Op-amps are built with different levelsof complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, andscientific devices.

The most commonly used configuration for CMOS operational amplifiers is the two stage amplifier. There is a differential front end which converts a differential voltage into a current and a common source output stage that converts the signal current into an output voltage. An important criterion of performance for these op amps in many applications is the settling time of the amplifier.

The aim of this work is to design and create a physical representation of low power Op-amp which can be fabricated. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down.

II. OPERATIONAL AMPLIFIER(OP-AMP)

Operational Amplifier(Op-amp) is a 3-terminal device. It has an Inverting input and Non-inverting input. Both these inputs are very high impedance. The output signal of an op-amp is the magnified difference between the two input signals[2]. Generally the input stage of an op-amp is often a differential amplifier. An op-amp is a DC-coupled differential input voltage amplifier with an rather high gain[3]. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an op-amp a negative feedback is used to control the large voltage gain. The negative feedback determines the magnitude of its output (”closed- loop”) voltage gain in numerous amplifier applications. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal Op-amp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp is one type of differential amplifier. This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. Andsince op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.

A basic op-amp consists of :

a. Differential Amplifier
b. Level shift, differential to single ended gain stage
c. Output buffer

In Fig 1. the first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain[4]. The second stage performs Level shifting, added gain and differential to single ended converter.

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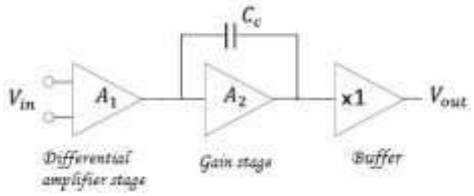

Fig 1. Block diagram of typical Operational amplifier (Op-amp)

The third block is the output buffer. The output buffer may sometimes be omitted to form a high output resistance unbuffered op-amp often referred to as Operational transconductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers). CMOS Operational Amplifier is one of the most versatile and important buildingblocks in analog circuit design[5]. Based upon the value of their output resistance they are being classified into two categories:

1. Unbuffered operational amplifier: These are Operational Transconductance Amplifiers (OTA), which have high output resistance.
2. Buffered Operational Amplifier: These are Voltage Operational Amplifiers, which have low output resistance.

Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer function is practically independent of the gain of the op-amp.The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement negative feedback concept[6]. An ideal op-amp having a single- ended output is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS technology design of op-amp continues to pose further challenges as the supply voltage and transistor channel length scale down.

The ideal op-amp: For any input voltages the ideal op- amp has infinite open-loop gain, infinite bandwidth, infinite input impedances (and hence zero input currents), zero output impedance, zero noise, and zero input offset voltage (exactly 0 V output when both inputs are equal). Real op-amps can only approximate to this ideal, and the actual parameters are subject to drift over time and with changes intemperature, input conditions, etc.

II. PROPOSED OPERATIONAL AMPLIFIER

Fig 2. shows the block diagram of an op-amp without output buffer. The output buffer may be omitted to form a high output resistance unbuffered op-amp often referred to asOperational transconductance amplifier or an OTA.

Differential amplifier with current-mirror supply (input stage) and common source amplifier with current supply (gain stage) by adding gain stage to differential amplifier forms an op-amp. Fig 3. shows CMOS Op-amp schematic.

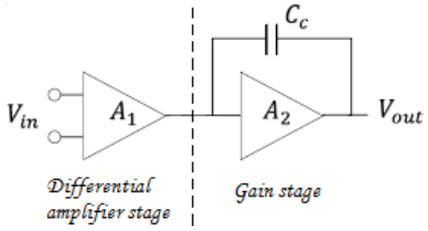

Fig 2. Block Diagram

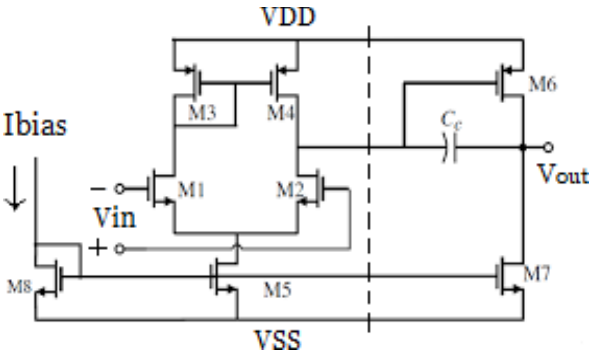

Fig 3. CMOS Op-amp design

The conception of the design has been accomplished by proposing an architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the necessary choices that must be made. Second step is to take the first-cut design and verify and optimize it. Simulations are done using Cadence virtuoso Spectre simulation tool.

Table 1. Specification of Op-amp

Specification	**Values**
Technology	180nm
VDD	1.8V
Av	>= 1000 (20log 1000 = 60dB)
CL	2pF
ICMR (max)	1.6V
ICMR (min)	0.8V
Slew rate	20V/µW
Phase Margin	>= 60º
Power dissipation	< 0.3mW
Gain bandwidth product	>= 5MHz

This design procedure assumes that the gain at dc (Av), unity gain bandwidth (GB), input common mode range (Vin(min) and Vin(max)), load capacitance (CL), slew rate (SR), settling time (Ts), output voltage swing (Vout(max) and Vout(min)), and power dissipation (Pdiss) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors. Check for transistors in saturation mode.

1. Determine the current at the input stage
   I0 =SR .Cc
2. Design for M3 and M4 from the maximum input

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$$i_D = K(W/L)(V_{gs} - V_t)2/2$$

Device parameters

Kn = (μnCox/2) = 300 μA/V2

Kp = (μpCox/2) = 60 μA/V

3. Design for M1 and M2 from gain bandwidth product Find gm by Gain bandwidth formula

   GB = dc gain * pole1= gm/ CL

   gm= GB* CL

$$i_D = K(W/L)(V_{gs} - V_t)2/2$$

$$gm2 = 2i_DK(W/L)$$

4. From the desired phase margin, have to choose the minimum value for Cc, i.e. for a 60degree phase margin we use the following relationship. This assumes that

$$z \geq 10GB\ Cc \geq 0.22CL$$

5. Determine the minimum value for the tail current

$$I5 = SR \cdot Cc$$

6. Design for M5 from the minimum input voltage. First calculate VDS5 (sat) then find M5, where M is defined as W/L ratio.

$$S5 = 2I5/\ K5[VDS5(SAT)]2$$

7. Have to find M6 by letting the second pole (p2) be equal to 2.2 times GB and assuming that

$$VSG4 = VSG6.$$

   If VSG4 = VSG6, then

$$I6 = (\ M6\ |M4)I4$$

8. For balance, I6 must equal I7
9. First stage gain Av1= gm1 / (gds1 + gds4)
10. Second Stage gain Av2 = gm6/ (gds6 + gds7)
11. Power Dissipation

$$Pdiss = (I5 + I6) * (Vdd + Vss)$$

Table 2. Calculated values

Current	**Values (μA)**
I0	50
I5	20
I6, I7	125
Transistor	**W/L (μm)**
M1/ M2	6/0.18
M3/M4	14/0.18
M5	12/0.18
M6	174/0.18
M7	75/0.18
M8	9/0.18

B. Layout

The Layout is the Physical representation of the circuit[7]. It contains Geometries that include n-well, active, polysilicon, implant, contacts, metal etc. These geometric shapes are known as layers. Each Geometry layer has rules to be followed given by fabrication unit. To start with layout we need to have schematic design, technology information and design constraints. Layout has following steps : Floorplan, placement, routing, verification and post layout simulation.

Floorplan - Creating sketch of layout, showing the locations and shapes of all the cells. It includes estimated area, Pin positions, Critical signals Like clock, reference signals, Special routing requirements like shielding, Power plan. Fig 8. shows the floorplan of the proposed op-amp design. It occupies 1140.48um of area, this area is estimated by considering number of MOSFET's, width and length and routing space.

Placement –Fig 9. shows placement of the proposed op-amp design. MOSFET's are placed as per the floorplan and verification is done to check the base level design rules are followed as per the fabrication unit.

Routing – Fig 10. Shows the routing of the proposed op-amp design. Metal orientation is as follows

Odd metals – Horizontal direction

Even metals – Vertical direction

Verification – Verifying all the blocks with respect to schematic and provided design rules by fabrication unit. Verifications like DRC – Design rule check and LVS – Layout v/s schematic are done for the proposed op-amp design.

Post layout simulation – It gives extracted view of the layout and includes extra parasitic added to the layout which should be in specified range as per the specifications.

III. RESULTS AND ANALYSIS

A. Gain calculation

1st stage:

$$Gain = gm1(ro1 \| ro4)$$

$$= gm/ (gds1+gds4)$$

$$=143/ 2.17+0.912$$

Gain = 46.39

Gain in dB = 20log 46.39 = 33.33dB

2nd stage:

$$Gain = gm6(ro6 \| ro7\ )$$

$$=gm6/ (gds6+gds7)$$

$$=1467/(7.475+43.02)$$

Gain =29.05

Gain in dB = 20log 29.05 =29.26dB

Total gain = 33.33+29.26 = 62.26dB

B. Power dissipation

The power dissipation of this op-amp is theoretically calculated.

Power dissipation(Pdiss) = Vdd * (sum of currents)

$$= 1.8 * (125+20)$$

$$= 261\mu\ W$$

$$=0.26mW$$

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Practically the power dissipation is 0.27mW.

Parameters considered to calculate in tool are

Vdd = 1.8 V

Vpulse = 0 to 1.8 V

pulse width=5us

period = 10us.

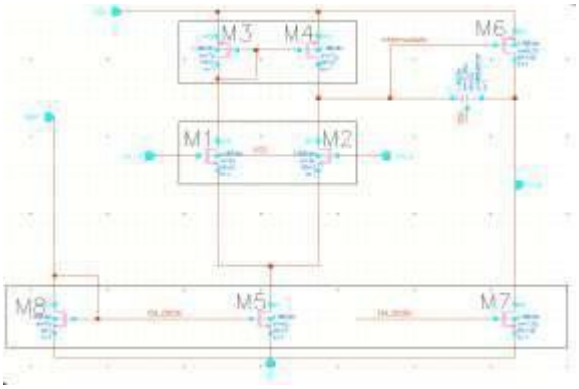

Fig 4. Schematic of an Op-amp

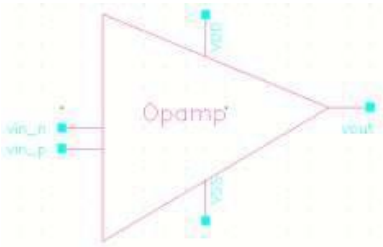

Fig 5. Symbol of an Op-amp

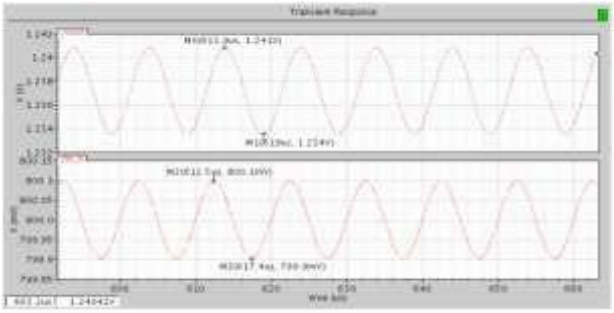

Fig 6. Transient analysis of an OPAMP

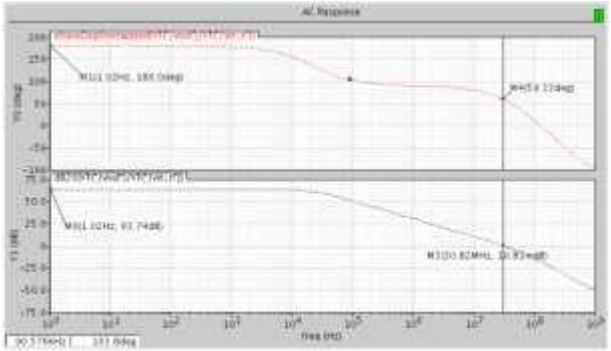

Fig 7. AC analysis of an Op-amp

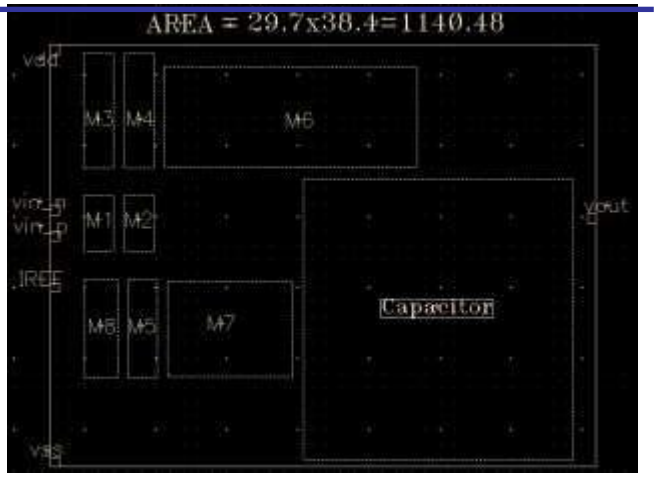

Fig 8. Floorplan of the Op-amp

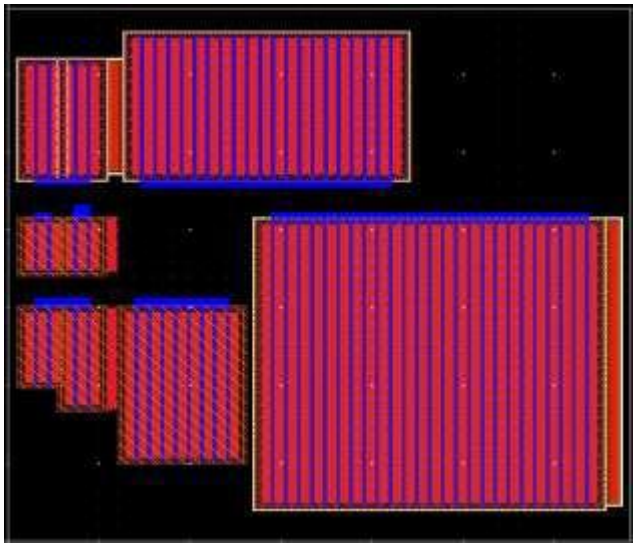

Fig 9. Placement of the Op-amp

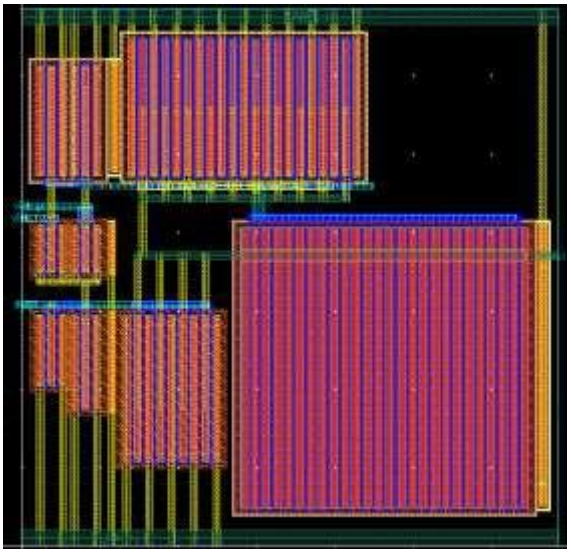

Fig 10. Routing of the Op-amp

IV. Conclusion

This work has been achieved its objective to design and layout of a CMOS two stage operational amplifier(op-amp) which operates at 1.8 V power supply at 0.18 µ (i.e., 180 nm) technology. This op-amp has very low standby

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power consumption with a high driving capability and operates at low voltage and the area occupied by the layout is 1140.48um. Future scope would be conducting post layout simulation of the design and finding out the parasitics added to design and reducing the same as per the specification.

V. REFERENCES

[1] Behzad Razavi, " Design of Analog CMOS IntegratedCircuits ", Fifth Edition,TMH Edition.

[2] Sayan Bandyopadhyay , Deep Mukherjee , Rajdeep Chatterjee "Design Of Two Stage CMOS Operational Amplifier in 180nm Technology With Low Power and High CMRR" Int. J. of Recent Trends in Engineering &Technology, Vol. 11, June 2014

[3] Tong Yuan, Qingyuan Fan ID "Design Of Two Stage CMOS Operational Amplifier in 180nm Technology"arXiv:2012.15737v1 [physics.ins-det] 27 Dec 2020

[4] Anjali Sharma , Payal Jangra , Sonu Kumar, Rekha Yadav "Design and Implementation of Two Stage CMOS Operational Amplifier" International Research Journal of Engineering and Technology (IRJET) e-ISSN:2395 -0056 Volume: 04 Issue: 06 | June -2017 www.irjet.net p-ISSN: 2395-0072

[5] Anchal Verma, Deepak Sharma, Rajesh Kumar Singh, Mukul Kumar Yadav "Design of Two-Stage CMOS Operational Amplifier" International Journal of Emerging Technology and Advanced Engineering, IISN2250-259, ISO 9001:2008 Certified Journal, Volume 3,Issue 12, December 2013

[6] David A. Johns and Ken Martin, " Analog Integrated Circuits Design", John Wiley and Sons.

[7] Kanika Sharma, Rahil Kumar" Design of a Two Stage CMOS Operational Amplifier using 180nm and 90nm Technology" International Journal of Advanced Researchin Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization) Vol. 5, Issue 5, May 2016,DOI:10.15662/IJAREEIE.2016.0505026