Design and Investigation of Power Reduction in D-Flip-Flop

S. Nivedha
PG Scholar
M.E VLSI Design
TRP Engineering College (SRM GROUP),
Tiruchirappalli – 621 105, India

S. Seramannan
Assistant Professor
Department of Electronics and Communication Engineering
TRP Engineering College (SRM GROUP),
Tiruchirappalli – 621 105, India

***Abstract*- The proposed system describes the power reduction in flip-flop. The system uses a technique called Topological-compression technique. A low-power flip-flop named topologically-compressed flip-flop (TCFF) is proposed. The power reduction is achieved by merging the logically equivalent transistors. This reduces the number of transistors in the flip-flop. The transistor which is connected to the clock signal consumes more power. In this method very small number of transistors, only three transistors are connected to clock signal which reduces the power drastically, and the smaller total transistor count assures the same cell area as conventional flip-flops. In the proposed flip-flop only three transistors are connected to the clock signal. The flip-flop circuit does not consume any power when the data input of the flip-flop does not change its state. This flip-flop can reduce 75% of the total power consumption in case of 0% switching activity. The simulation has been carried out using Microwind tool.**

Key words—Flip-flops, low-power.

I. INTRODUCTION

The mobile market keeps on expanding. In addition to the conventional mobile phone, digital camera, and tablet PC, development of various kinds of wearable information equipment or healthcare associated equipment has newly prospered in recent years. Today's technologies make possible powerful computing devices with multi-media capabilities. Consumer's attitudes are gearing towards better accessibility and mobility. Their desire has caused a demand for an ever-increasing number of portable applications requiring low-power and high throughput. For example, notebook and handheld computers are now made with competitive computational capabilities as those found in desktop machines. It is important that these high computational capabilities are placed in a low-power, portable environment. The weight and size of these portable devices is determined by the amount of power required. The battery lifetime for such products is crucial , hence, a well planned low-energy design strategy must be in place. In order to meet the demand in high computational applications, the clock rate is steadily increasing, with clock jitter and clock skew being an increasingly significant part of the clock cycle.

The energy consumed by low-skew clock distribution networks is perpetually growing. Clock-related power consumption can reach more than 30-40% of the total power of microprocessor and is becoming a larger fraction of the chip power. In addition, the number of logic gate delays in a clock period is reduced by 25% per generation, and is approaching a value of 10 or smaller beyond 0.13 µm technology generation. As a result, latency of flip-flops or latches is becoming a larger portion of the cycle time. In order to achieve a design that is both high performance and power efficient , careful attention must be paid to the design of the flip-flop and latches.

II. CONCEPT OF EXSISTING SYSTEM

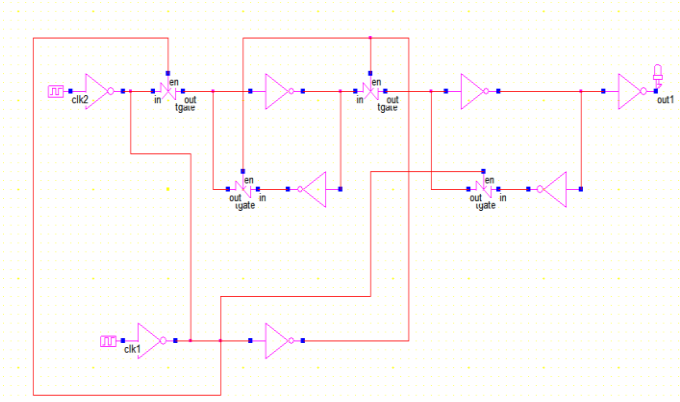


Fig. 1 Conventional transmission-gate flip-flop (TGFF).

Here we analyze problems on previously designed typical low power flip-flops with comparison to a conventional flip-flop as in Fig.1. The Fig. 2 shows a typical circuit of differential sense- amplifier type FF (DiffFF). This circuit is very effective to amplify small-swing signals and so it can be used in output part of memory circuits. In this type of flip-flop , the effect of power reduction degrades if the data activity is low, because these kind of circuits have pre-charge operation in every clock-low state. Even though if we use reduced clock swing, then it requires a customized clock generator and an extra bias circuit.

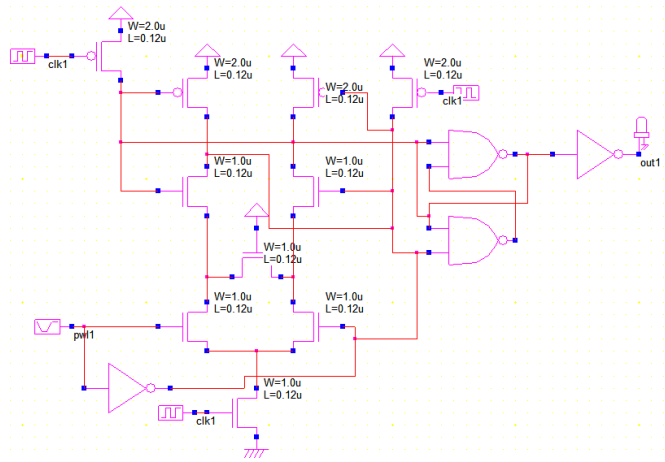


Fig. 2 Differential sense-amplifier flip-flop (DiffFF).

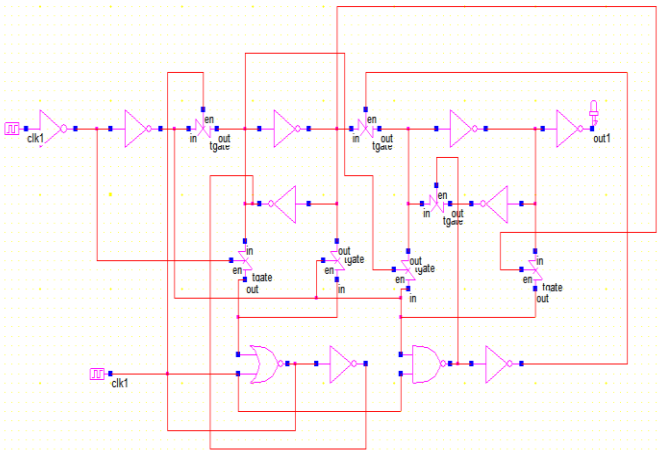


Fig. 3 Conditional-clocking flip-flop (CCFF).

Figure 3 shows a circuit of conditional- clocking type flip-flop (CCFF). This circuit monitors the change in input data at each and every clock cycle. If the input data are not changed then the circuit disables the operation of internal clock. By this operation, the power can be reduced when the input data are not changed. But the drawback is that the cell area doubles that of the conventional circuit shown in fig.1. and mainly due to this size issue , it becomes hard to use if the logic area is relatively large in the chip.

Figure 4 shows the circuit of cross-charge control FF (XCFF) [7]. The feature of this circuit is to drive output transistors separately in order to reduce charging and discharging of gate capacitance. However during actual operation, some of the internal nodes are pre-set with clock signal if the data is high, and this operation dissipates extra power to charge and discharge internal nodes. As a result, the effect of power reduction will decrease.

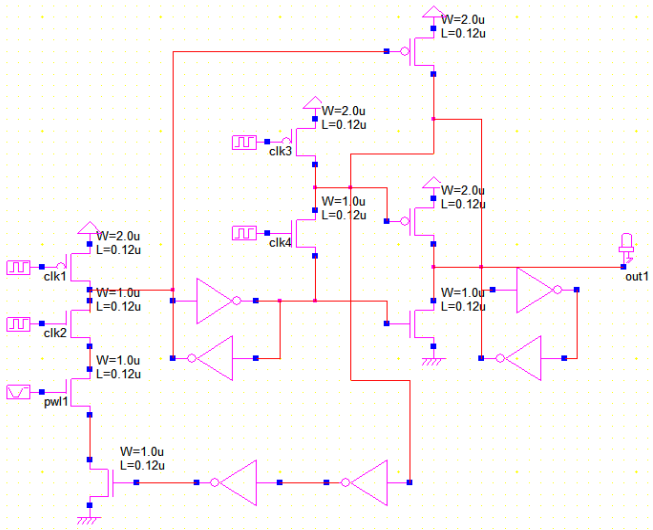


Fig. 4 Cross-charge control flip-flop (XCFF).

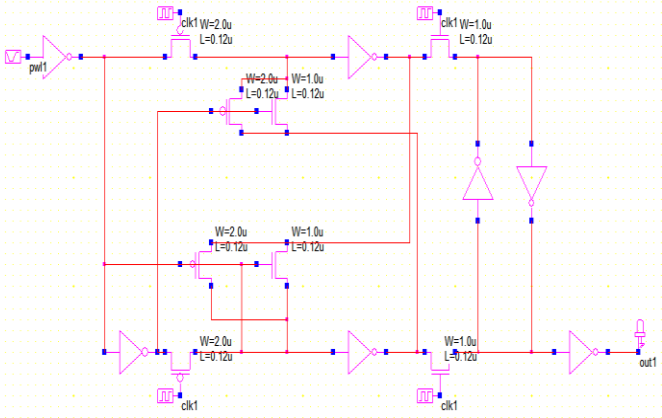
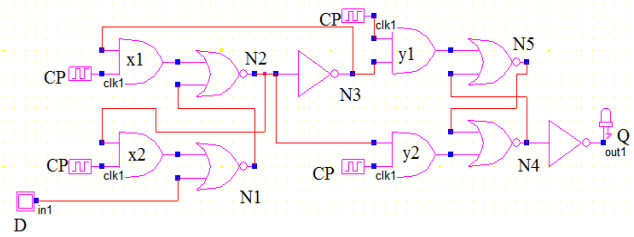


Fig. 5 Adaptive-coupling flip-flop (ACFF).

The figure5 shows the adaptive coupling type flip-flop which is based on a 6 transistor memory cell. In this flip-flop, the double channel transmission gate is replaced by a single-channel transmission gate with additional dynamic circuit which has been used for the data line in order to reduce the clock related transistors. But here the delay gets affected easily by input clock slew variation because different types of single channel transmission gate are used with the common data line and clock signal. Moreover , characteristics of single channel transmission gate circuits and dynamic circuits are strongly affected by process variation. Therefore, their optimization is very difficult, and performance degradation across various process occurs.

III. DESIGN METHODOLOGY

The power of the FF is mostly dissipated in the operation of clock-related transistors, and reduction of transistor count is effective to avoid cell area increase and to reduce load capacitance in internal nodes.



AND logic inputs:

X1: CP & N3

X2: CP & N2

Y1: CP & N3

Y2: CP & N2

Fig. 6 Schematic diagram of proposed FF.

In the conventional FF shown in 9 transistors are 12 clocked transistors. It is quite difficult to reduce the clock-related transistor directly from this circuit. One reason is because transmission-gates need a 2-phase clock signal, thus the clock cannot be eliminated. Another reason is that transmission-gates is constructed by both PMOS and NMOS to avoid degradation of data transfer characteristics caused by single-channel MOS usage. There-fore, instead of transmission-gate type circuit, we consider a combinational type circuit as shown in Fig. 6. To reduce the transistor-count we consider a method consisting of the following two steps. The first step is to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals. Then, merge those parts in transistor level as the second step.

IV . CONCEPT OF PROPOSED FLIP-FLOP

The FF which is shown in figure 6 consists of the master-latch is an asymmetrical single data-input type.

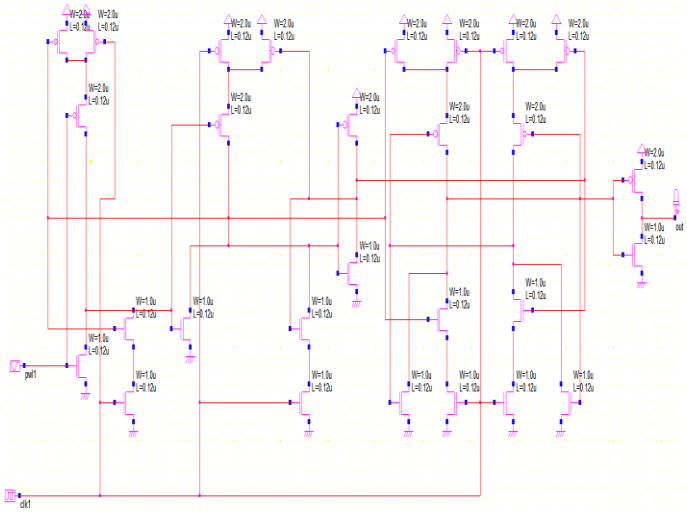


Fig. 7 Transistor level schematic of Fig. 6

The feature of this circuit is that it operates in single phase clock, and it has two sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2. Fig. 7 shows the transistor-level schematic of Fig. 6. Based on this schematic, logically equivalent transistors are merged as follows. For the PMOS side, two transistor pairs in M1 and S1 blocks in Fig. 7 can be shared as shown in Fig. 8. When either N3 or CP is Low, the shared common node becomes VDD voltage level, and N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 individually.

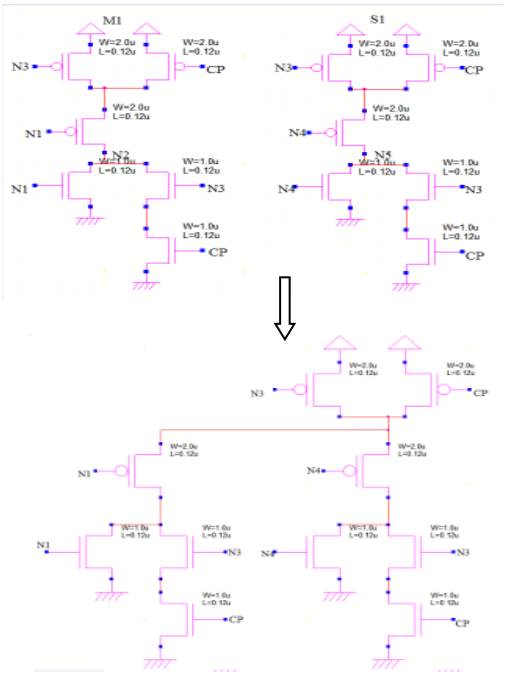


Fig. 8 Transistor merging in PMOS side

When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N3 and CP. As well as M1 and S1 blocks, two PMOS transistor pairs in M2 and S2 blocks are shared. For the NMOS side, transistors of logically equivalent operation can be shared as well.

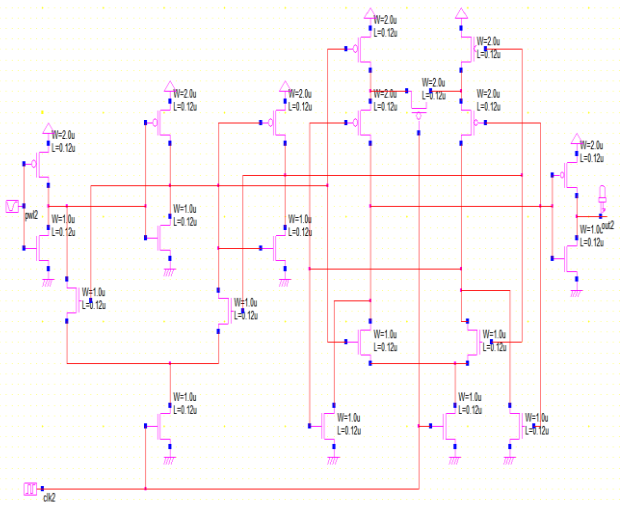


Fig.9 Transistor level schematic of topologically compressed flip-flop (TCFF).

Two transistors in M1 and M2 blocks in Fig. 8 can be shared. Transistors in S1 and S2 are shared as well. Similarly the transistors are merged in PMOS side.

This process leads to the circuit shown in Fig. 9. This circuit consists of seven fewer transistors than the original circuit shown in Fig. 7. The number of clock-related transistors is only three. We call this reduction method Topological Compression (TC) method. The FF, TC-Method applied, is called Topologically-Compressed Flip-Flop (TCFF).

V. SIMULATION RESULTS

a)PROPOSED METHOD

The simulation Output of 28Transistor flip-flop is shown below

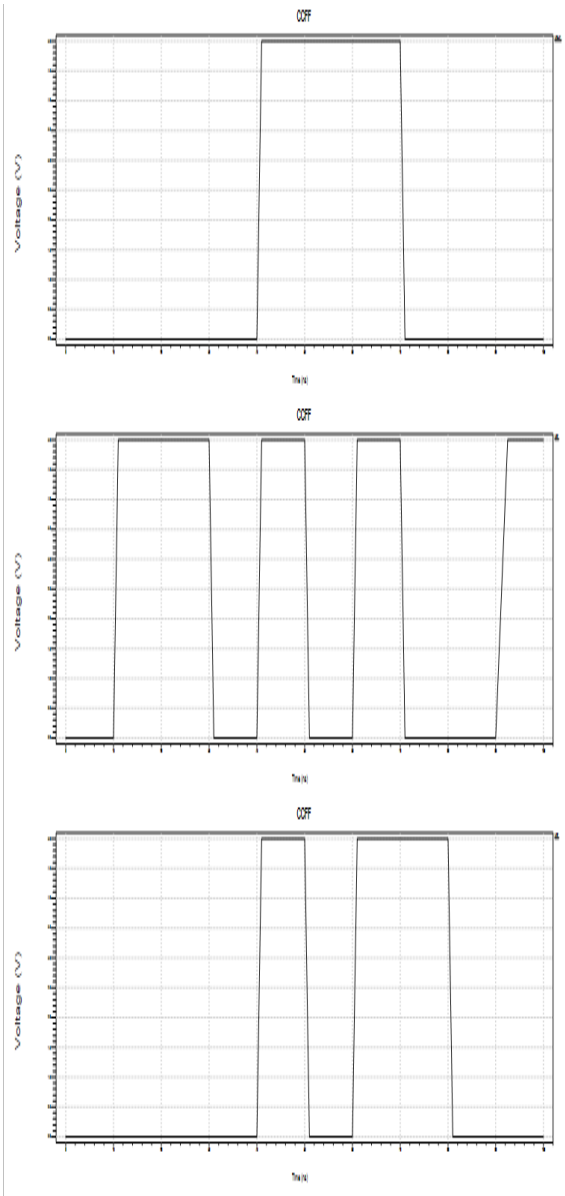


Fig.10 Output of 28Transistor flip-flop

The simulation output of Topologically Compressed Flip-flop is shown below

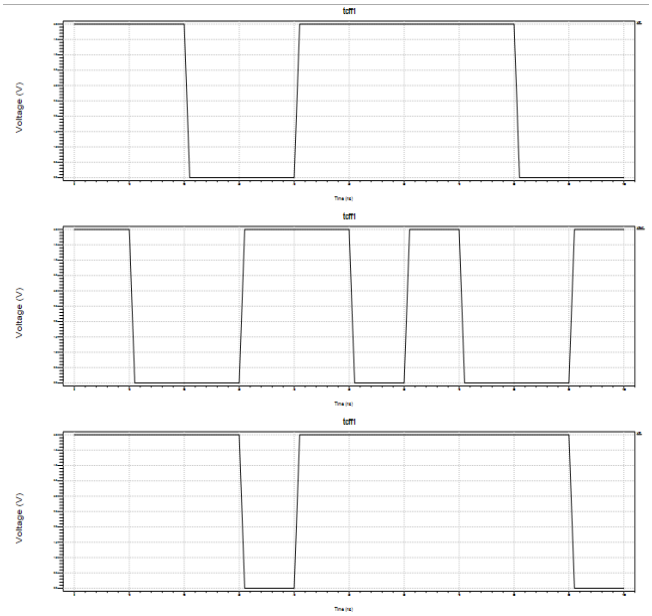


Fig.11 Output of Topologically Compressed flip-flop

TABLE1

Comparison of flip-flops

Types of flip-flop	Power (µw)
TGFF	179
Diff FF	101.02
CCFF	52.6
XCFF	33.8
ACFF	22.9
28T	20.5
TCFF	17.1

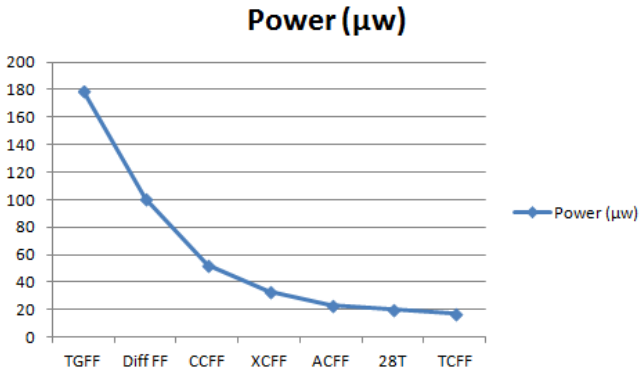


Fig.12 Power graph

VI. ANALYSIS OF POWER DISSIPATION

Power dissipation analysis has been carried out for the proposed circuit 28 transistor flip-flop. Here the power dissipation is analyzed for the voltage between 0.5v and 5.0v.

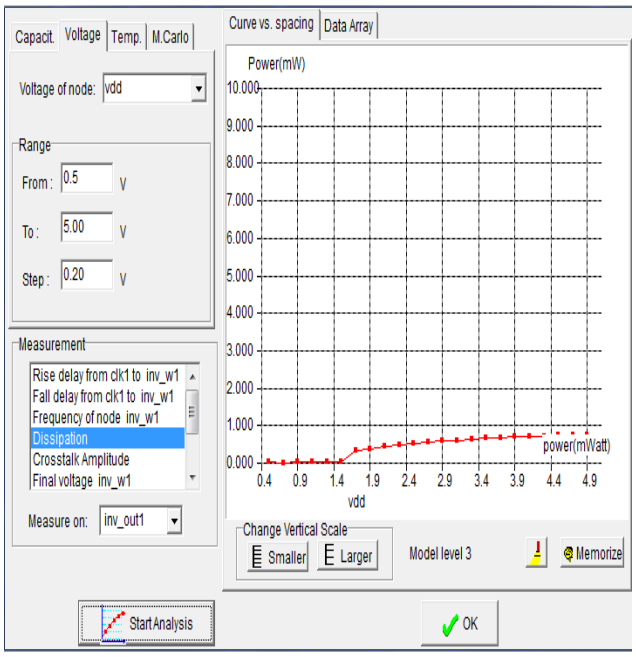


Fig.13 Power dissipation analysis of 28T FF

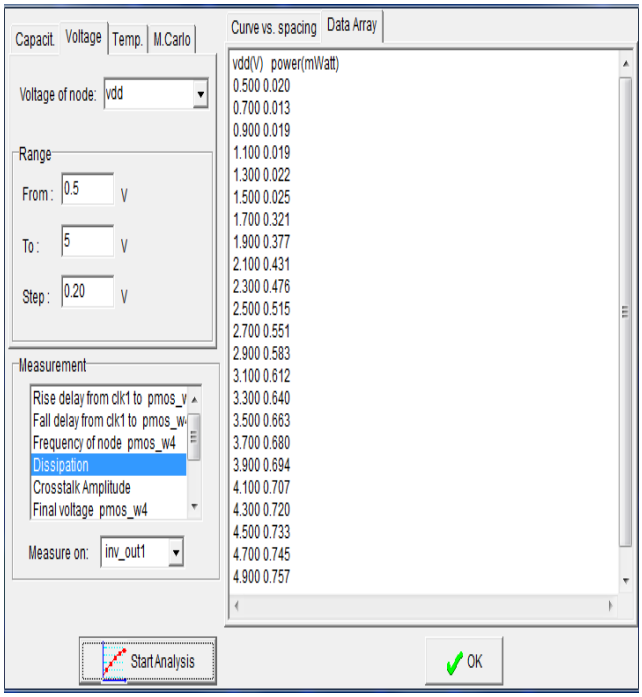


Fig.14 Data array for power dissipation analysis of 28T FF

Power dissipation analysis has been carried out for the proposed circuit 28 transistor flip-flop. Here the power dissipation is analyzed for the voltage between 0.5v and 5.0v.

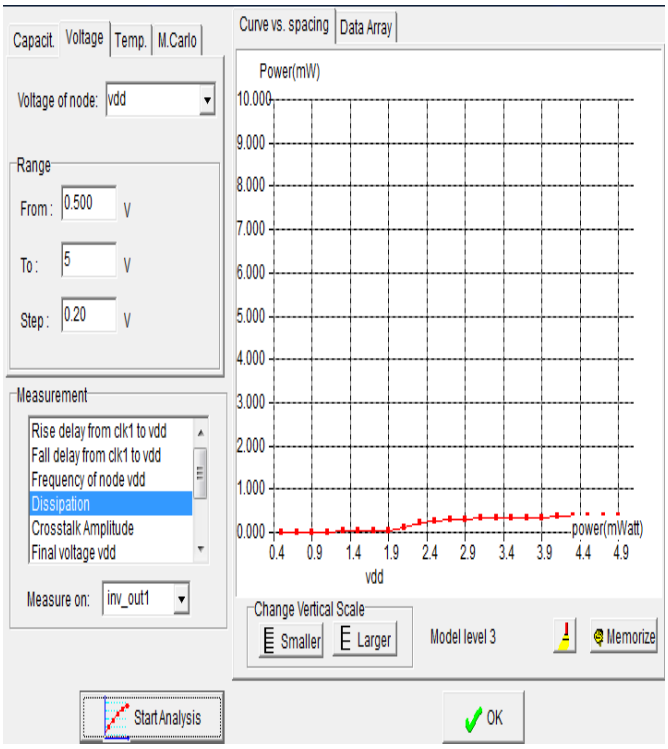


Fig.15 Power dissipation analysis of TCFF

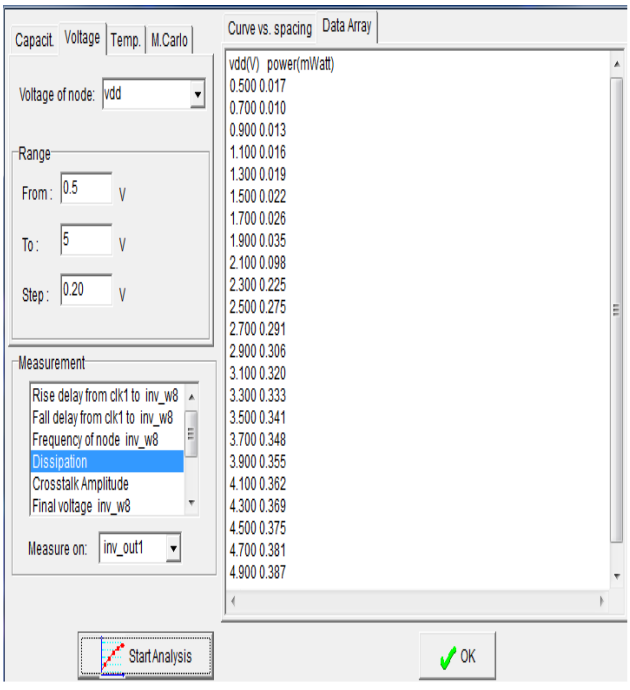


Fig.16 Data array for power dissipation analysis of TCFF

VII. CONCLUSION

A low-power FF, TCFF, is proposed using topological compression design methodology. TCFF has the lowest power dissipation in almost all range of the data activity compared with other low-power FFs. The power dissipation of TCFF is 75% lower than that of TGFF at 0% data activity without area overhead. In TCFF, since data-input or data-output operation is controlled by three clock - related transistors, by changing the size of those transistors, performance can be changed. Changing only three transistors in 21 transistors of a TCFF circuit does not affect cell area much. The topology of TCFF is easily expandable to various kinds of FFs without performance penalty. In summary, including a variety of clock-related transistor sizes, TCFF can be applied to various speed systems, and it can reduce whole chip power more effectively.

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