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Design and Implementation of TCSG and High Speed Protocol for HF Radar

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***Abstract*— The target of the this paper is to augment the existing HF and PR weather radars situated at Thumba Equatorial Rocket Launching Station (TERLS), Vikram Sarabhai Space Center (VSSC), Trivandrum and maintained by the Space Physics Laboratory (SPL), V.S.S.C, Kerala, by replacing the existing Analog and partially digital radar control, receiver and transmitter units with a fully digital, integrated system-on-board. The proposed new architecture of HF Radar Digital Receiver consist of mainly four modules. Focus on implementing the Timing and Control Signal Generation (TCSG) module in FPGA and also a High Speed Protocol for serial communication. TCSG unit controls the whole synchronization of HF Radar Receiver. HF Radar settings are to be entered into the TCSG module in FPGA in run time.. The high speed protocol is designed for communicating the Radar Receiver to the PC and also it communicating with the modules in FPGA. To implement this, hardware ML605 Evaluation board is used.**

***Index Terms*—TERALS, Timing and control signal generation, DDC, Direct digital synthesizer**

I. INTRODUCTION

The HF Radar receiver system used for Ionospheric measurements, installed at VSSC, Trivandrum, is a phase coherent, pulsed, Monostatic and moderately high power Doppler radar operating at 18 MHz (in the current case) and it is installed at the magnetic equatorial station Trivandrum (8.5ºN,77ºE). It is a powerful tool to study the plasma instability processes responsible for the generation of Equatorial Electro Jet (E.E.J) and Equatorial Spread F (E.S.F) irregularities [1]. The HF Radar system used here works mainly on 18 MHz; a pulsed RF signal of the above frequency is generated by the exciter. This signal is amplified to 50kW peak power in the transmitter and is fed to the antenna. This electromagnetic energy is radiated into space by antenna array. The back scattered signal from the irregularities are passed through a coherent receiver where the signal is phase detected using two reference signals having quadrature phase relationship.[2]. The in phase and
quadrature phase outputs of the two phase detectors (sine and cosine channels) have all the information contained in the backscattered received signal.

II. LITERATURE SURVEY

In 19th centaury they developed an analog vacuum tube based radar receiver. On that radar is fully analog based and they having a RF amplifier to amplify the RF signal which will coming from an antenna. The Mixer were mix up the output from the amplifier and a local oscillator. In IF stage, the central frequencies were used are 445 kHz &10.7 MHz for AM & FM broadcasting, then the modulated signal is given to the Demodulator to collect the original form of the modulated signal. Then in 20th century they were modified the system as partially digital. That is the transmitter section was analog and receiver part is digital. In that system, the RF amplifier which were present in the analog system replaced with an A/D converter and other all subsequent functions such as mixing, filtering, demodulation were done by using a digital signal processing elements. Now they again modified the system as fully digital and integrated system on board .Which is Implemented using Virtex6 FPGA [8] [9] & ML605 Evaluation board [10].

III. DESIGN METHODOLOGY

The target of this paper is to augment the existing HF and PR weather radars situated at Thumba Equatorial Rocket Launching Station (TERLS), Vikram Sarabhai Space Center (VSSC), Trivandrum and maintained by the Space Physics Laboratory (SPL), V.S.S.C, Kerala, by replacing the existing Analog and partially digital radar control, receiver and transmitter units with a fully digital, integrated system-on-board.

IV. PROPOSED NEW ARCHITECTURE OF HF RADAR RECEIVER

The task of implementing the HF Radar Receiver as a whole is divided into four modules:

- Timing and Control Signals Generation (TCSG)
- Signal Generation and Down Conversion block (DDS & DDC)
- Signal Processing Unit (FFT)
- GUI - Data Storage Interfacing & ADC - DAC Interfacing

ADC module is for digitizing Doppler shifted data (18MHz ± f_d). For Analog to digital conversions and vice versa use 4DSP FMC 150 ADC/DAC FMC daughter card with ADS62P49, dual 14bit 250 MSPS ADC and DAC 3283, dual 16bit 800MSPS DAC. Fig 1 shows the Receiver block diagram.

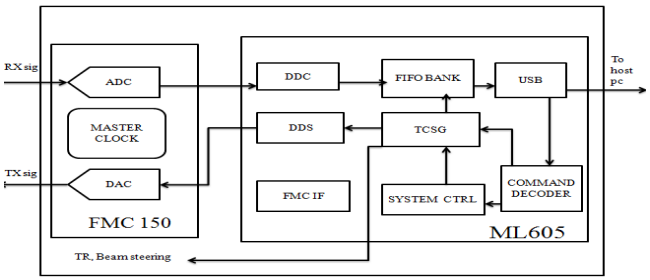

Fig 1. Receiver block diagram

The 18 MHz Digital RF signal(14 bit) is digitally down converted to baseband signal in Digital Down Converter(DDC) module. DDC consist of two multipliers which multiplies the received signal with in-phase and quadrature carrier signals (18 bit) to get baseband I & Q signals (32 bit). The multirate filter consisting of a low pass filter and down sampler is implemented using an accumulator.

The In phase and Quadrature phase sinusoid signals are generated using Direct Digital Synthesizer (DDS) module. DDS is configured to generate 18.1 MHz sine and cosine signals of output width 18 bits , phase width 30 bits, frequency resolution .25 Hz , phase angle width of 16 bits.

TCSG is wired around a state machine. TCSG generates Timing signals based on four counters viz PRF counter, PW counter, Window counter and Range gate counter. PRF counter generates the time base for TX signal, TR signal, window start, PRF counter have a variable time period equal to PRT(pulse repetition time) pulse width counter keep track of the pulse width, it have a variable terminal count corresponding to selected pulse width. Range gate counter counts each pulse when window is on, it selects the FIFO to which sampled data is written.

There are 64 FIFOs each 1024 deep and 64 bit width, FIFOs are arranged into 4 banks each having 16 FIFOs. Each FIFO is selectable through FIFO select lines and FIFO bank select lines. System control manages start acquisition, read data, test mode and stop commands. It is wired around a state machine. Command decoder is implemented as a multiplexer with lower bits of command as select lines and higher bits as input.

V. TIMING AND CONTROL SIGNAL GENERATION

TCSG unit controls the whole synchronization of HF Radar Receiver. So this module forms an important class of circuits in HF Radar Receiver. HF Radar settings are to be entered into the TCSG module in FPGA in run time. For this, TCSG module is designed. The high speed protocol is designed for communicating the Radar Receiver to the PC and also it communicating with the modules in FPGA. To implement this, hardware ML605 Evaluation board is used. General block diagram of TCSG is as shown in Fig 2.

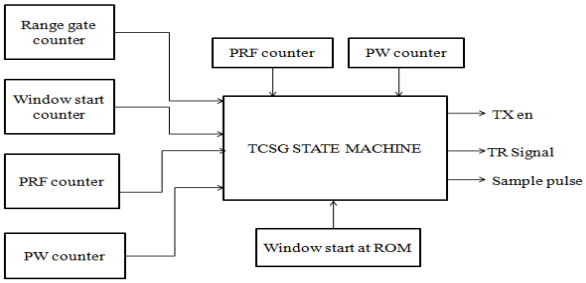

Fig 2. General block diagram of TCSG

VI. FSM FOR TCSG

Coding for TCSG module is done in VHDL using state machine technique and initial simulations were carried out in Xilinx ISim. Description of states used for controller design is as shown below. Fig 3 shows the State machine of TCSG.

State 0 = initialization of timer values

State 1 = T/R pulse high, which means Transmitter section ON. Beam orientation is also enabled here.

State 2_00 = TX pulse is of width 20µs

State 2_01 = TX pulse is of width 60µs

State 2_10 = TX pulse is of width 80µs

State 2_11 = TX pulse is of width 100µs

State 3 = TX becomes low, T/R high for (150 - PW) µs

State 4 = TR becomes low and a wait period before reception

State 5 = Window Starts At pulse becomes high, enabling the start of reception, ADC should be enabled here.

Done state = Window Starts becomes low, showing the end of reception and wait for pulse repetition time.

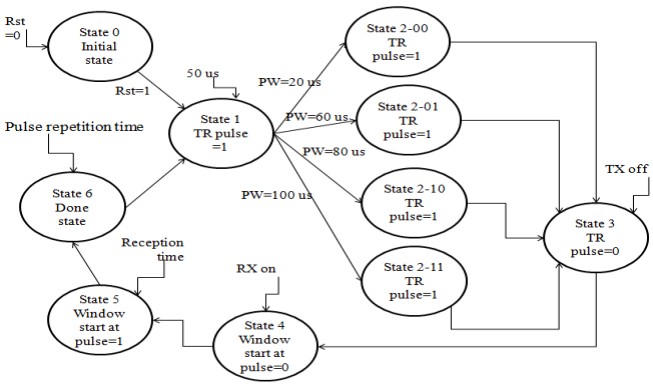

Fig 3. State machine of TCSG

VII. GUI USING MATLAB

HF radar settings are to be entered into the TCSG module running in FPGA through a graphical user interface (GUI). So for writing the specification values for TCSG module, in real time, a GUI is created using MATLAB software. Using this, settings can be serially sent to the USB core module.

VIII. SERIAL COMMUNICATION USING USB

Here the communication between Radar Receiver and PC is done through a high speed protocol. From Radar we will get 32 data*2 (I & Q) *1024 samples*64 Range gates*250 PRF data in 4sec. In 1 sec we will get 1048576 bits. Our aim is to collect the data from receiver as much as possible. So we used here USB for communication rather than UART. The controller which is used here are Cypress EZ (CY7C67300) micro controller. The data which is coming from the PC is getting in Cypress controller through a USB port. The USB peripheral controller read the data which is stored in the memory of Cypress by using a HPI interface and then the Radar read the data from the controller. Likewise the data which is coming from the Radar is write into the controller, then that data is again write into the Cypress controller by using a HPI interface. At last the PC read the data from the Cypress controller. The block diagram in Fig 4 shows the communication path between PC and a Radar Receiver.

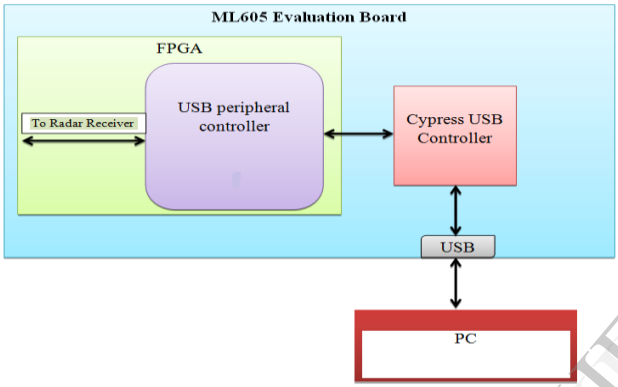

Fig 4. USB communication block diagram

IX. FSM FOR SERIAL COMMUNICATION PROTOCOL

Coding for USB core is done in VHDL using state machine technique and initial simulations were carried out in Xilinx ISim. Fig 5 shows the description of State design for USB.

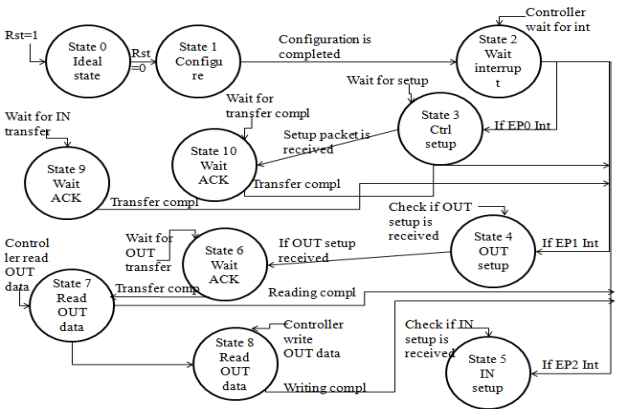

Fig 5. Sate machine for USB

X. SIMULATION AND IMPLEMENTATION RESULTS

TCSG module and the USB core has been coded in VHDL and Simulated in ISim using Xilinx ISE 13.2. In TCSG when TR Pulse is High then the TX (Transmission) is ON but RX is OFF. And when TR Pulse is Low then the RX (Reception) is ON but TX is OFF.

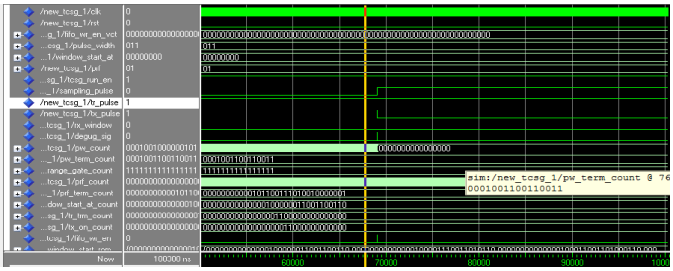

Fig .6.TX ON when TR is High

First we have to give the Pulse Width as 20us, Window start at as 540us, Pulse Repetition Frequency as 167Hz. Then reset the system and removed and then give the clock as '1' and keep the tcsg_run_en as '0' and run it. Then change the tcsg_run_en as '1'. After compile and run we will get TX pulse is '1' (ON) when TR pulse is '1' (HIGH) at that time the RX window is '0' (OFF).

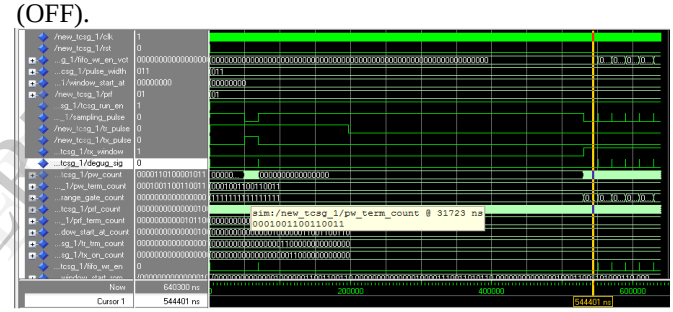

Fig 7.RX ON when TR is Low

The same way receiver part is simulated. Here also given the Pulse Width as 20us, Window start at as 540us, Pulse Repetition Frequency as 167Hz. Then reset the system and removed and then give the clock as '1' and keep the tcsg_run_en as '0' and run it. Then change the tcsg_run_en as '1'. After compile and run the code with 540ns then we will get RX pulse is '1' (ON) when TR pulse is '0' (LOW) at that time the TX window is '0' (OFF). After completing the Reception the process which will continue from the start that is at TR pulse is ON.

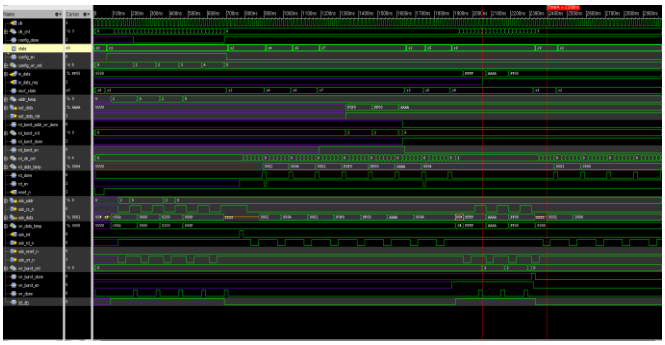

Fig .8.Complete simulation of USB

Here used universal serial bus for serial communication, which is a high speed protocol. After completing the configuration, it goes to next state that is state2 then there it will wait for an interrupt. If EP0 (Endpoint 0) came then it goes to state3 that's for control setup, like wise if EP1 (Endpoint 1) or EP2 (Endpoint 2) are came then it goes to state 4 and 5 for OUT and IN setup. After completing the writing process it goes to state2 and waits for an Interrupt.

XI. IMPLEMENTATION RESULTS USING THE NEW SYSTEM

At present, HF radar data processing algorithm is implemented in MATLAB and it is envisaged that in near future it will be implemented in on-line processing using DSP processor. Presently, de-noising is not performed in the HF radar signal processing. However, there is a provision for implementing this in future versions of data processing software. The following are the HF radar signals at various steps of data processing.

A. E- region measurements

Presented here in Fig 9 and Fig.10 are the radar backscattered signal from the daytime E region on June 27, 2014 employing the Zenith, East and West and beam of the radar. The typical daytime drift is around ~ 15Hz which corresponds to Doppler velocity of about 200 m/s. The E region irregularity spectrum as measured in zenith at different range gates starting from 87km to 132km, each range gate being 3km.

The various radar parameters like number of coherent integrations, beam orientation etc. fixed for this measurement is given at the top of the figure.

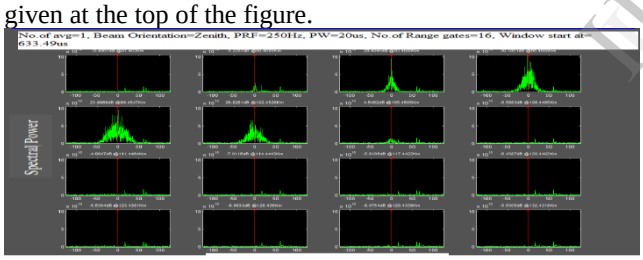

Fig 9. E region irregularity spectrum as measured in zenith at different range gates starting from 87km to 132km, each range gate being 3km

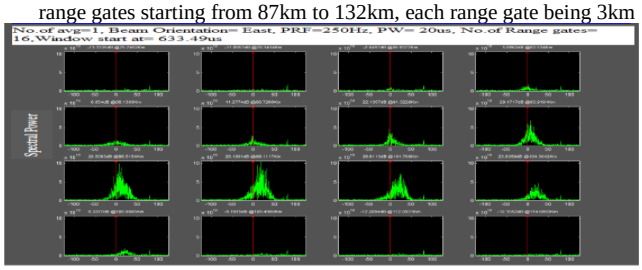

Fig 10. E region irregularity spectrum measured using east beam at different range, starting from 75 km to 114 km, each range gate being 3km

B. F-region measurements

The refurbished HF radar has been operated in the nighttime for the measurements concerning the Equatorial Spread-F related irregularities over Trivandrum. Presented here in the Fig 8 is a typical ESF backscattered signal in the first eight range gates starting at ~363 km altitudes. The backscatter is found to be maximizing around 423km altitude which is consistent with the typical ESF measurements made earlier using HF radar from Trivandrum. It is apparent, however, that the signal to noise ratio needs to be further improved (desired level ~12-15dB) for unambiguous estimation of the moments.

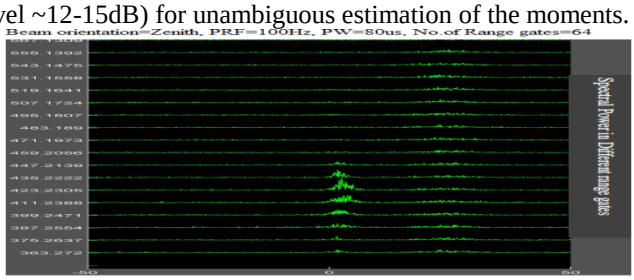

Fig 11. Exhibiting the height range spectra of moderate ESF irregularities. X axis represents the Doppler in (Hz) and the spectra represents the relative power of the backscattered signal.

XII. CONCLUSION

HF Radar is a crucial component in accessing the behavior of Electro Jet (E region) and wind current at an altitude range of 80 - 110 km and 150 – 1000 km (F region) above the earth surface. The augmentation of the Receiver system of HF Radar to the State-of–the-art, Digital Receiver using FPGA has been configured. Here TCSG and USB Core are coded in VHDL and synthesized in Xilinx ISE 13.2. Then a GUI is created using MATLAB from where settings can be serially send to the USB core module. Finally the TCSG and USB module using MATLAB is configured in FPGA and integrated with the system. The final implementation phase focus on system integration of all the Digital Receiver with High speed protocol.

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