

Design and Implementation of Single Output Forward Converter for Spaceborne Applications

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Abstract - Spaceborne electronic systems demand compact, efficient, and highly reliable power supplies capable of operating under varying input conditions while maintaining stable output regulation. This work presents the design and hardware implementation of a 35 W single output DC DC Forward converter, intended for spaceborne power supply applications. The converter operates at a switching frequency of 140 kHz. A voltage feed-forward control technique is employed on the primary side using a PWM controller to achieve superior line regulation and rapid dynamic response to input voltage transients. A Magnetic Amplifier (Mag-Amp) is incorporated as a secondary-side post-regulator to enhance load regulation and minimize output voltage ripple. Comprehensive protection circuits including over-voltage, under-voltage, and over-current protection are implemented to ensure reliable operation in harsh space environments. The hardware prototype achieves an efficiency greater than 79 percent at full load, a line regulation of 0.14 percent, a load regulation as low as 0 percent, and an output voltage ripple well below the 30mV peak-to-peak as per specification.

Keywords - Forward Converter; Spaceborne Power Supply; Voltage Feed-Forward Control; Magnetic Amplifier (Mag-Amp); PWM Controller .

I. INTRODUCTION

Power supply units (PSUs) for space and high-reliability applications must satisfy stringent requirements, including high efficiency, wide input voltage range, galvanic isolation, low output ripple, and robust protection. DC–DC converters are central to spaceborne power management systems, where they must operate reliably across extreme temperature ranges and withstand radiation exposure [1][6].

Among the various DC–DC converter topologies including Buck, Boost, Buck-Boost, Cuk, SEPIC, Flyback, Half-Bridge, and Full-Bridge the Forward converter stands out for medium-power space applications due to its simple topology, inherent galvanic isolation, high efficiency, and compact form factor. Unlike the Flyback converter, which stores energy in the transformer core during the switch ON period, a Forward converter transfers energy directly to the load during conduction, resulting in better output regulation and lower transformer stress [3][5][9].

Conventional voltage-mode feedback control suffers from slow dynamic response to input line variations, making line regulation difficult over a wide input range. The voltage feed-forward control technique overcomes this limitation by directly modulating the PWM duty cycle in proportion to input voltage changes, thereby achieving instantaneous compensation without relying solely on the feedback error amplifier [2][7].

To achieve accurate secondary-side load regulation, a Magnetic Amplifier (Mag-Amp) is employed as a post-regulator. Mag-Amps exploit the magnetic saturation properties of high-permeability cores to effectively function as a controlled switch, providing robust, passive regulation with high radiation tolerance a critical advantage for space environments [10].

II. CONVERTER SPECIFICATIONS

Table 1 lists the key design specifications for the proposed forward converter.

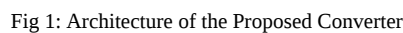
Table 1: Specifications of the Proposed Forward Converter

Parameter	Specification
Topology	Forward DC–DC Isolated Converter
Input Voltage Range	30 V – 44 V
Switching Frequency	140 kHz
Duty Cycle Range	27% – 40%
Output Voltage / Current	7 V / 5 A
Output Power	35 W
Efficiency at Full Load	> 70%
Line Regulation	≤ 1%
Load Regulation	≤ 1%
Output Voltage Ripple	< 30 mV p-p
Operating Temperature	–55°C to +125°C

III. SYSTEM ARCHITECTURE AND BLOCK DIAGRAM

The architecture for the proposed forward converter is illustrated in Fig 1. The input stage contains a Common Mode Interference (CMI) filter and a Differential Mode Interference (DMI) filter for electromagnetic compatibility (EMC) followed

The output is rectified with a diode and filtered with an LC network to supply the load. The circuit incorporates OVP, UVP, and OCP protection circuits.



The proposed forward converter circuit is shown in Fig 2

Mode 1 – Switch ON:

Mode 2 – Switch OFF:

When the MOSFET is OFF, the voltage across the primary transformer winding reverses. The reset diode, D3 conducts allowing the discharge of the magnetizing current to reset the transformer core. On the secondary side, the diode D1 becomes reverse biased while the D2 (freewheeling diode) conducts current to the load, maintaining the inductor current to flow. The output capacitor supplies energy to the load, partially discharged to maintain the output voltage. The Mag-Amp is OFF and the converter cycle repeats to maintain a regulated output voltage.



A. Transformer Design

The optimum design is decided by the small size and lower dissipation of transformer, so Window Factor (KW), Flux Density (BM) & Current Density (J) values are assumed, for optimal design.

Window Factor (KW) = 0.35

Maximum Flux Density (BM) = 0.12 Tesla

Current Density A/mm² (J) = 6 Amp/mm²

Efficiency = 70%

Maximum duty cycle (Dmax) = 0.4

Switching Frequency (Fsw) = 140 kHz

$$V_d = \text{Diode Drop}$$

Output Power (P_{out}) = 35 W

$$A_p = \frac{\sqrt{D_{\max}} * P_{\text{out}} \left(1 + \frac{1}{\text{Efficiency}} \right)}{K_w * I * 10^{-6} * B_m * F_{\text{sw}}} \quad (1)$$

$$A_p = A_c * A_w \quad (2)$$

$$N_p = \frac{(V_{in_{min}} * D_{max})}{B_m * A_c * 10^{-6} * F_{sw}} \quad (3)$$

$$T_{\text{ratio}} = \frac{N_s}{N_p} = \frac{V_{\text{out}} + (V_D * D_{\text{max}})}{D_{\text{max}} * V_{\text{inmin}}} \quad (4)$$

$$N_s = T_{ratio} * N_p \quad (5)$$

Selected core: OR42616UG, AL: 5213mH/1000T.

B. Selection of MOSFET Switch

The selection of a MOSFET is based on several important electrical parameters, including the drain-to-source voltage

(V_{DS}), drain current (I_d), drain-to-source ON-state resistance ($R_{DS(on)}$), total gate charge (Q_G), and output capacitance (C_{OSS}). These parameters significantly influence the switching and conduction characteristics of the device. The final MOSFET selection and package size are determined by evaluating the total power dissipation, which includes both conduction and switching losses, to ensure efficient and reliable operation.

Selected MOSFET: JANSR2N7584T1, 200V, 0.029 Ω , 45A

C. Mag-Amp Core Design

The Mag-Amp core is selected using the area product method with a withstanding volt-second product of 65 μ Vs calculated from the secondary pulse voltage and switching period. A nano-crystalline cobalt alloy toroidal core 6-L2016-W763 is selected. The number of Mag-Amp turns $NMA = 9$ turns, wound with wire sized for 3.5 A secondary current at 6 A/mm² current density.

D. Secondary diode selection

The output diode is selected based on the secondary-side voltage and current ratings. Schottky diodes are preferred in Forward converters due to their low forward voltage drop, high current capability, and negligible reverse recovery time, which minimizes switching losses and improves converter efficiency. Considering a 70% derating with an additional 50% margin for leakage inductance voltage spikes, the 35CGQ150 Schottky diode (150 V, 35 A, $V_F=0.6$ V, space-grade die) is selected for the proposed converter.

E. Output LC Filter Design

The output LC filter is designed to limit ripple at the secondary of the Mag-Amp. With the effective secondary duty cycle and a 25% inductor current ripple allowance, the output filter inductor $L = 20$ μ H and filter capacitor $C = 12$ μ F are calculated. This ensures output ripple remains well below the 30 mV p-p specification.

F. PWM Controller and Gate Driver Selection

The UC2525A PWM controller is selected to generate the switching pulses for the Forward converter operating at 140 kHz. The switching frequency was set by choosing appropriate RT and CT values according to the manufacturer's specifications. The controller was provided with an internal oscillator, error amplifier, PWM comparator, and soft-start circuit to ensure the exact duty cycle during the stable state. The PWM output signal was sent into the MIC4424YM MOSFET gate driver which provided high current outputs to adequately charge and discharge the gate of the primary power switch. The result was a short switching time, low switching losses, and reliable operation of the main power switch.

G. Protection Circuits

Three protection circuits are provided as follows:

1. The under-voltage protection (UVP) circuit senses the input voltage. If it drops below 28 V, the PWM shutdown pin is set to latch preventing incorrect operation of the converter and damage to the switching components.

2. The over-voltage protection (OVP) circuit senses the output voltage. If it increases above 7 V specification, the shutdown signal disables the PWM to protect the load.

3. The over-current protection senses the input current and initiates shutdown of the PWM IC, if it rises above 130% of the rated value (protection is latched). This protects switching devices and the transformer in the circuit.

VI. EXPERIMENTAL RESULTS

Fig 3 below represents the experimental platform utilized to verify the prototype's hardware model's functionality. A programmable DC power supply is used to provide the input voltage for the converter under test. The electronic load was attached to the converter's output to simulate various load conditions. The load allows the measurement of the output voltage and current of the converter under test. A Digital Storage Oscilloscope is used to view and analyze the converter's waveforms.

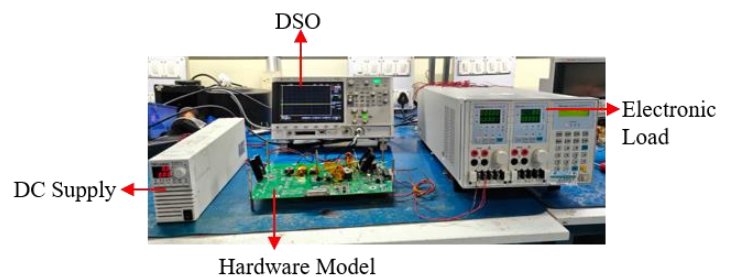
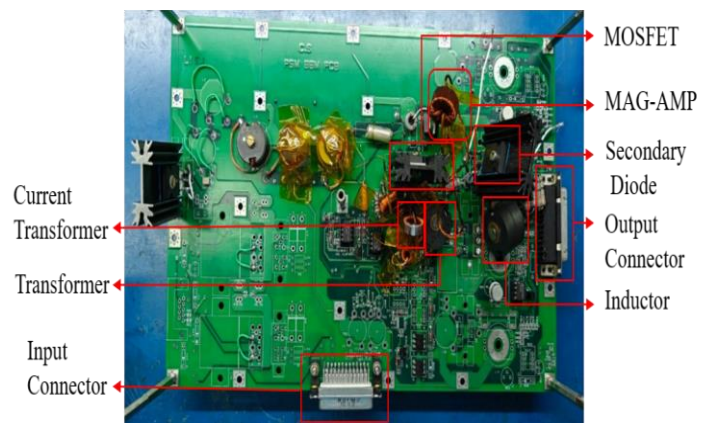


Fig 3: Experimental Setup

A hardware prototype model is developed incorporating all the designed blocks: input EMI filters, inrush current limiter, current transformers, start-up and bias circuits, forward converter power stage, Mag-Amp post-regulator, output rectifier and LC filter, PWM controller, gate driver, protection circuits, and opto-coupler isolated OVP feedback. Further, key components include MOSFET switching device, high-frequency transformer design using pot core, Mag-Amp on nano-crystalline cobalt core, PWM controller IC, and gate driver IC is presented Fig 4.



i) Top View



ii) Bottom View

Fig 4: Hardware Module of the Proposed Converter i) Top View ii) Bottom View

A. Output Voltage Regulation

Table 2 presents measured output voltage for the input voltage that ranges from 34 V to 42 V and load conditions from no-load to full load (5 A). It is observed from the results that, output voltage remains considerably regulated between 7.07 V and 7.09 V across all test conditions, which further demonstrates excellent regulation by combined feed-forward and Mag-Amp technique.

Table 2: Measured Output Voltage (V) vs. Input Voltage and Load

Vin (V)	Output Voltage(V)			
	No Load	Min Load (0.5 A)	Nom Load (2.5 A)	Max Load (5 A)
34	7.09	7.08	7.08	7.07
37	7.09	7.08	7.08	7.08
42	7.09	7.08	7.07	7.08

B. Output Voltage Ripple

The Hardware implemented circuit testing for Ripple voltage measurements is performed using a Digital Storage Oscilloscope at output terminals across the output capacitor, for full range of input voltages and load conditions. All measured values are well within the customer defined 30mV p-p specification. Table 3 summarizes the ripple measurements.

Table 3: Measured Output Voltage Ripple (mV p-p)

Vin (V)	Ripple(mV)			
	No Load	Min Load (0.5 A)	Nom Load (2.5 A)	Max Load (5 A)
34	9.6	8.0	6.8	9.4
37	8.0	6.4	7.2	8.6
42	11.8	8.2	10.0	7.6

C. Magnetic Amplifier Characterization

To validate Mag-Amp operation, voltage waveforms before and after the Mag-Amp are captured at full load (5 A) across secondary side for input voltages that ranges from 34V to 42V. Also, the saturation delay, the time from secondary voltage pulse onset to Mag-Amp saturation is consistently measured at 720 ns across all test conditions, confirming stable and predictable Mag-Amp regulation. Table 4 summarizes the Mag-Amp waveform parameters. The obtained delay measurement waveform that shows the saturation delay of the Mag-Amp at 37 V input and full-load condition is presented in Fig 5.

Table 4: Mag-Amp Waveform Characterization at Full Load (5 A)

Vin (V)	Delay Time (ns)	Before Mag-Amp Vpp (V)	After Mag-Amp Vpp (V)
34	720	97	82
37	720	105	86
42	720	113	96

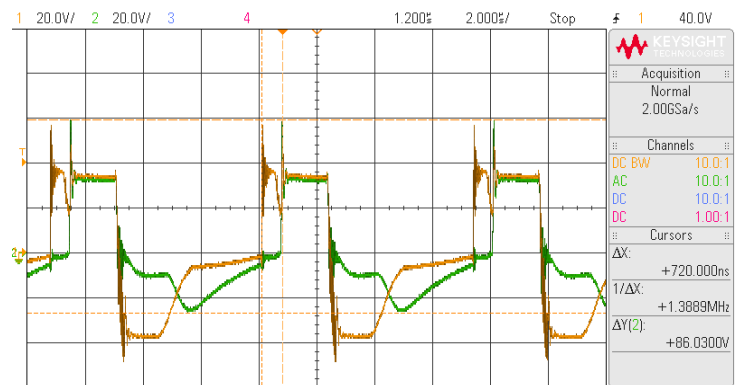
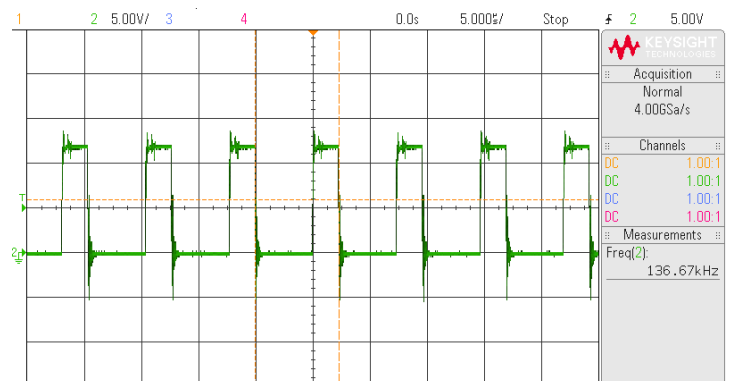


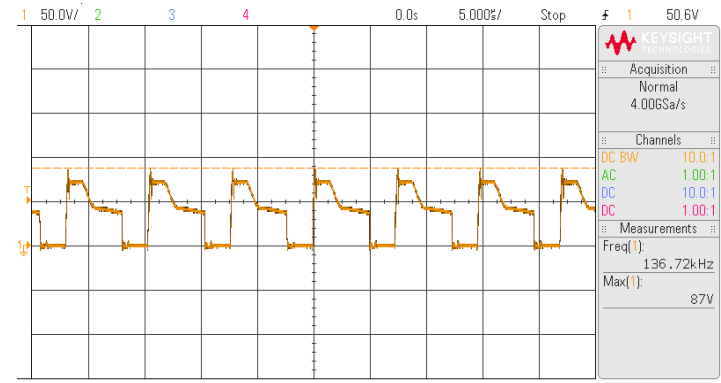
Fig 5: Delay measurement waveform showing the saturation delay of the Mag-Amp at 37 V input and full-load condition

D. MOSFET Switching Waveforms

The MOSFET gate-to-source voltage (V_{GS}) is measured at 37 V input, full load, confirming a switching frequency of 136.67 kHz, closely matching the designed 140 kHz. The drain-to-source voltage (V_{DS}) peaks at approximately 87 V during the OFF state, well within device ratings, with limited voltage overshoot confirming effective snubber circuit operation is presented in Fig 6.



i) Gate-to-source voltage (V_{GS}) waveform of the MOSFET at 37 V input and full-load condition



ii) Drain-to-source voltage (V_{DS}) waveform of the MOSFET at 37 V input and full-load condition

Fig 6 (i),(ii): MOSFET Switching Waveforms

E. Line and Load Regulation

Line regulation, defined as,

$$\% \text{Line Regulation} = \frac{V_{out \max} - V_{out \min}}{V_{out \text{nom}}} \times 100$$

is measured at 0.14% — significantly better than the 1% specification, is shown in Table 5.

Load regulation, defined as,

$$\% \text{Load Regulation} = \frac{V_{out \text{min load}} - V_{out \text{max load}}}{V_{out \text{nom load}}} \times 100$$

In this work, achieved Line and Load Regulation for input voltages of 34 V, 37 V, and 42 V respectively, as presented in Table 5 & 6. The obtained values for line and load regulation are found to be within the given specifications (<1%) by the customer.

Table 5: Line regulation

Vin(V)	Output Voltage(V)	Line Regulation
34	7.07	0.14%
37	7.08	
42	7.08	

Table 6: Load Regulation

Load Condition	Vin=34V Vout(V)	Vin=37V Vout(V)	Vin=42V Vout(V)
10%	7.08	7.08	7.08
50%	7.08	7.08	7.07
100%	7.07	7.08	7.08
Load Regulation	0.14%	0%	0%

F. Converter Efficiency

Efficiency is measured across load terminals for different input voltage values. It is observed from Table 7 that, for full load (5 A) efficiency ranges from 78.4% to 79.6%, for input voltage that ranges from 34 V to 42 V, better than mentioned (>70%) specification by the customer. Table 7 presents the efficiency values for various load conditions. Further, a low efficiency value attained for minimum load ($\approx 52\%$), which is a characteristic of fixed-frequency converters where switching

and magnetic losses dominate at light loads. At full load, the converter demonstrates comfortably the target efficiency.

Table 7: Measured Efficiency (%)

Vin (V)	Min Load (0.5 A)	Nom Load (2.5 A)	Max Load (5 A)
34	52.10%	76.60%	79.50%
37	53.20%	75.90%	79.60%
42	52.70%	75.20%	78.40%

VII. CONCLUSION AND FUTURE SCOPE

This research work includes the complete design, simulation, and hardware validation for a 35 W, 7 V / 5 A single-output Forward converter for spaceborne power supply applications. The combination of primary-side voltage feed-forward PWM control and secondary-side Magnetic Amplifier post-regulation provides outstanding regulation performance (0.14%) line regulation and near-zero load regulation. Further, output voltage ripple consistently below 12 mV p-p across all operating conditions is effectively achieved over a significant margin for the designed value of 30 mV p-p specification. Also, obtained the converter efficiency of 79% at full load for the 34–42 V input voltage range, with the hardware switching frequency of 136.67 kHz closely matching with the 140 kHz design target.

Further, the Mag-Amp saturation delay of 720 ns remains constant across all tested input voltages, confirming predictable and stable secondary-side regulation. MOSFET V_{DS} stress is limited to 87 V with effective snubber suppression. The implemented protection circuits (OVP, UVP, OCP) ensure safe operation during fault conditions and making the converter suitable for high-reliability spaceborne applications.

Future work may explore replacing the conventional silicon MOSFET with a SiC or GaN device to improve switching efficiency and reduce losses at higher frequencies. Additionally, in future days, the circuit can be modified using a digital controller instead of analog PWM controller IC to provide enhanced control flexibility, programmability, and real-time Hybrid Miniaturized Circuit integration for spaceborne systems.

ACKNOWLEDGMENT

Authors are grateful to the management, B.M.S Educational Trust, Principal and Vice Principal, BMS College of Engineering and Centum Electronics Ltd. for their continuous assistance and support.

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