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Design and Implementation of Router Arbitration in Network on Chip

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Abstract— In this paper we designed a reliable transmission of router arbitration for NoC router. On chip interconnection network start to play a more important role in determining the performance and power of the entire chip. Technology scaling has enabled the integration of billion of transistors on a single chip. The proposed round robin arbiter handles the situation to allot priorities to incoming to incoming inputs based on round robin arbiter algorithm used in the router, in which priorities are assigned in clockwise the request was just served should have the lowest priority on the next round of arbitration. This proposed RRA is described in verilog and we used the modelsim tool to validate the code. We analyses the average power consumption of proposed RRA approach is reduced and it provides a large reduction in occupation of area.

Keywords— System on Chip, Arbiter, network-on-chip, round robin arbiter, router

I. INTRODUCTION

As technology scaling enables the integration of billions of transistors on a chip, economies of scale are prompting the move toward parallel chip architectures with application-specific system-on-chip (SOC) leveraging multiple processing cores on a single chip for better performance at manageable design costs. As these parallel chip architectures scale in size, on-chip networks have becoming the main communication architecture, replacing dedicated interconnections and shared buses. NOC architectures have to deliver good latency-throughput performance in the face of very tight power and area budgets. These trends make on-chip network design to be one of the most challenging and significant design problems.

Network-on-chip (NoC) has emerged as flexible and suitable design approach to solve the interconnection problem for MP SoC during the last decade. NoC is a packet switched network where router nodes are used to propagate a packet from a source module to a target module. The routers can be arranged in an arbitrary topology and are connected with an arbitrary number of modules. Furthermore, a flit (the basic transmit unit in NoC's) can be propagated using different routing, switching and arbitration schemes. On the one hand, this large variety of parameters is the essence for high flexibility. On the other hand, it spans a very large design space. This makes the optimization of the interconnection infrastructure challenging.

With respect to many-core SoCs, the network-on-chip will become a bottleneck. Therefore, parameters, such as network topology, routing strategy, etc., must be investigated carefully for this next generation of SoCs Fast and flexible analytic models are necessary for a comprehensive design space exploration (DSE). The DSE usually starts with a very large design space (e.g., many different topologies, routing schemes, core mappings, etc.). That's why the design space has to be reduced iteratively by discarding alternatives with the worst performance. A high accuracy is essential to acquire reliable information for the design optimization already in an early design phase. The authors of this paper observed that existing analytic models are not able to provide a sufficient accuracy.

This is especially the case for NoC routers using the popular round-robin arbitration scheme. This arbitration scheme offers a low complexity and local fairness and is therefore used in many existing network-on-chip designs for handling best-effort traffic. The arbitration scheme has a strong impact on the whole network throughput, bottlenecks and path latencies. Therefore, it influences design decisions significantly. Wrong design decisions can lead to over-provisioning, i.e., waste of chip area. On the other hand, performance requirements may not be fulfilled, which is even worse. Thus, it is essential to employ arbitration models that offer a high accuracy

Figure 1 gives an impression of the complex traffic flow within routers. Therein, we see splitting and merging of traffic flows. Collisions can occur, which must be resolved by an arbitration algorithm, such as round robin. Furthermore, the collision resolution is dependent on the current state of the arbiter and it differs between the inputs. Though, round-robin is an apparently simple arbitration algorithm, existing analytic approaches cannot reflect the internal collision and collision resolution behavior precisely.

In this paper, we introduce an analytic service time model that is specifically designed to reflect the behavior of round robin arbiters and offers a high accuracy. Following, the service time model is used to extend an existing queuing model for NoC routers. The model provides information about the steady-state distribution of the routers. Based on this, many important network performance metrics, such as mean latencies or network throughput, can be derived.

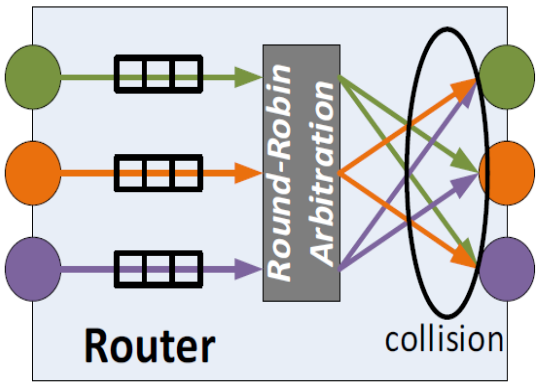


Fig 1. Collisions in routers with merge and split of traffic flows controlled by round-robin arbitration.

II. RELATED WORK

The circuits (Cnet) switched network consists of a switch which can connect any input port to any output in order to bypass some intermediate nodes and produce a shorter distance to the destination (Cnet) circuits are constructed using a light weight and high speed setup network. at each node the router split the traffic Between these two sub networks in such a way that the power and performance matrices of the NoC's improved.

According to the path search and setup methods, CS NoC's can be classified into two categories: dynamic setup methods or static setup methods. Static setup methods schedule paths at compilation time. As a result, they may not well support applications like H.264 with requirements for dynamic communication setups. Therefore, we only focus on dynamic methods which search and setup paths at run time.

Dynamic methods can be further classified into centralized or distributed methods. Generally speaking, centralized setup has two disadvantages: One is scalability and the other is dropping of failed setup requests. Since retrying of failed requests causes the blockage of the following requests, failed setup requests are usually dropped in centralized setup methods.

III. NOC TOPOLOGIES

A NoC can be characterized by the structure of the routers connections. This structure or organization is called **topology** and is represented by a graph G (N, C) where N is the set of routers and C is the set of communication channels. The routers can be connected in direct or indirect topologies.

In the direct topologies, each router is associated to a processor and this pair can be seen as a single element in the system (so-called a node in the network). In this topology, each node is directly connected to a fixed number of neighbor nodes and a message between two nodes goes through one or more intermediate nodes.

Only the routers are involved in the communication in a direct topology and the

Communication is based on the routing algorithm implemented by the routers. Most NoC implementations are based on orthogonal arrangements of the routers in a direct topology. In this arrangement, nodes are distributed in a n-dimensional space and the packet moves in one dimension at a time. These arrangements are the ones that present the best tradeoff between cost and performance, and also present good scalability.

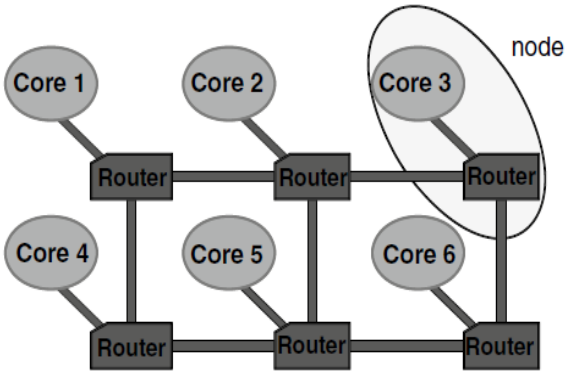


Fig 2. 2-D Grid Topology

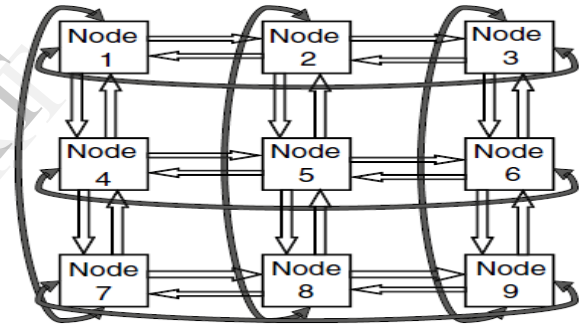


Fig 3. 2-D Torus Topology

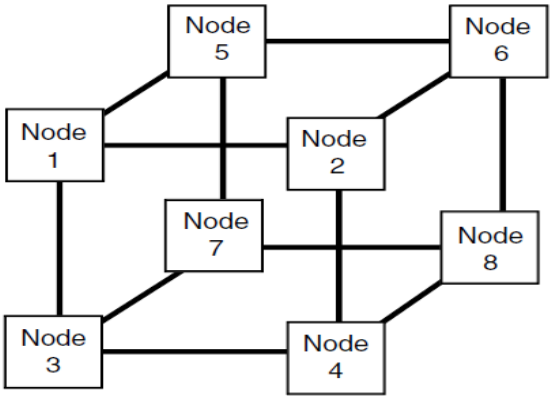


Fig 4. 3-D Hypercube Topology

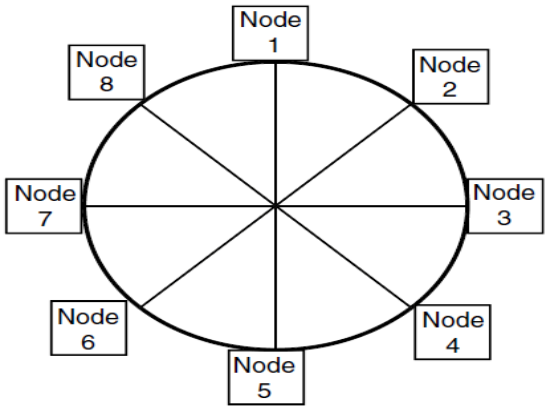


Fig 5. Octagon Topology

In an indirect topology not all routers are connected to processing units as in the direct model. Instead, some routers are used only to propagate the messages through the network, while other routers are connected to the logic and only those can be source and/or target of a message. Some topologies of indirect networks stand out: the crossbar, and the multi-stage. The multi-stage topology is a regular NoC, where routers are identical and organized in stages. Input and output stages are connected to the functional units in one side and to the internal nodes in another side

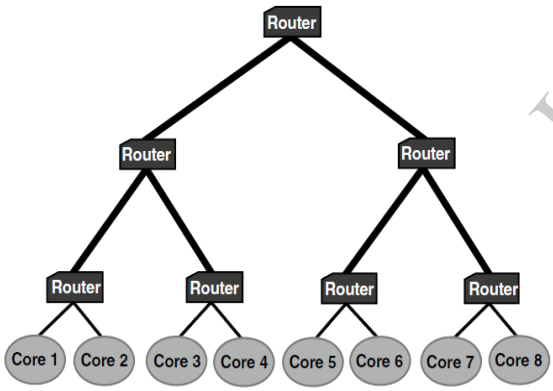


Fig 6. Fat-Tree Topology

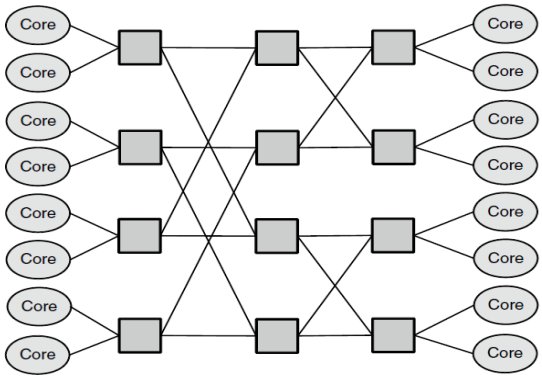


Fig 7. 3-Stage Butterfly Topology

IV. ROUTER ARCHITECTURE

In this work we have designed a Parallel router which is having Low Area as shown in the figure-1. The motivation is to reduce the area which also reduces the power consumed. We choose one of the popular methods of buffering called store and forward. The motivation behind choosing such a scheme is to have the simplest possible decoding logic, thereby, reducing both area and power. Establishment of connections is made automatically without any complex decoding logic.

A. Router Design

The router consists as shown in the figure-1 of five ports east, west, north, south and local port and a central cross point matrix. Each port has its input channel and output channel. Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port.

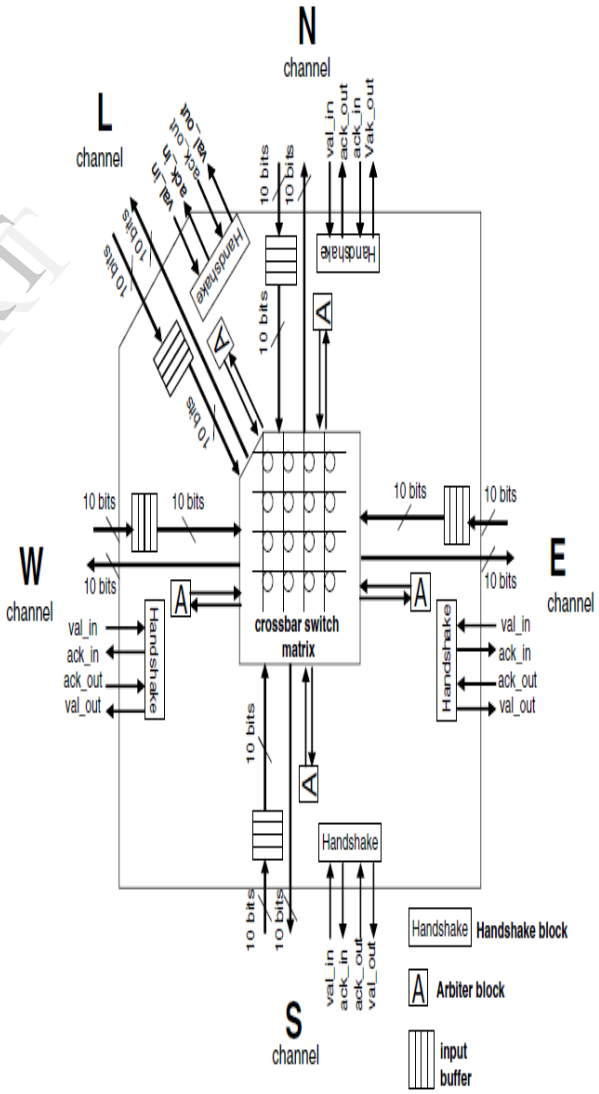


Fig 8.Router Architecture

Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily.

The buffering method used here is store and forward. Control **logic** is present to make arbitration decisions. Thus communication is established between input and output ports. The connection or configuration is made between both with the central cross point matrix. According to the destination path of data packet, control bit lines of cross point matrix are set. The movement of data from source to destination is called switching mechanism. The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 8 bits to 120 bits. The solution consists of an on-chip data-routing network generally Known as Network-on-Chip (NoC) architecture .

B. Input channel

One input channel at each port is found, each running its own control logic as shown in the figure-2. Each input channel has a FIFO of depth 16 and data width of 8 bits and a control logic which has implemented as a Finite State Machine (FSM).The input channel accepts request from other neighboring routers. On receiving the request, if it is free, it will acknowledge the request. The first flit is the header and the following flits constitute the data. It will accept the data as long as the request signal held high. The previous router's output channel ensures that the request line is held high until it empties the packet of data, being accepted by the input channel. The input channel accepts the acknowledgement line is high, as long as there is a transfer taking place (indicated by the request line).

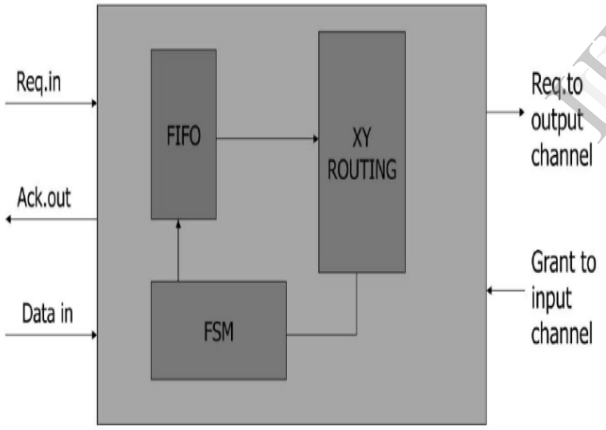


Fig 9. Input channel

The transfer being completed the request and the acknowledgement line go low in sequence. The packet of data received from the previous router is stored locally in the FIFO thereby implementing a store and forward dataflow. Next the control logic reads the header of the packet and using decides which output channel is to be requested for sending out of the router and sends the request to that output channel. It is to be noted that each of the input channel is running an independent FSM and hence can initiate five possible parallel connections at the same time. Once the input channel gets a grant from the requested output channel, the control bits of cross point matrix are set appropriately by the granting output channel.

C. Crossbar

Cross bar is a set of multiplexers and demultiplexers having an interconnection allowing all possible connection between the five inputs and output channel. The output channel while granting the request of an input channel configures the multiplexers and demultiplexers of the cooperating input and output channel thereby establishing the connection between them for the transfer of the packets.

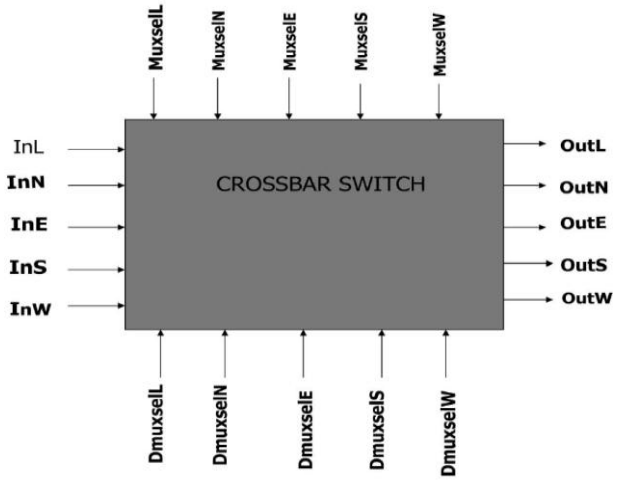


Fig 10.Crossbar switch

A crossbar switch (also known as cross-point Switch, cross point switch, or matrix switch) is a switch connecting multiple inputs to multiple outputs in a matrix manner. The design of crossbar switch has 5 inputs and 5 outputs. Fig.4 shows Multiplexer based crossbar switch. As we are getting five input packets of 40 bits each from five ports of router, number of 5:1 multiplexers used inside the crossbar are five. All five inputs are given to all the multiplexers. Select line is of Three bits. Out of five select lines which one is selected is depend on the logic of arbiter. Outputs of multiplexers are the output ports of the 5X5 router.

D. Output channel

Depending upon the mux selection the mux is working based upon request from the input channel,and based on the input corresponing output will get from the crossbar.

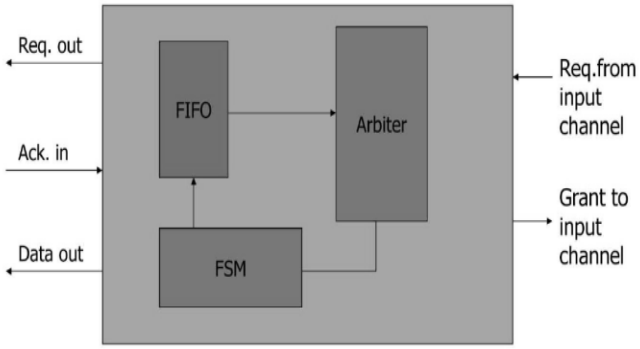


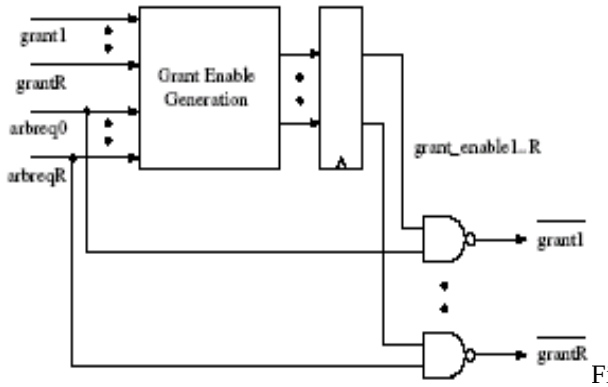
Fig 11.Output channel

One output channel at each port which has an 8 bit FIFO of depth 16 and a control logic making an arbitration decisions is found. The output channel gets request from the different input channels and grants one and sets the control bit lines of cross point matrix.

It accepts the packet into its FIFO as long as the sending input FIFO is not empty thereby providing a simple decoding logic. When transfer is complete the cross point matrix controls are reset.FSM then initiate the process to send the data into the neighboring router using handshake mechanism. Empty status of its FIFO triggers the next inter-channel transfer.

V. ARBITER

The power consumption or the area from the arbitration logic has been shown to be very minimal. However, poor arbitration can limit the throughput of the router and reduce the overall performance of on-chip networks. The latency of the arbitration logic also often determines the router cycle time. Separable allocators have been proposed for on-chip networks which separates the allocation into two stages – input and output arbitration. These allocators require an efficient matching algorithm and novel switch allocation has been proposed to increase the matching efficiency for on-chip networks. However, arbitration is still often in the critical path. Arbitration is needed since resources (such as channel bandwidth) are shared, but if they are reserved ahead of time, arbitration complexity can be reduced or removed completely. In this work, we present simplifying arbitration by giving priority to those packets already in the network that continue to travel in the same dimension – thus removing the switch arbitration from the critical path.



Figure

Fig 12.Block Diagram of Arbiter

VI. ROUND ROBIN ARBITRATION

Round-robin Arbitration (RRA) is one of the simplest scheduling algorithms for processes in Networks operation as shown in the Table 1.It is generally used to operate the time slices, assigned to each process in equal portions and in circular order, handling all processes without any priority (also known as cyclic executive). Round-robin scheduling is simple, easy to implement, and starving-free. Round-robin scheduling can also be applied to other scheduling problems, such as data packet scheduling in computer networks

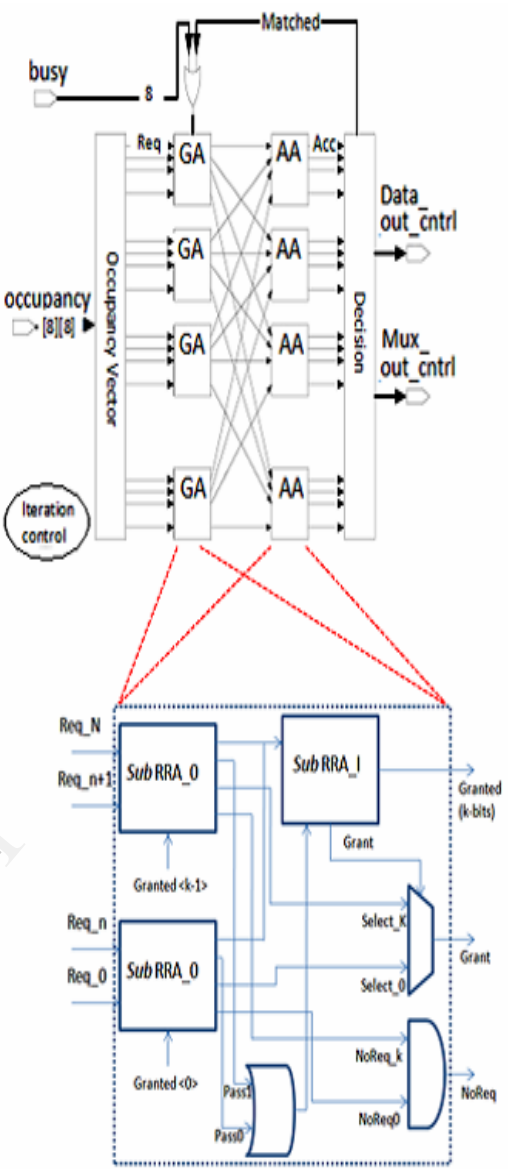


Fig 13.Round Robin Arbiter

VII. RESULTS

We use the Xilinx Spartan-3 board, which has an xc3s200 FPGA to functionally verify the standalone router and the NOC system. We use the Xilinx 10.1ISE to synthesize the system and Modelsim 6.3c to simulate the model and generate the activity data of the place and router model.

VIII. CONCLUSION

This paper proposes the implementation of round robin arbitration in router architecture of circuit switched NOCs, which influences reliable and efficient network, and the result shows the Round Robin Arbiter consumes low power and occupies smaller area in router architecture. The implantation of Round Robin Arbiter in the router architecture will take an advantage in FPGA that utilization of area power consumption is very less.

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