Design and Implementation of Reversible Combinational Circuits by Creating Libraries of Basic Gates using Verilog HDL

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***Abstract*-This paper signifies the research work on design of reversible gates and various applications of it using Verilog HDL and VHDL with Xilinx ISE version 13.1, spartan 6 FPGA. Reversible gates have the facility to generate unique output vector from each input vector and vice-versa. Irreversible gates are the circuits which have an information loss. Losing information in a circuit causes losing power. So reversible gates have a better advantage when compared to irreversible gates. Using Verilog and VHDL we are creating a library of reversible gates such as AND, OR, CNOT, NAND, NOR, XOR. Using this library, we are implementing applications such as full adder, decoder (2:4),decoder (3:8),multiplexer, fullsubtractor, comparator.**

Keywords- Reversible logic, Irreversible logic, Xilinx, Spartan 6 FPGA, Library of basic gates, Implementation of digital circuits.

I. INTRODUCTION:

Computers today terribly waste energy and storage capacity. They throw away millions of bitsevery second. These are based on irreversible logic devices, which have been recognized as being fundamentally energy inefficient for several decades.So reversible gates are the best remedies.Reversible gates are the circuits in which losses are minimized. In these circuits number of inputs will be equal to the number of outputs and there is one to one mapping between vectors of inputs and outputs. Fredkin gate, Toffoli gate, interaction gate, and switch gate are typical ones.

Full adder- Adder is a digital circuit which adds n number of input bits with carry.Adder circuits are not only used in ALUs, but also used in various processors to calculate various increment or decrement operations, addresses, etc.

Multiplexer-Multiplexer is a device which has many inputs and only one output. It selects one of several analog or digital input signals and forwards the selected inputs into a single line.

Decoder-a binary decoder is a combinational logic circuit which converts binary information from n coded inputs to a maximum of 2^n unique output. The decoders are used in analog to digital conversion in analog decoders.

Fullsubtractor- A full subtractor is a digital combinational circuit that performs subtraction n input bits, taking borrow into consideration. They are used for mathematical calculation, electronic calculators and in digital devices.

Comparator-Comparator is an electronic combinational circuit that compares n input bits and it has 3 outputs namely lesser than, greater than and equal to. They are used in devices such as ADC, Oscillators, traffic lights, etc.

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance.

- **Needand for reversible gates over irreversible gates:**

In recent times researchers have investigated various reversible logic gate and their all-feasible implementations.

Process improvements are eventually a dead end

- Energy usage will become prohibitive
- Heat dissipation will become more problematic

Classical computer dissipates a lot of energy

- Bulk electron processes

Many electrons used to do a single logical operation

II.PROCEDURE AND METHODOLOGY*:*

We are implementing applications like full adder, and multiplexer using XILINX ISE version 13.1 and spartan 6 FPGA. Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs. This tool enables the developer to synthesise their designs, perform time analysis, examine RTL diagrams, design reactions to different stimuli, and configure the target device with the programmer. Spartan 6 FGPA is a hardware kit which is used for implementation of the developer designs. This kit is easy to use and implement any complex circuit using VHDL and Verilog HDL. FPGA -

FIELDPROGRAMABLEGATEARRAY is an integrated circuit manufactured to be configured by the developer.

1. *STEPS:*

Create a new folder in D-drive
↓
Double click on ISE icon-go to file-new project-location D
↓
Project settings -family -spartan 6
Device-XC6SLX4
Package-TQG144
Simulation-ISIM
Preferred language-verilog
Next-finish
↓
Click on project-new source-Verilog module-file name-type the code
↓
Simulation -ISIM-behavioural check syntax-simulate behavioural
↓
Force constants-force a value -apply-OK
↓
Implementation
↓
User constraints-I/O pin planning post synthesis -select the pins
↓
Implement design
↓
Generate programme file
↓
Device manager-ports-VFPGA6-check the port
↓
Double click on VSF6-enter the com port
↓
Give the file used -configure
↓
Check the output in the kit

III. RESULTS*:*

A. Implementation of library

1.Toffoli AND
2.Toffoli OR
3.CNOT
4.Toffoli NAND
5.Toffoli NOR
6.Toffoli XOR

1.Toffoli AND- In and gate output goes high when both input a and b are high or output goes low.

Block diagram:

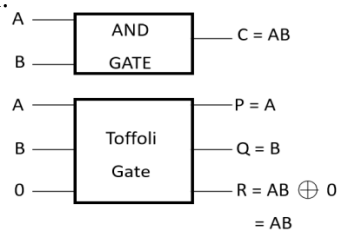

Figure 1.block diagram of Toffoli AND gate

Truth table:

Table 1.truth table of Toffoli AND gate

Input		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Waveform:

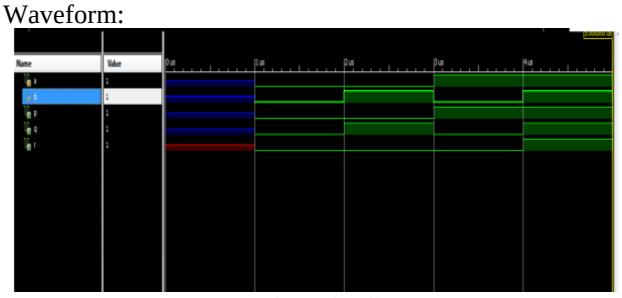

Figure 2.waveform of Toffoli AND gate

2. Toffoli OR: Gate in which output goes high when any one of the inputs is high and output goes low when both inputs are low.

Block diagram:

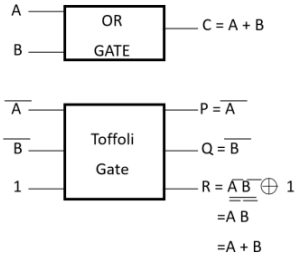

Figure 3.block diagram of Toffoli OR gate

Truth table:

Table 2.truth table of Toffoli OR gate

Input		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Waveform :

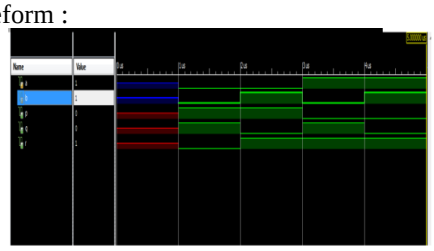

Figure 4.waveform of Toffoli Or gate

3. CNOT: Gate in which output is a compliment of input. It has only one input and output.
Block diagram:

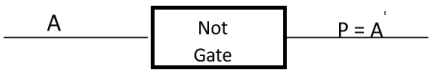

Figure 5.block diagram of NOT gate

Truth table:
Table 3.truth table of CNOT gate

A	P
0	1
1	0

Waveform:

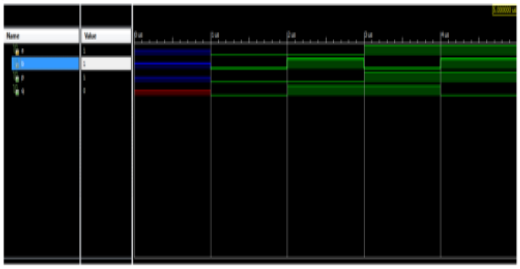

Figure 6.waveform of CNOT gate

4.ToffoliNAND: Complement of and gate.
Block diagram:

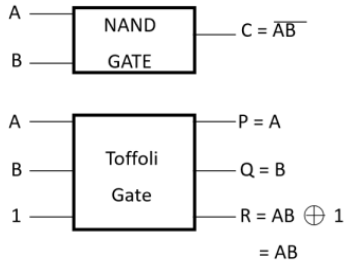

Figure 7.block diagram of NAND gate

Truth table:
Table 4.truth table of Toffoli NAND gate

Input		Output
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Waveform:

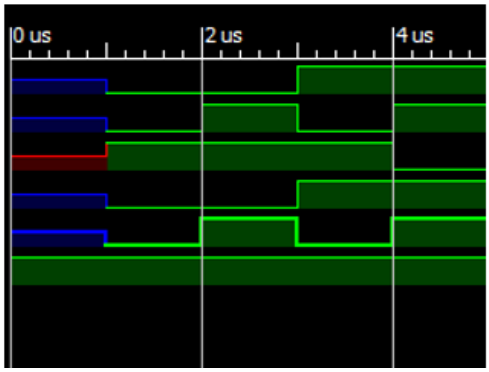

Figure 8.waveform of Toffoli NAND gate

5. Toffoli NOR: Compliment of OR gate.
Block diagram:

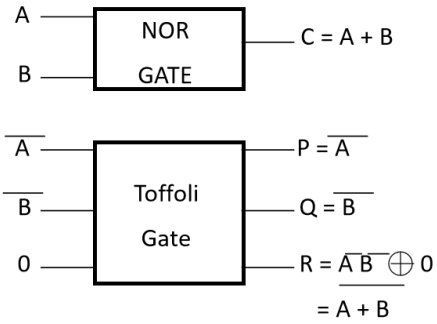

Figure 9.block diagram of Toffoli NOR gate

Truth table:
Table 5.truth table of Toffoli NOR gate

Input		Output
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Waveform:

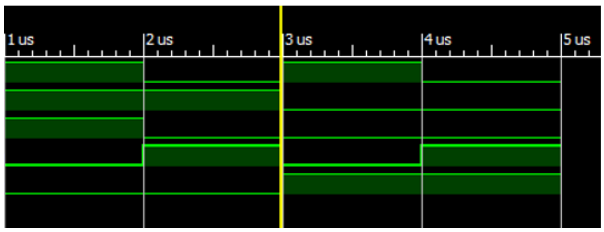

Figure 10.waveform of Toffoli NOR gate

6.Toffoli XOR: Gate in which output goes high when one of the inputs is set otherwise output goes low.
Truth table:

Table 5.truth table of Toffoli XOR gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Waveform:

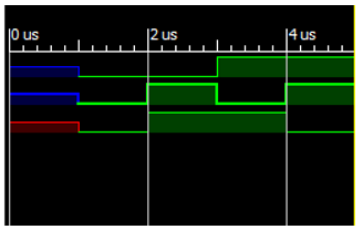

Figure 11.waveform of Toffoli XOR gate

Implementation of applications such as:

1. 2:4 decoder
2. 3:8 decoder
3. full adder
4. multiplexer
5. full subtractor
6. comparator

1. 2:4 Decoder: this reversible decoder is designed using 2 R-I gates and a pair of not gates.

Block diagram:

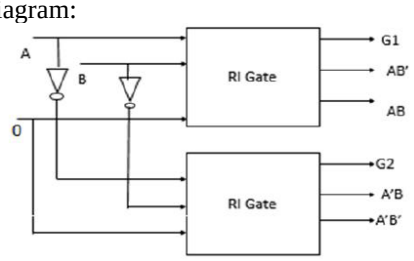

Figure 12.block diagram of 2:4 decoder

Waveform:

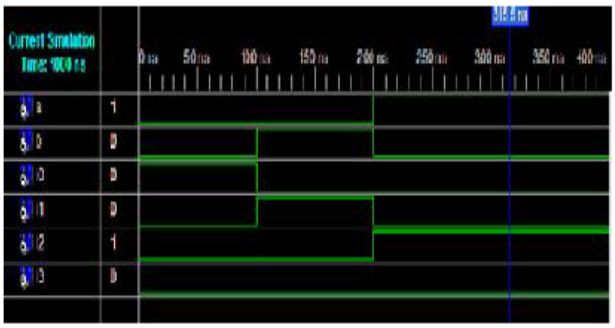

Figure 13.waveform of 2:4 decoder

1. 3 TO 8 DECODERS:

The output of 2:4 decoder id given to 4 different R-I gates such that we get 3:8 decoder.

Block diagram:

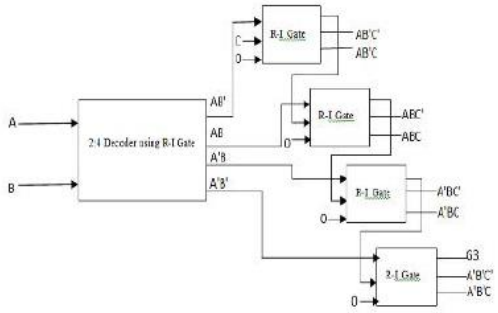

Figure 14.block diagram of 3:8 decoder

Waveform:

Figure 15.waveform of 3:8 decoder

2. FULL ADDER: It is a combinational circuit which adds n number input bits with carry. These circuits can be implemented using HDL and VHDL.

Truth table:

Table 6.truth table of full adder

Input			Output	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$Sum = A \oplus B \oplus C$

$Carry = AB + BC + CA$
$= AB \oplus BC \oplus CA$

Waveform:

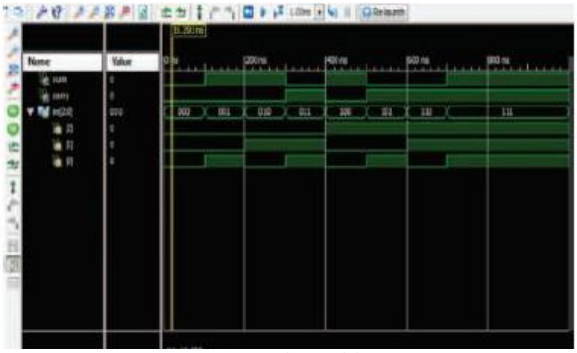

Figure 16.waveform of full adder

4. MULTIPLEXER:

The 4 x 1 multiplexer is designed using 2:4 decoder, 2 and gate and or gate. Also, each output line of the decoder is given to 2 AND gate and followed by or gate. In this we designed 2:4 decoder is designed using fredkin gate.

Waveform:

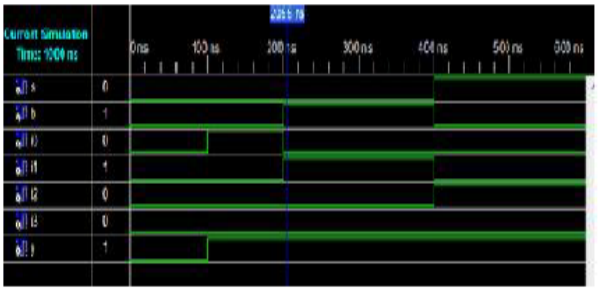

Figure 17.waveform of multiplexer

5.FULL SUBTRACTOR: It is combinational circuit that performs subtraction of two bits with borrow.

Block diagram:

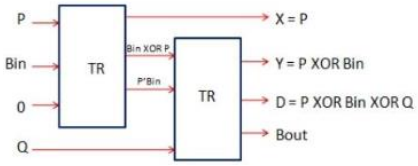

Figure 18.block diagram of full subtractor

Truth table:

Table 7.truth table of full subtractor

Inputs			Outputs	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Waveform:

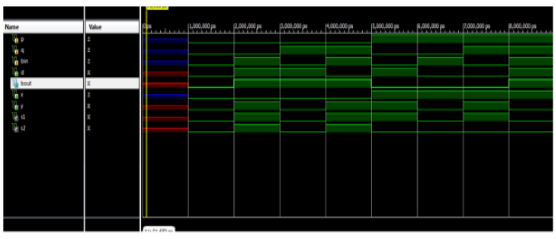

Figure 19 .waveformof full subtractor

6.COMPARATOR: It is a combinational circuit which compares given n input bits. It has three outputs such as lesser than, greater than, equal to. It isused in CPU's and microcontrollers.

Block diagram:

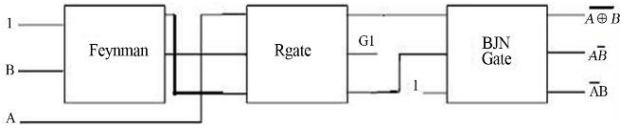

Figure 20.blockdiagram of comparator

Truth table**:**

Table 8.truth table of comparator

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Waveform:

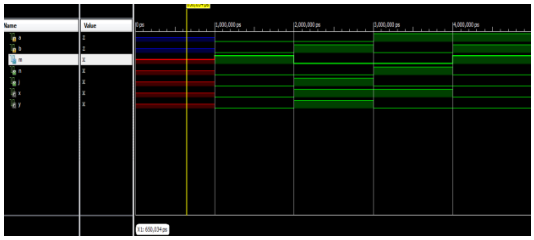

Figure 21.waveform of comparator

1.CASE STUDY*:* In recent times researchers have investigated various reversible logic gates and their all-feasible implementations.The advantages ofour method is that it is implemented at gate level and all logics used in it are simple and easy to design**.**The circuits are designed using minimal number of gates**.** The existing designs of comparator use more no of gates such as 8 to 9 TR gates in reference [9], where as we have implemented using 2-3(least)no of gates such as 1 TR gate, 1 Feynman and 1 BJN gate. As mentioned in reference [7], fullsubtractor and adder is designed using 9 gates and hence the design gets complicated for writing code and simulation. We have reduced and implemented using 3 gates in our own techniques.

II**.**FUTURE SCOPE:

This paper presents the usage of library created using reversible gates and implementing higher complex digital circuits. The paper can further be extended towards the digital design system development using reversible logic circuits which arehelpfulinquantum computing, low powerCMOS,cryptography,opticalcomputing,dnacomputing,digitalsignalprocessing,communications,computer graphics and Nano technology.

III.CONCLUSION:

In this paper, the library of reversible gates has been created such as and, or, cnot, nand, nor and xor. Using this library applications like full adder, decoder and multiplexer has been implemented. Using irreversible gates also these applications can be created but there will be a drawback of garbage outputs, high cost, energy and power losses and information loss also will be there. So reversible gates have more advantages and above-mentioned drawbacks can be minimized.

The advantages are:

- Information, like energy, is conserved under the laws of physics.
- Thermodynamics can be used to tie the irreversibility of a system to the amount of heat it dissipates.
- .Furthermore, there are evidences to suggest that reversible circuits may be built in an energy lossless way.

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