Design and Implementation of Integer-N Frequency Synthesizer using 45nm CMOS Technology

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***Abstract*—This paper proposes an inductor-less frequency synthesizer.This PLL based synthesizer uses ring oscillators for VCO. This system generates various frequencies using one reference frequencyfor attuning in communication system. An inductor based VCO has large area and low Q factor so by implementing an inductor less VCO by using ring oscillators which is a series combination of CMOS inverters, the area of the chip is optimized. The synthesizer is designed in GPDK045 library of 45nm processto operate in the range of 1 GHz to 2.3 GHz and itexhibits an in-band phase noise of -97.2 dBc/Hz with a lock time of 3.2ns.**

Keywords-Frequency synthesizer, (Phase Locked Loop) PLL, (Voltage Controlled Oscillator) VCO, (Phase Frequency Detector) PFD, (Charge Pump-Loop Filter) CP-LF, Divider CMOS ring oscillator.

I. INTRODUCTION

A frequency synthesizer (a system of frequency synthesis) provides a way for generating the array of high-stable frequencies for synchronization ofcommunication systems and support of multifrequency operating mode. The recent growth in wireless communication systems has raised the demand for more channels in mobile communication applications. As, we defined in the high frequencystandards, such as in various wireless communications which includes WiGig, WirelessHDetc., To achieve a higher data rate, complex modulations such as CSVCO (Current Starved Voltage Controlled Oscillator) is adopted, whichincreases the requirements of the oscillator's phase noise and phase error. For past few years, ithas already been demonstrated that advanced CMOS technology can realizedifferent wave ICs. CMOS implementation reduces cost and improves yield,as the RF front-end integrates with analog and digital baseband circuits.

A frequency synthesizer is also called as a PLL synthesizer. A PLL is a device which locksan output signal phase in accordance with the input reference signal phase. The signals of interest may be any periodic waveform but are typically sinusoidal or digital clock. A basic PLL is a negative feedback system that consists of a phase detector, a low pass loop filter and a voltage-controlled oscillator (VCO) as shown in figure 1.

Section II describes the components of the synthesizer. In Section III, the performance parameters are outlined. The result of the simulated study is defined in Section IV.

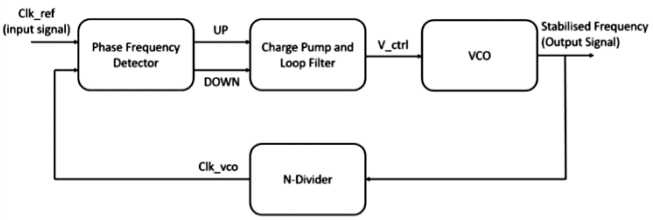

Fig.1. A Conceptual synthesizer with inductor-less VCO.

II. LITERATURE SURVEY

The author in [1] describes an architecture of the frequency synthesizer which has no inductor hence achieving an in-band low phase noise of 109 dBc/Hz. It is realized using a 45nm CMOS technology incorporating an analog noise trap to suppress the quantization noise. The design reduces the loop bandwidth, increasing the locking time by a considerable proportion.

In [2] the author talks about a system where the numerical evaluations of the response speed and the stability of hybrid frequency synthesizersare obtained. The lowest level of spurious spectral components in wireless communication systems are provided. This proposal is only achieved in a mathematical model.

In [3] author describes a design realized in 45-nm CMOS technology to suppress reference sidebands to less than -65 dBc while consuming 4 mW of power. The wideband architecture has been successfully extended to a Fractional-N loop as well. The chip size is reduced with low noise levels but the designing is difficult

In [4]author describes an in-band phase noise of 112 dBc/Hz and a reduced reference spur and power requirement suitable for wireless communication applications. It provides a lock time of 2.95 s. The design is realized using 180nm CMOS technology which is a drawback.

III. PROPOSED METHODOLOGY

A. *Phase Frequency Detector (PFD)*

Phase frequency detector is an important part of the PLL circuit. PFD is a circuit that measures the difference in phase and frequency of two signals, i.e., the signal that comes from the VCO, and the reference signal.PFD has two outputs UP(QA) and DOWN(QB) which are signaled according to the phase and frequency difference of the input signals. Figure 2shows a PFD with its inputs and outputs.

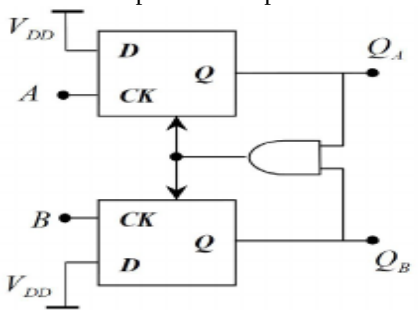

Fig .2. Detailed block diagram of PFD.

The PFD consists of two D flip flops and an AND gate. As the fig 2 showsthe D input of the flip-flops is connected to VDD and the input signals Cref(A) and cvco(B) are applied to the clock input. When one of the clocks switches to logic high, thisflip-flop will be charged and changes its output to high. The AND gate is used for preventing bothflip-flops to be high at the same time. The design of the schematic of PFD is shown in fig. 3.

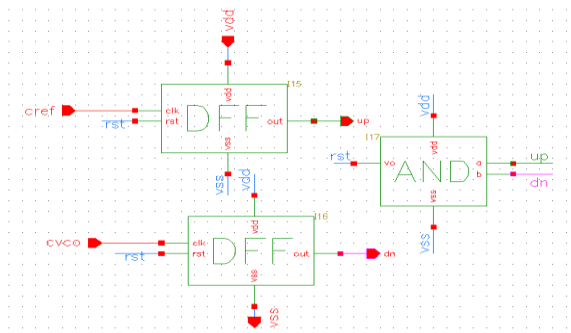

Fig. 3. Schematic of a PFD

B. *Charge Pump and Loop Filter*

Charge pump is the circuit that translates the UP and DOWN signals from thePFD to control voltage that will control the VCO. As shown in figure4, charge pump consists of two switched current sources driving a capacitive load. Charge pump is switched on and off by the PFD output signals UP and DOWN.As shown in fig. 5, the schematic of the charge pump shows the output signals UP and DN.

The design of the PLL, loop filter is crucial to the operation of the whole phase locked loop. The choice of the circuit sizes and values here is done very carefully with balanced compromise between number of requirements.

The PLL filter is used to remove any unwanted high frequency components which may pass out of the phase detector and appear at the VCO input. They would then appear at the output of the VCO, as spurious signals.

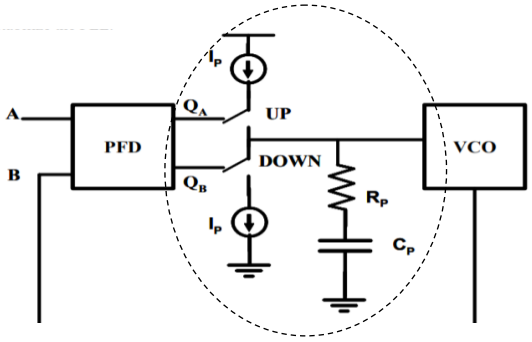

Fig. 4. Charge Pump and loop filter in PLL

C. *Ring Osciallator in VCO*

Use of LC tanks in the design of VCO (Voltage Controlled Oscillator) acquires large chip area and has low Q factor. Oscillators based on LC tanks have low frequency tuning range and the required frequency of operation may not reside in the limited tuning range as the temperature varies. Therefore, inductor less oscillators are under tremendous research.

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \quad (1)$$

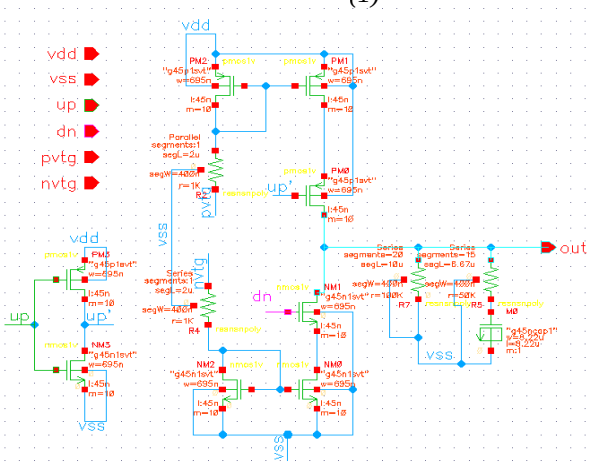

Fig. 5. Schematic of a charge pump

The use of CMOS ring oscillators is the best alternative to overcome the LC tank drawbacks. Due to the absence of LC tanks, the general Q factor considerations as per equation (1) are no longer valid. In case of LC resonators, the capacitor stores electrical energy and the inductor stores the magnetic energy. Meanwhile, some of the energy is dissipated through the resistor connected in parallel. The definition of Q factor in equation (1) does not apply to ring oscillators.

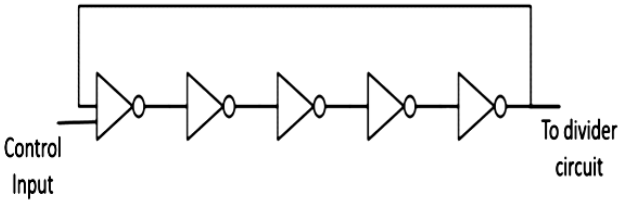

Fig. 6. Schematic of a simple 5- ring oscillator

A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false. A schematic diagram of a simple five inverter ring oscillator is shown in Fig.4.

A single inverter computes the logical NOT of its input, it can be observed that the last output of a chain of an odd number of inverters is the logical NOT of the first input. The final output is asserted a finite amount of time after the first input is asserted and the feedback of the last output to the input causes oscillation.This final output is asserted a finite amount of time after the first input is asserted; the feedback of this last output to the input causes oscillation. A real ring oscillator only requires power to operate; above a certain threshold voltage, oscillations begin spontaneously. To increase the frequency of oscillation, the applied voltage may be increased; this increases both the frequency of the oscillation and the power consumed, which is dissipated as heat.

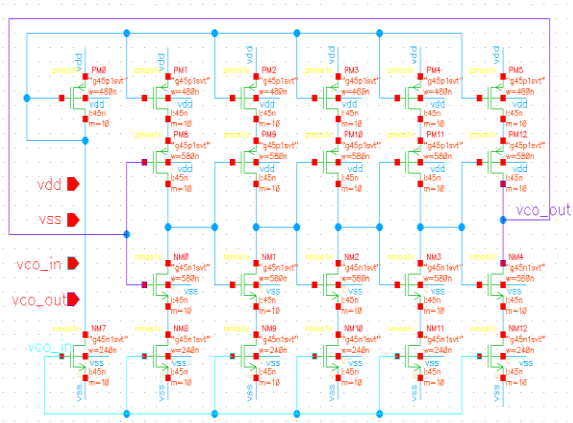

Fig. 7. A transistor level schematic of a five-stage ring oscillator

D. N-Integer Divider

It is a circuit which divides the output frequency by an integer value so that the input reference clock frequency is comparable with the VCO generated frequency. The output of the VCO is fed back to the PDF through the frequency divider circuit and forms a closed loop. Figure 8, shows the schematic of the frequency divider circuit.

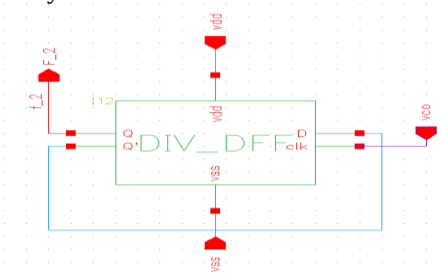

Fig. 8. Schematic of integer divider circuit

IV. EVALUATION/PERFORMANCE PARAMETERS

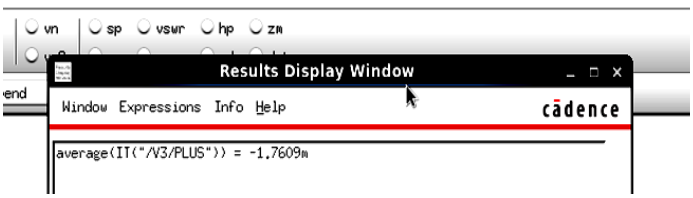

Fig. 9. Power consumption is measured to be 1.76 mW

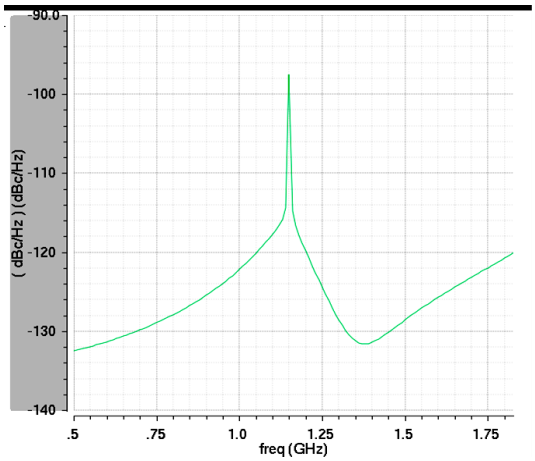

Fig. 10. Measured phase noise at 2.3GHz

The simulation result of phase noise is shown in figure 10. The phase noise of this circuit is -97.2 dBc/Hz. This was simulated using ADE L in Cadence. And the locking time of the PLL is measured to be 3.2ns at 2.3GHz using Spectre simulator in Cadence. This is shown in figure 11. The power consumption measured in the same tool is 1.76mW as shown in figure 9.

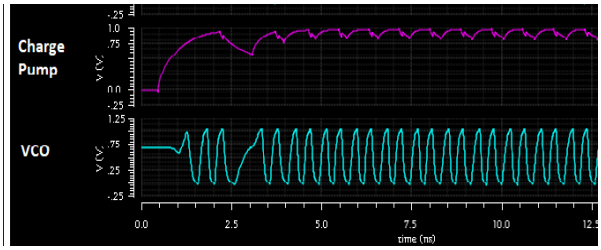

Fig. 11. Measured lock time is 3.2ns at 2.3GHz

V. RESULTS

The Integer-N synthesizer is designed in 45-nm digital CMOS technology. The die measures around 66um x 52um. It operates within the range of 1 GHz to 2.3GHz with a phase noise of -97.2 dBc/Hz, which satisfies IEEE standards. The power consumed by the whole circuit is 1.76 mW at 2.3 GHz.

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