Design and Implementation of High Precision Advanced Weighing Machine with TFT Panel

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Abstract

Now a days the demand of digital weighing machine increasing day by day in most of business enterprises because measuring the weight with digital weighing machine is user friendly with variety of various applications. This research paper shows the design and implementation of high resolution advanced digital weighing scale design based on 24-bit sigma-delta ADC along with fully featured touch controlled 5.6 inch TFT display screen, 2.4GHz wireless remote display link, RS232 link for computer attachment, RC5 remote control operation and thermal printer connectivity for billing. Basically we have carried out work that how efficiently we can use the 24 bit sigma- delta ADC and several software as well as hardware level techniques to achieve great resolution. Now a day's requirement of measuring up to 1mg, 5mg accuracy on resistive strain gauge (which is low cost) which requires highly professional work to get the stable reading at above mentioned accuracy. Providing high precision is the prime goal and with that designing user friendly software functionalities like, types of weight unit conversions, power saving operation, real time data with computers, printer for billing, 6-digit memory store and recall facilities, common calibration system, tare system etc. The main agenda we have tried to implement behind this design are low cost and complete solution of customer side.

1. Introduction

The trends to use digital weighing machine instead of classical weighing system is adopted mostly in the world and so the demand increases to design variety of advanced digital weighing machine at competitive level.

A digital weighing scale widely uses a load cell (resistive strain gauge) to measure weight. It converts pressure into appropriate voltage levels. This voltage level filtered and converted into digital data using 24-bit sigma-delta Analog to digital convertors (ADC) and processed by embedded hardware with specific microprocessor or microcontroller along with variety of applications controlled with embedded hardware.

2. Design Enhancement for Advanced System Design

All The System shown in Figure 1 shows the advanced featured digital weighing scale system with various features. This system includes 5.6 inch TFT touch controlled LCD panel to give complete GUI interface to user which is easy and more reliable for every type of users. This system has, 2.4GHz wireless remote display link helps user to remotely monitor real-time weighing data away from working site or helpful in feeding weighing data in any automatic plant operation, IR remote operation (using RC5 protocol) attached with the system to control operations of weighing scale either using touch screen or by remote control, and the most useful and necessary applications RS232 connectivity and thermal printing options are also designed.

The trends of weighing scale designers' increases towards higher accuracy and lower cost production. It will increase demand of high-performance analog signal processing at low cost. The scope of this requirement is not obvious; most weigh scales output the final weight value at a resolution of 1:3000 or 1:10000 which is easily met (apparently) by 12-bit to 14-bit Analog-to-Digital Convertors (ADC). However, a closer examination of weigh scales shows that meeting the resolution of 1:200000 is necessary for very precise measurement. This requirement is not that easily accomplished; in fact, the Analog to digital convertors (ADC) accuracy needs to be closer to 24-bits. In this paper, the main areas considered are peak-to-peak-noise resolution, RMS Noise, A/D-converter dynamic range, gain drift, filtering, and data averaging techniques.

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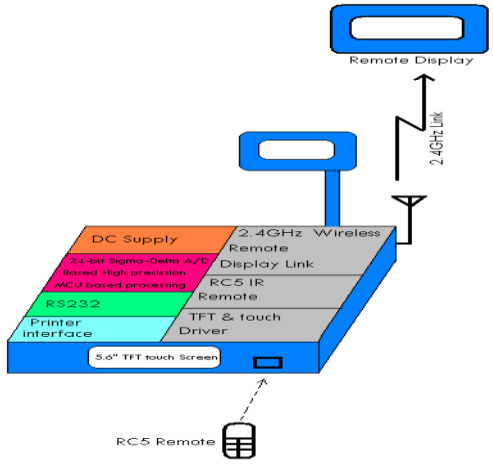

Figure 1. Advanced Digital Weighing Scale System.

3. Advanced Weighing Scale System Design

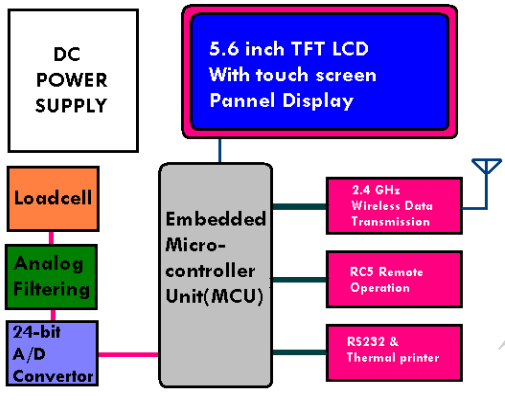

Figure 2. Hardware Block Diagram of Complete System.

3.1. Load cell sensor

The weigh-scale uses a resistive bridge type load-cell pressure sensor. The voltage output directly proportional to the pressure placed on sensor. A typical resistive load-cell sensor is illustrated in Figure 3 it contains a resistor bridge circuit of 4 – resistors with two variable arms, where the resistance vary with weight applied generates a differential voltage at a reference level of 2.5 V. Each resistance is of 350 ohm[7].

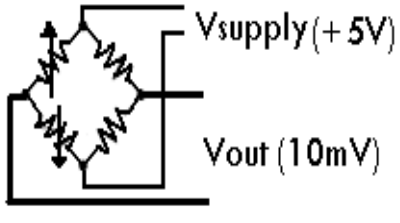

Figure 3. Load Cell Bridge Sensor[7].

3.2. Electrical Sensitivity of load cell

The load cell's electrical sensitivity is defined as the ratio of the full load output to the given input voltage. It is in mV/V unit. For example if input voltage given to bridge is +5V then at full load the output voltage is 10 mV. (If the electrical sensitivity of load cell is 2mV/V)[6]. The most linear portion of the load cell is two-third of full rated load[6]. Hence we can use only 6.66 mV as most linear output of load cell's span. The challenge thus posed is to measure small signal changes within this 6.66 mV full-scale range in such a way as to get the highest achievable performance—not an easy task in the industrial environments where weigh scales would typically be used.

3.3. Total error of load cell

The total error is the ratio of the output error voltage to the rated output voltage. A typical load cell has a total error specification of about 0.02%[7]. It is a most important parameter, because it affects the accuracy that further needs an improved signal conditioning circuit. Also it creates the complications for the choice of A/D-converter resolution, as well as the design of the low noise amplification circuit and efficient filter.

3.4. Drift

Load cell is the device which drifts its output over time which is not due to the effect of temperature. As per the experiment done on a typical load cell with a constant temperature a fixed load putted on the load cell for 24-hours the measured result using 24 bit ADC is a total drift of 125 LSBs[7].

3.5. Choice of sigma-delta analog-to-digital convertor

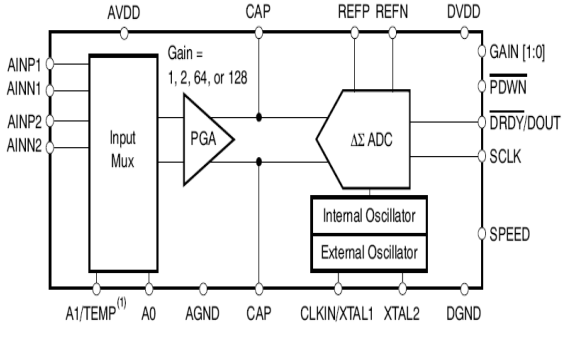

Figure 4. Internal Block Diagram of ADS1232 A/D-Covvertor[1].

The ADS1232 (Texas Instrument) are precision 24 bit, 2-channel differential input analog-to-digital converter with on chip low noise Programmable Gain Amplifier (PGA) up to gain of 128[1]. It has on chip temperature sensor to measure ambient temperature and

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communicates in SPI (Serial Peripheral Interface) mode [1].

This sigma delta A/D-convertor gives 23.5-bit effective resolution without signal amplification and is uses a 3rd order modulator and 4th order digital filter[1]. Two data rates are supported 10 or 80 SPS (Samples per Second) with both 50Hz and 60Hz rejection. Also other features like internal oscillator, on demand offset calibration, and power down mode. The most important parameters to consider when designing a weigh-scale system are *ADC dynamic range, internal count*, gain and offset drift, noise-free resolution, filtering, and *data averaging*. The system must be designed to be radiometric, hence independent of supply voltage.

3.6. ADC Dynamic range and internal counts

In weigh-scale applications using standard high-resolution ADC, the entire full-scale range of the ADC is unlikely to be used. The load cell has a 5V supply and a full-scale output of 10 mV. The linear range is only two-thirds of full-scale output i.e. 6 mV. Using a gain 128 of internal Programmable Gain Amplifier (PGA) on the front end, the ADC input will see about 768 mV full-scale. If a standard 2.5V reference is used, only 30% of the ADC's dynamic range is used. If the internal count needs to be 1:200000 resolution accuracy for the full-scale range of 768 mV, the ADC therefore needs to be of the order of three to four times better in order to meet the performance requirements. In this case, for a count resolution of 1:800000 then the ADC would require 19 bits to 20 bits of accuracy (i.e. noise-free-bits). The real practical challenge arises for the signal-processing requirement.

3.7. Gain and Offset

The Industrial weigh scale operates at a 50˚C temperature range. Manufacturers must take accuracy of the system in to account at temperatures above room temperature because gain drift with temperature can be a foremost source of error. The Offset drift is not as big a consideration. Many sigma-delta ADCs are designed with inherent chopping-mode techniques, which give the advantage of better immunity to noise and lower drift which is useful features for weigh scale designers. For example, the A/D converter has an offset drift specification of 10nV/°C. In a 20 bit system, this would contribute a total of only ¼ LSB errors over the full 50 °C operating range[1].

3.8. Noise-Free resolution

The noise of sigma-delta ADC can be specified in two ways root means square (RMS) or peak to peak (p-p). We will mainly consider peak to peak noise in our design because which helps to determine noise free bits resolution. The term noise-free-code resolution of an ADC is the number of bits actually can be utilized by programmer for system design. The resolution beyond which it is not possible to conspicuously decide individual codes due to the effective input noise associated with all ADCs. This noise can be presented as an RMS noise (in LSBs). Multiplying by 6.6 provides a reasonable equivalent peak-to-peak value[1].

Gain	RMS Noise	Peak-to-Peak Noise	ENOB	Noise-Free Bits
1	420nV	1790nV	23.5	21.4
2	270nV	900nV	23.1	21.4
64	19nV	125nV	22.0	19.2
128	17nV	110nV	21.1	18.4

Table 1. Various noise parameters of ADS1232[1].

The RMS and Peak-to-Peak noise are referred to the input. The Effective Number of Bits (ENOB) is defined as:

- $ENOB = ln(FSR/RMS\ noise)/ln(2)$[1]

The Noise-Free Bits are defined as:

- $Noise\text{-}Free\ Bits = ln(FSR/peak\ to\ peak\ noise)/ln(2)$[1]
- $FSR(Full\ Scale\ Range) = V_{REF}/Gain$[1]

3.9. Sigma-delta ADC noise performance (Test Results)

The plots of figure 5 shows test results for the weigh scale reference design. All results shown are based on the standard deviation (RMS noise) of the measured ADC output codes. To convert to "noise-free-resolution bits" we use the following calculation:

Standard deviation =RMS Noise (LSBs)
Peak-to-peak noise =6.6xRMS Noise (LSBs)
Noise in bits of resolution=log_2(p-p noise resolution LSBs)
ADC noise-free resolution (bits) = 24 – (noise in bits)
= 24 – log_2 (6.6 x RMS Noise (LSBs)) bits of resolution

The Figure 5 shows the data measured using the reference voltage same as the input to the ADC. The standard deviation (RMS noise) of the measured reference is 3.25 LSBs. multiplying it by 6.6 to find the peak-to-peak noise gives 21.4672 LSBs. So the total bits that contain noise is 4.42. Finally for a 24-bit ADC, the "noise-free resolution bits" is 19.58. Performing same operation with other typical load cell the "noise-free resolution bits" in this case is 19.4 bits. This

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concludes that the load cell itself adds only 0.2 bits of error noise in the final result.

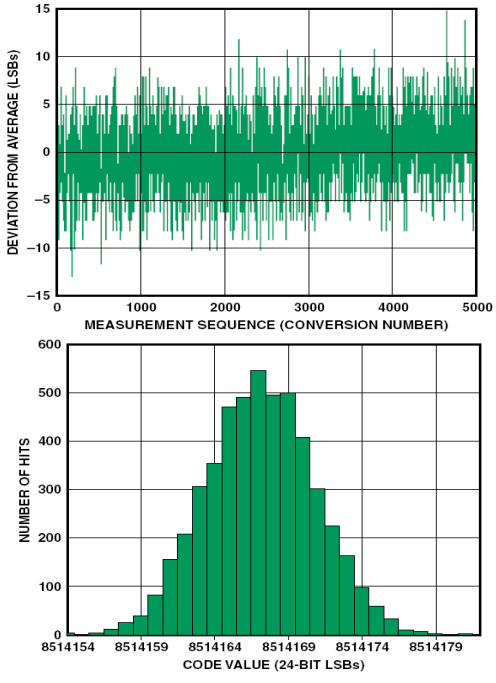

Figure 5. ADS1232 noise performance at: gain = 128, update rate = 10 Hz, reference = 5 V, inputs shorted to the reference. RMS noise = 3.2526 LSBs, peak-to-peak resolution = 19.576 bits.

3.10. Improving the ADC Results

The low-bandwidth, high-resolution ADS1232 has a resolution of 24 bits. However, the effective number of bits has the limitation because of noise, which depends on the sample rate and the amplifier gain setting used. In order to increase the effective resolution and remove as much noise as possible, the P89V51RD2 [5] microcontroller was programmed to employ an averaging algorithm to get better performance. To find noise histogram, ADC input is connected with ground and at fixed reference voltage a number of readings is being taken and plotted in a graph as shown in Figure 6. This graph shows variation in readings (variations are Gaussian in nature) at same input this is because of quantization and thermal noise in the A/D convertors.

Doing averaging of the data is a good method to reduce random white noise while keeping the sharpest step response. The software algorithm called "moving average algorithm" is implemented to improve ADC result. Algorithm shown in figure 7 it operates on most recent M data readings. The algorithm takes M inputs from ADC discard highest and smallest readings from M readings and averaged remaining M-2 readings as shown in the equation:

$$y[i] = \frac{1}{M-2}\sum_{j=0}^{M-3} x[i+j]$$

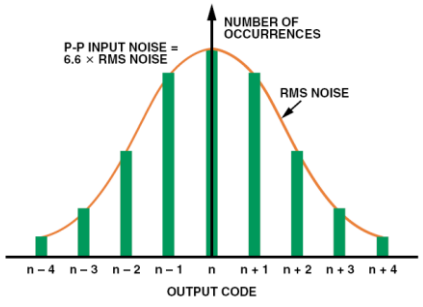

Figure 6. Histogram for an ADC Measuring a constant analog input.

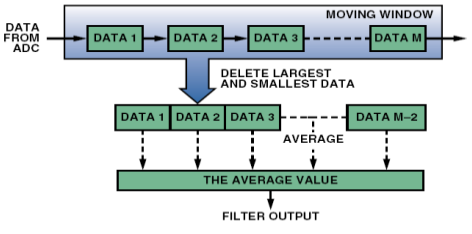

Figure 7. Moving average Algorithem.

This is the first order averaging techniques so the output data rate is same as input data rate in this filtering technique. For high update rate second order averaging is generally used to reduce waveform dispersion. In that case, the output from the first stage is averaged through a second stage to get better results.

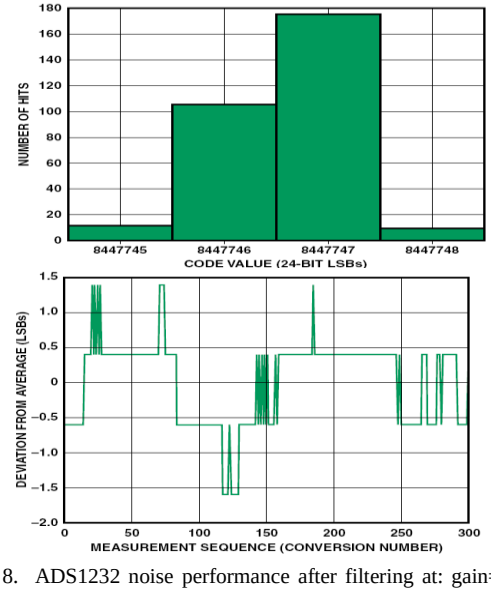

Figure 8. ADS1232 noise performance after filtering at: gain=128, update rate=10Hz, refrence=5V, RMS noise=0.611 LSBs, p-p resolution=21.9 bits.

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Figure 8 shows the measured data from the ADS1232 after averaging. The moving average algorithm adds 2.3 bits more in to noise free resolution bits. Finally the achievement of 21.9 bits of noise frees resolution instead of 19.6 bits (without averaging). This algorithm can spectacularly improve the final result. The only disadvantage of this algorithm is a higher settling time due to the channel delay of the averaging.

3.11. 5.6" TFT Touch Panel Design

5.6 inch TFT graphics LCD with attached touch panel module [9] is 640x480 pixel resolution, 16.7 Million colors, and supports RS232 or USB mode for communication with microcontroller unit. It has additional facility that will reduce the programmer's load of coding using the GUI graphics and touch design tools [9]. The design images can be created using Photoshop software and that can directly be loaded in to LCD module and we need to give the index number of each image and that will be called using serial commands.

Figure 9. 5.6 inch TFT with touch screen display pannel view.

We have designed front panel as shown in Figure 9. It shows the graphics arrangement, control buttons, weight display screen, external device control buttons like 2.4GHz wireless display, remote, RS232, print bill etc.

3.12. 2.4 GHz wireless display link circuit design

This is an FSK Transceiver module, which is designed using the Chipcon IC (CC2500)[3]. It is a single chip transceiver. It communicates serially with 3-wire SPI protocol and it has Locked Loop (PLL) for tuning. It can be useful to use in NRZ, UART, and Manchester encoding and decoding. It gives high performance and low cost solution. It gives 30 meter range with onboard antenna. In a specific system, this module will be used together with a microcontroller. It provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication and wake on radio. It can be used in 2400-2483.5 MHz ISM/SRD band systems. The circuit is designed with features like low power consumption, Integrated bit synthesizer, integrated IF and data filters, high sensitivity (104 dBm), reliable distance transmission, programmable output power (-20dBm to +1dBm), and operating voltage 1.8V to 3.6V[3].

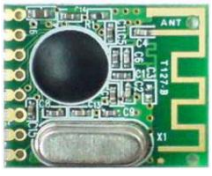

Figure 10. 2.4GHz Transreceiver module[3].

The circuit shown in Figure 11 designed with features like FSK (Frequency Shift Keying) technology, half duplex mode with automatic switching between TX and RX mode, adjustable data rate (1.2 to 500 kbps), and error checking of data using CRC (Cyclic Redundancy Check) inbuilt.

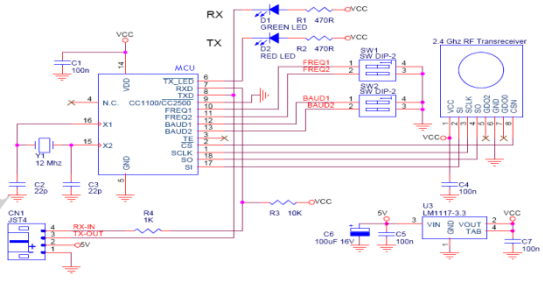

Figure 11. Circuit designed for 2.4GHz wireless remote display link.

The communication protocol is completely user transparent and automatically controlled. This circuit will be connected with weighing scale MCU (Microcontroller Unit)[10] board to establish 2.4GHz wireless link for remote display.

3.13. Infrared RC5 decoder for remote control

The RC5 protocol[5] uses Manchester coding of a 36 kHz IR carrier frequency. A protocol frame contains 14 bit with each bit of time period 1.778ms. The logic "0" and "1" can be represent as shown in figure 13 with burst frequency of 36 KHz. The main reason to use this type of logic for "0" and "1" is to reduce transmission power consumption.

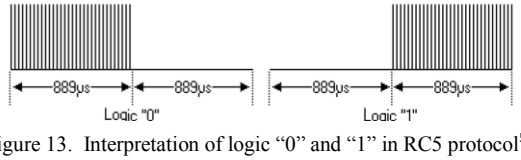

Figure 13. Interpretation of logic "0" and "1" in RC5 protocol[5].

The first two pulses are the start pulses, and both at logic high "1". Here it has to be noticed that half of a bit time is over before the receiver will detect the real start of the message. The 3rd bit is a toggle bit which

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will be inverted every time a key is pressed and released. This is the way the receiver can differentiate between a key that remains down, or is pressed repeatedly. The next five bits as shown in figure 14 shows the address of IR device (MSB first) and the next 6 bits contains command (MSB first). The total message contains 14 bits and time required to transmit one frame is 25ms[5].

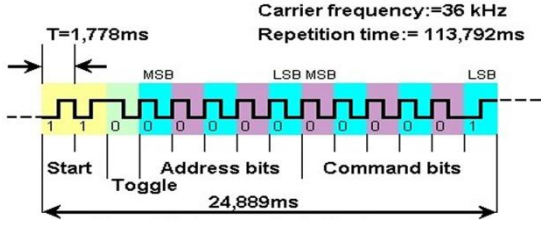

Figure 14. Bit format of Command and Address transmittion in RC5 protocol[5].

3.14. RS232 data link for computer application

RS232 is the standard protocol to communicate with computers. MAX232[4] is an integrated circuit , which converts signals from TTL voltage levels to signals suitable for RS232 and RS232 signals into TTL voltage levels from a single + 5 V supply via on-chip charge pumps and external capacitors[4]. The MAX232 makes possible to design a complete system on single voltage power supply and no needs extra power supply for RS232 conversion.

4. Software Implementation

4.1."Main" function flowchart

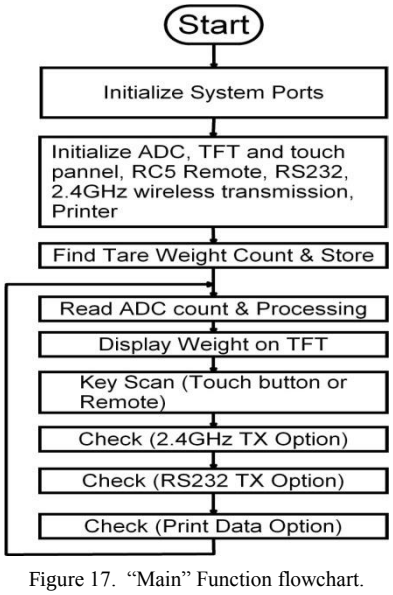

Figure 17. "Main" Function flowchart.

4.2. Improving the response time to weight change

The basic averaging algorithm can improve the result against noise, but it has a problem when the weight is changed from input slightly. When the weight change, the output of the load cell should move to a new balanced state in a short time. As per the algorithm, the output of this designed filter can only indicate the exact result after the filter refresh M times. The response time is limited by the number of averaging points. A typical algorithm is design to judge the change of the weight. Figure 18 and figure 19 show the flowchart of this algorithm.

All the *M* readings of the second-stage will be filled with the same new data for skipping the transition period of the load cell very fast after weight change. Also, the load cell has its settling time. For compensation of this, when a weight change is detected after that all the data in the averaging moving window will be filled with the newest ADC data for the next six continuous cycles of averaging to pass the recovery time. After the six cycles of refreshing, the averaging will be continue.

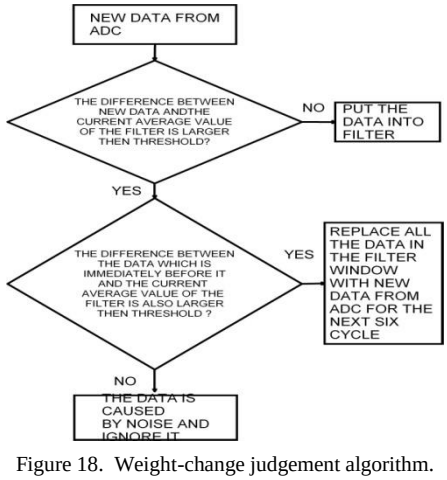

Figure 18. Weight-change judgement algorithm.

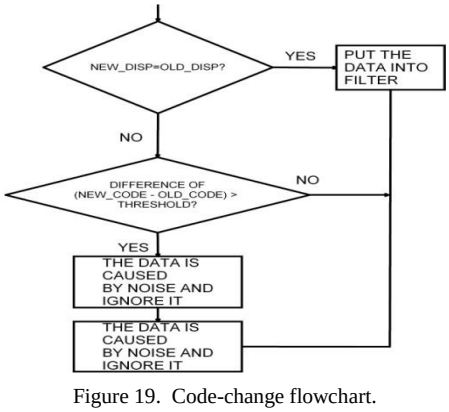

Figure 19. Code-change flowchart.

The complete software is designed in C language using Keil C51[2] compiler with 8-bit microcontroller,

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for TFT Panel graphics designing accomplished with Photoshop CS2 software, For GUI programming designed with DWIN toolbox for TFT & Touch panel programming.

5. Hardware Implementation

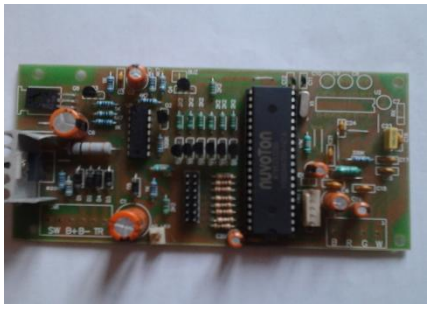

Figure 20. Designed main processing board for weighing scale "front view".

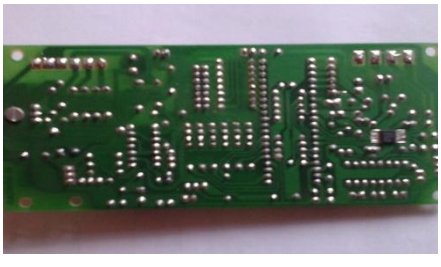

Figure 21. Designed main processing board for weighing scale "back view".

Designing hardware PCB we have used UCAM software [8]. Several precautions are taken to reduce interference of noise to the 24-bit ADC for accurate result. Proper power supply design as well as grounding is provided for proper result.

6. Conclusion

By doing this work we experienced that it is tough task to get good result with 24-bit Sigma-Delta ADC under certain noisy circumstances. We need excellent knowledge of analog signal processing, PCB designing, very good command over coding etc. We achieved resolution of 1:800000 internal counts and 1:200000 external counts. With the help of this it is possible to design very high precision weighing scale at low cost. This paper also deals with 5.6" TFT panel which is new in weighing scale area. The features included in this design also compatible with many industrial applications.

7. References

[1] Texas Instrument's website, www.ti.com for the datasheet of ADS1232.

[2] KEIL an ARM company's www.keil.com for the C compiler and programming support.

[3] ITexas instrument's, website www.ti.com for 2.4GHz wireless module design using chip CC2500.

[4] Maximum semiconductor's www.maxim.com for MAX232 IC datasheet.

[5] Philips Semiconductor's website www.philips.com for RC5 protocol standard information, and for the datasheet of P89V51RD2 microcontroller.

[6] "ALTHEN Sensor" for load cell specification, www.althensensors.com . M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

[7] Load cell specifications on the website, www.loadcells.com/Load-Cells/Load-Cell-Overview.html

[8] PCB desigining UCAM software information www.ucamco.com/en-us/products/pcbsoftware.aspx

[9] For touch screen TFT design "DWIN" company in china presented toolboxs, photoshop CS2 for image design.

[10] Data sheet from www.microchip.com for PIC microcontroller for 2.4GHz protocol implementation.

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