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Design and Implementation of High Performance DDR3 SDRAM controller

Mrs. Komala M[1]
Research Scholar
Jain University, Bangalore
india

Suvarna D [2]
PG Student(M.Tech)
SJBIT,Bangalore
Karnataka, india

Dr K. R. Nataraj[3]
HOD, Dept. of ECE
SJBIT,Bangalore Karnataka,
Karnataka, india

***Abstract*—Synchronous DRAM comes under the family of non-volatile memory technologies which are contain a unique features like low latency and large density of storing data. DRAM is also reduces the area because of flexible architecture and it contain unique capability to perform large data sets. Compared to flash and disk the DRAM is more flexible, it requires less power to each and every set of data operation and gives high speed of operation.DDR3 SDRAM or double-data-rate three synchronous dynamic random access memories is a random access memory technology used to enhance the writing and reading speed of working data of a digital electronic system.**

Here we introduced an FPGA based system to overcome earlier problems which we have faced in other technologies of NVM. This system executes application specific operation using non-volatile DRAM controller architecture and to appraise its performance using DDR3 SDRAM technology.DDR3 come under SDRAM family of technologies and DDR3 SDRAM is the 3rd generation of double data rate memories. DDR3 SDRAM gives lower power consumption and high performance compare to earlier generation.DDR3 SDRAM is a higher density device and having flexible architecture and achieves higher bandwidth, low latency and due to "fly-by" routing signals it reduces routing constrains in architecture of SDRAM instead of low skew tree distribution. If DDR3 SDRAM which interfaces with external circuit which gives maximum speed up to 400 MHz /800 Mbps in devices. The design is simulated and synthesis in Xilinx ISE and virtex 5.

Key words- Storage system, DDR3 SDRAM, NVM, FPGA, Virtex 5.

I. INTRODUCTION

With the current scenarios of big data, workloads in data analysis are largely influenced by difficulties associate with memory storage, hence everyone is looking for emerging technology i.e. DDR3 SDRAM which is very fast and byte-addressable non-volatile memory(NVM) technology and it has additional advantages like low power consumption and higher density as process technology scales.DDR3 SDRAM devices runs at 1.5V and achieves high speed operations.DDR3 memory devices are reduces 30% of power consumption compared to DDR2. DDR3 SDRAM is an improved and enhanced version of DDR2 SDRAM family. DDR3 is primarily suitable for I/O data transfer at eight times at the rate of data memory cells or stream over a large data structures. Thus DDR3 enables higher data bus rates and higher range then the previous technologies. It allows 512 megabits to 8 gigabits of data on chip and it can enable maximum memory module size up to 16gigabytes.

DDR3 SDRAM is also containing a similar technology which has present in SDRAM principles. So there are a few differences between DDR2 and DDR3 SDRAM's. Due to increase in the doubling of the data prefetch rate, the frequencies of DDR3 memory much greater than that of DDR2, Where the data is moved to the input output buffer from info storage device. DDR2 SDRAM technology uses 4-bit samples of data, DDR3 SDRAM technology uses 8-bit samples of data which is increases prefetch in memory storage i.e. also known as 8n-prefetch. DDR3 SDRAM technology which increases the internal bus width rate by twice between input/output buffer and the actual DRAM core compared to earlier technology [2][4]. It results, the efficient data transfer rate of DDR3 SDRAM is increases and the buffers which are placed externally start working faster and it is in depended of memory core. The actual DDR3 input/output buffers and the core frequency of the external storage device bus is appears 8 times higher than that of memory chips, and this storage device frequency was 4 times lower than that of the external bus So, without changes or improvements of semiconductor manufacturing process we can achieve almost accurate hit which is higher than that of actual core frequencies in DDR3 memory compared to DDR2 SDRAM.

DDR3 SDRAM controller architecture mainly consists of write data FIFO, read data FIFO reg, address FIFO, Command_FIFO, clock counter and refresh counter, initialization_fsm, command_fsm, data path, bank control. Here we designed a DDR3 SDRAM controller architecture using system Verilog and verified using FPGA kit.

DDR3 SDRAM has few advantages over a DDR2 SDRAM they are

- Higher speed
- Master reset
- Lower power
- More performance
- Larger densities
- Modules for all application

II. BACKGROUND AND MOTIVATION

In the recent few years, for all types of computing system the basic unit of memory storage is disk. Disk are highly suitable for all type of computing system but also has some drawbacks like low latency and low bandwidth, in main memory storage and system processor. Disks contain limited

write duration and it has some other drawbacks such as long write latency and high energy writes. In DDR SDRAM family of technologies contain special software and hardware enhancements such as selective writes, hybrid memory, new row buffer design architecture, write buffers to overcome earlier technology limitation and it is suitable for charge based memory such as SDRAM.

A. SDR

SDR SDRAM (Single Data Rate synchronous DRAM), is comes under first generation of memory technology and SDR is slower than that of DDR family because per clock cycle only one word of data is transmitted (single data rate). But earlier technologies such as EDO-RAM and FPM-RAM are very slow than that of SDR SDRAM. These memory technologies, each time it took 2 to 3 clock cycle to transfers one word of data.

B. DDR2 SDRAM

DDR2 is the 2nd generation of double date rate memory. By expanding bandwidth of data which increases the DDR2 data transfer rate and also by increasing core frequency of external memory which is faster than that of main memory compared to external buffer, by doubling the prefetch buffer data rate. DDR2 is having pin configuration of 240 pin DIMM (dual in line memory module) design that operates at 1.8 volts. DDR2 DIMM sockets increases the data bandwidth and performs fine memory application. The higher frequency of data transfer will take place at lower voltage. DDR2 is contain a pin configuration of 240 pin DIMM design [1] [3] and DDR has a pin configuration of 188 pin DIMM and it runs at higher voltage of 2.5 volts compared to DDR2.

Each and every system devices has a different and unique motherboard sockets, even DDR2. And these motherboard sockets designed for particular features which exist in design architecture and these are not fit for other designs like DDR technology motherboard sockets. If the DDR2 is forced into the DDR socket it will get damage and once memory will get damage than it doesn't has any protection shield to the high voltage level. In earlier technology the data was suffers from low bandwidth, high power consumption because of high energy writes and limited write duration compare to DDR3 SDRAM.

DDR3 SDRAM controller architecture is motivated by desire to retain the conventional memory storage technology to overcome those issues which are faced in previous memory storage technology. DDR3 is primarily suitable for I/O data transfer at eight times the data rate of the memory cells or stream over a large data structures. Thus it enables higher bus rates and higher peaks than the previous technologies. It allows 512 megabits to 8 gigabits of data on chip and it can enable maximum memory module size up to 16 gigabytes. DDR3 SDRAM devices runs at 1.5V and achieves high speed operations.DDR3 memory devices are reduces 30% of power consumption compared to DDR2.

III. DDR3 SDRAM CONTROLLER

DDR3 SDRAM also fallows the same principles which are present in SDRAM family of technologies. This architecture allows doubling of data rate by expanding bandwidth of data and without having any change in clock rate it increases the data rate of external bus for internal operations, and the width of a clock. It achieves 800-1600 M transfers/s, and the internal RAM array has to perform 100-200 M fetches per second.

Usually DDR family memory chips are highly useful in market which are being made for commercial purpose, and DDR3 memory chips are modified version of DDR2 memory chips which are highly advanced compared to previous memory chips. The initial clock rate of DDR3 is 400 and 533MHz and it increased the buffer size to 8bit for prefetch operation. This gives rise to increased operating frequency which resulting in high data transfer rate for internal operations. DDR3 SDRAM which runs at 1.5 V for transferring data from memory chip and to counter or prevent the heat effects of chip which are produced from high frequency of data operations by lowering the voltage. The DDR3 architecture contains pin configuration of 240 pins, but the position of the notched key is at different position to avoid the insertion into a motherboard RAM socket designed for DDR2 because these two devices are contain similar features and both devices are compatible with each other by mechanically and also electrically. It contain special feature like memory reset option, high frequency and lower applied voltage which was not present in previous version. The memory is erased by using software reset action. This option is not available in earlier technology they were cleared the memory only when after the system reboot will take place. And the memory reset features specifies that the memory chip will be empty, it indicates that the system is more stable. It also contain special memory key notches which are present at different location in a motherboard [2] [4].

Table 1: Comparison between DDR2 and DDR3

	DDR2 SDRAM	DDR3 SDRAM
Data transfer rate	400-800Mbits/s	800-1600Mbits/s
Voltage	1.8 V±0.1V	1.5V±0.075V
Banks	4/8	8
Prefetch	4 bits	8 bits
Burst Length	BL= 4,8	BL =4,8
Topology	Conventional T	Fly-by
Chips packaging	60 BGA for×4/×8	78 BGA for×4/×8
	84 BGA for×16	96 BGA for×16
Chips capacity	256 Mbit -4Gbit	512 Mbit -8Gbit

3.1 ARCHITECTURE OF DDR3 SDRAM CONTROLLER

Fig 1 shows the architecture of DDR3SDRAM controller consists mainly consists of write data FIFO, read data FIFO reg, address FIFO, Command_FIFO, clock counter and refresh counter, initialization_fsm, command_fsm, data path, bank control. To initialize the modules present in the design architecture by using initialization_fsm signal this propagates proper i-state to perform particular action. And to perform the normal read write, high write and high read operations by using command_fsm signal, this propagates c-state for

particular action. Data latching and data dispatching is done by using data path modules from external circuit unit to memory banks of DDR3 SDRAM vice versa. To open the exact bank and exact address location in that bank, here the DDR3 SDRAM bank management system uses the address FIFO, this gives an address to the command_fsm so that the bank control unit can do this particular operation. the Write data FIFO provides the data to the data path module In the case of normal write and fast write operation. The read data reg gets the data from the data path module normal and high read operation. The DDR3 controller gets the address, data and control from the external circuit in to the Address FIFO. Write data FIFO and control FIFO respectively [8] [9].

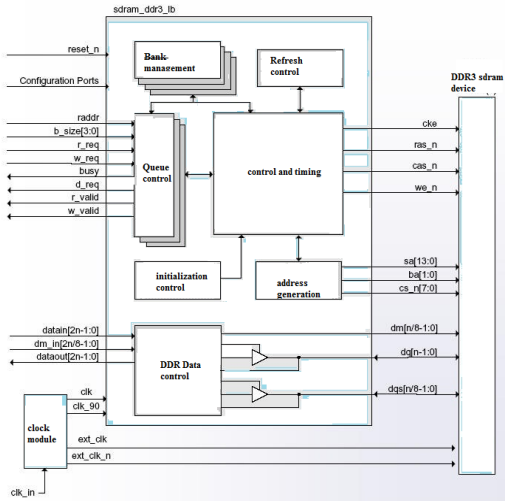

Fig 1: DDR3 SDRAM controller block

3.1.1 ADDRESS FIFO

Address FIFO gives the address which is specified from the address generator to a DDR3 SDRAM controller, this performs the read operation from the memory and also it writes the data into the memory were the address location has specified. Address FIFO has a width of 13 bit and depth of the register in the stack is 8.

3.1.2 WRITE DATA FIFO

Write data FIFO gives signals to the controller for a particular write operation; this writes a data into a memory address which are specified by the address FIFO. Here the address FIFO having a width of 64 bit and depth of the register in the stack is remains same i.e. 8.

3.1.3 COMMAND FIFO

Command FIFO gives command to the controller to carry out read operation from the memory and also it writes the data into the memory to the specified address location. These are controlled by address FIFO. Control FIFO has a width of 2 bit and depth of register in stack is 8. In controller architecture the command FIFO carried out some operations they are, 1.When 01 signal gives to the controller from the command FIFO which executes the normal read operation.

2. If 10 signal gives to the controller which executes the write operation. 3. If control signal is 11 then it executes fast read operations [6].

3.1.4 READ DATA FIFO

Read data FIFO gets the data send to the external circuit when DDR3 controller performs Normal read or Fast read operation.

3.2 FINITE STATE MACHINES

DIFFERENT STATES OF INITIAL FSM:

- Before going to read or write process we must be initialized the DDR3 memory.
- Memory must be in IDLE state after the initialization of DDR3.
- Refresh is done continuously using refresh logic.
- To open and closing the rows the pre-charge must be done after refresh.
-According to the priorities the commands are performed
-After all these command performance the memory must brought into IDLE state.

3.2.1 IDLE:

When system is in idle the reset is applied the initial fsm is forced to IDLE state irrespective of which state is remains idle without performing any operations.

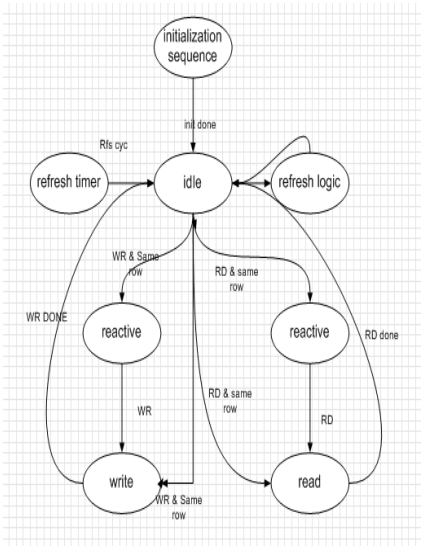

Fig 2: different states of FSM

3.2.3 REACTIVE:

Here the controller needs a command such as REACTIVE which is used to disable particular open row in the exact bank or open row in all bank locations. The input selects such as BA0, BA1, selects the bank, and the particular A10 input selects whether a single bank is reactive or whether all banks are reactive[4][7].

3.2.4 AUTO REFRESH:

During normal read and write operations, we keep on refresh the analog circuits to avoid the leakage in DRAM by using AUTO REFRESH signal. Before refreshing control pin in DRAM an AUTO REFRESH command is issued in that time all bank present in the system must be idle.

3.2.5 BANK MANAGEMENT IN DDR3:

Bank management system which handles the banks present in the DDR3 memory or stacks, here memory has divided into 8 banks in DDR3 to store the particular written data. The bank selection is carried out by bank selection inputs such as BA [0:2] signal. Selection of bank is as shown in table 2.

Table 2: Bank Selection

BA[0:2]	BANK
000	BANK0
001	BANK1
010	BANK2
011	BANK3
100	BANK4
101	BANK5
110	BANK6
111	BANK7

IV. RESULTS

Fig 3, 4, 5 shows the snapshots of the simulation results of DDR3 controller in various modes of operation. Simulation and synthesis of the design is done by using "Verilog HDL" language in Xilinx virtex 5 FPGA XC5 VLX50T+ 113 series kit.

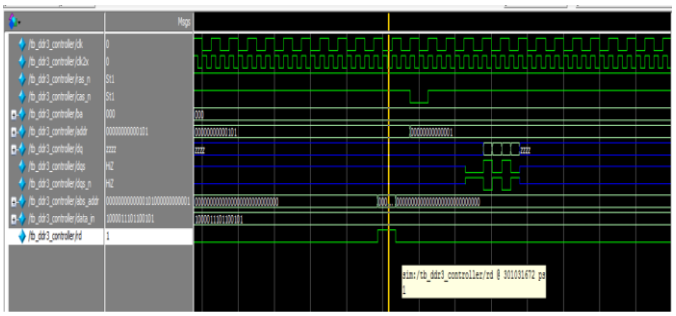

Fig 3: Results of simulation in refresh logic mode.

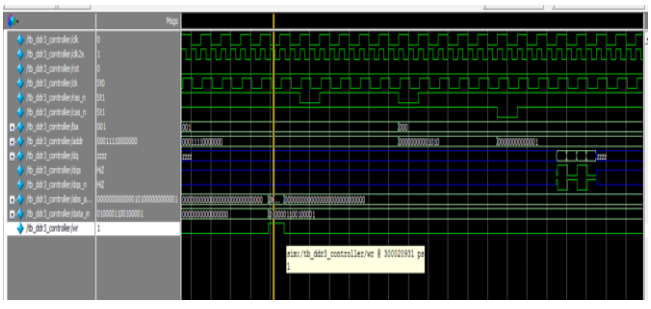

Fig 4: results of simulation in write mode.

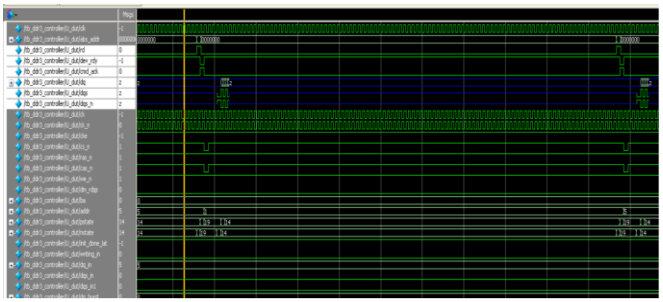

Fig 5: results of simulation in read mode.

4.1 POWER ANALYSIS

Using XPower analyzer tool, here the tool will analyzed the dynamic power consumptions and power leakage in the circuit. Dynamic power can analyze using two methods such as clock gating and without clock gating as show below.

4.1.1 With Clock Gating

Table 4: with clock gating

Vin	1.2v
Frequency	200Mhz
Supply power	0.138W
Dynamic power	0.077W

4.1.2 Without Clock Gating

Table 5: without clock gating

Vin	1.2v
Frequency	200Mhz
Supply power	0.138W
Dynamic power	0.080W

Based on the data switching operations the power analyzer tool will analyzes the power, which is taken inside the DDR3 memory controller. From the above table we can say that, by using clock gating, there is a significant reduction in dynamic power compared to without clock gating i.e. 0.080W to 0.077W. During simulation only once in an operation the device will enter into a sleep mode to avoid the data collision between them.

V. CONCLUSION

In this paper high performance DDR3 SDRAM memory controller for computing system using virtex 5 FPGA XC5 was designed and implemented. DDR3 SDRAM controller gives adequate hardware and software compatibility to provide efficient code for offload applications to get advantages of high bandwidth and fast performance on switching operation from the storage array. DDR3 SDRAM controller is designed using system Verilog simulation and synthesis is done by using Xilinx Virtex 5 FPGA XC5 VLX50T+ 1136 series kit. Using XPower analyzer tool, here the tool will analyzed the dynamic power consumptions and power leakage in the circuit. DDR3 SDRAM devices runs at 1.5V and achieves high speed operations.DDR3 memory devices are reduces 30% of power consumption compared to DDR2. By using DDR3 SDRAM controller architecture we can reduce power from 0.080W to

0.077W and also it improves heat generation, gives high memory configurations for storing higher capacity of data.

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