

Design and Implementation of FPGA Router using Virtual Cut-Through Switching Technique

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Abstract–This paper presents design of a router in FPGA. Now a days, the routers which are available in the market these are having a fixed format of software. In other words, the packet format, the switching technique and source to destination path this all the data is available in fixed format. Hence, our goal is to design a reprogrammable router which can accept any type of modifications at user end. For packet transfer we are going to use Virtual cut-through switching technique. This technique has large data transfer speed, lower latency, higher bandwidth utilization capability among all other switching techniques.

Keywords - FPGA,Router, reconfigurable, virtual-cut through, Switching technique.

I. INTRODUCTION

Parallel processing is a technique for improving the performance of computer is becoming increasingly widespread. The work involve in computation is divided into separate form. These parts can be computed in parallel, allowing the overall computation to complete in short time [1].The switches or routers control the path a message takes through channel as it travels from source node to destination node. The use of network increases the communication bandwidth of parallel computer therefore many messages can be sent simultaneously using different channels. There are number of possible ways that FPGA's could be used for this router design or other designs without waiting for technology improvements. If we are waiting for technology of FPGA and synthesis tools then these are not practical so instead of that the design can be changed. Field-Programmable Gate Arrays are designed to provide exactly these sorts of capabilities. They are intended to provide the benefits of custom CMOS VLSI design while avoiding the associated design overhead time including initial engineering cost and inherent risk. Because they can be reprogrammed an unlimited number of times, they can be used in designs where the hardware is changed dynamically or where it must adapt to different applications. The low initial cost and high adaptability of an FPGA make it easy for implementing a router for small research computers, computer that are likely to undergo large amount of modifications [5]. The objectives of this paper are to provide the sufficient amount of information to the reader about Networking Architecture Implementation using Digital VLSI.

This paper gives the brief idea about basics of router, its internal structure and simulation results.

II. ROUTER IMPLEMENTATION

Fig.1 shows functional blocks of router. We are trying to make router of 3 inputs and 3 outputs. So at the source end we have provided 3 sources where they have given to the synchronizer which will synchronize it. Next FIFO arranges input packets in the First In First Out manner where they are forwarded to a core controller which has a main routing logic. According to the routing logic, packets will be sent to allotted destination where output from destinations will give to multiplexer. Output of a multiplexer will be decided by the core controller using select lines and finally output will be display on the LCD.

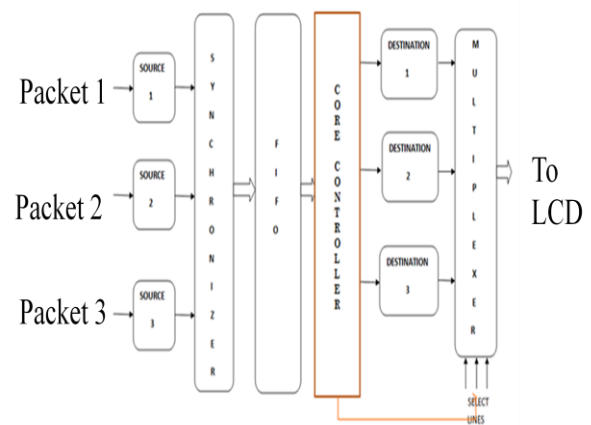


Fig.1 Functional blocks of router

III. PACKET GENERATION

Fig.2 shows the packet structure. We are transmitting a packet which consists of 12 words. Out of which first word is Preamble and the second word is CRC bits. The use of CRC bits is that to determine the transmitted packet is received correctly at respected destination. At the input side we are using CRC generation block. This block adds the 16 bits CRC code in the packet during formation of packet. This completes the second word of a packet. After receiving the remaining words the packet is send to the output side. At the output side CRC check bit unit is used.

This block determines CRC bits which are generated at input side. If these bits get matched then the packet received correctly. If there is any difference in these bits then the error signal is send.

Preamble (16 bit)	CRC (16 bit)	DATA (10 x 16 bit)
[1 st word]	[2 nd word]	[10 words]

Fig.2 Packet Format

IV. INTERNAL STRUCTURE

1.INPUT component

The internal structure for input port component is

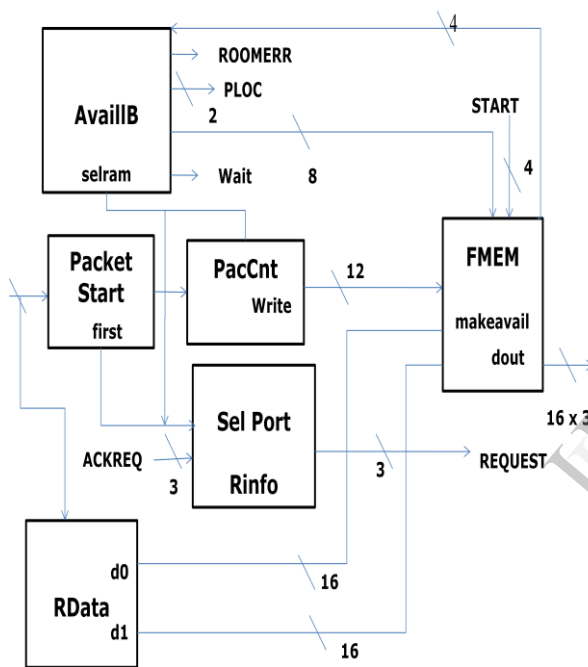
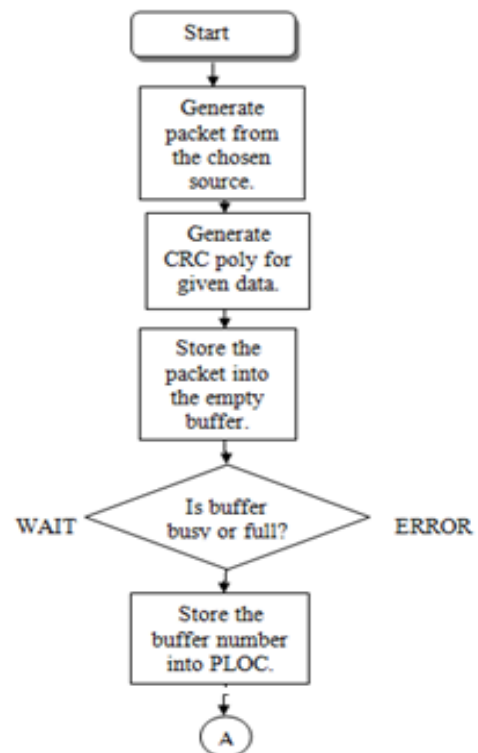


Fig.3 Structure of input port component

- Packet start component is responsible to indicate start of new packet.
- In RData component the incoming packet is stored in even and odd numbered word fashion.
- Selport component is used to determine where to send an incoming packet.
- Pac count component is used to collect all 12 words together.
- AvailB component is used to determine status of the buffer to store a packet.
- FMEM consists of 4 buffers and 3 multiplexers. These are used to at the output side to retrieve the selected packet data properly.

2. Routing Flow of Packet at Input side

1. START
2. Generate a packet from the chosen source.
3. The next step is to generate CRC poly for given data. The use of CRC poly is to determine whether the received packet is error free or not.
4. Now, the packet is ready to transmit at output port. But for this the output port number should be determine. So, during this process the packet is stored in buffer.
5. The next task is to determine the status of buffer.
 - a. If buffer is busy then it gives wait signal.
 - b. If buffer is full then it gives error signal.
 - c. If it is empty then it is stored in respected buffer.
6. Now, store the respected buffer number into the PLOC.
7. Now this information is used at output side to retrieve the respected packet.
8. The next step is to combine the PLOC data and chosen input port number to form meaningful request record.
9. Is produced request record is not meaningful then jump to 6.
 - a. If it is meaningful then go to the next step.
10. This request record is stored in SFIFO.
11. The output of SFIFO is send to T-controller. T-controller is responsible for to transmit the packet to outside network.
12. END.



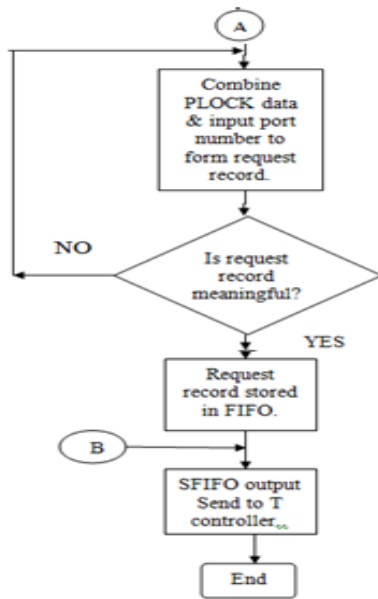


Fig.4 Flow Chart of input side

3. OUTPUT component

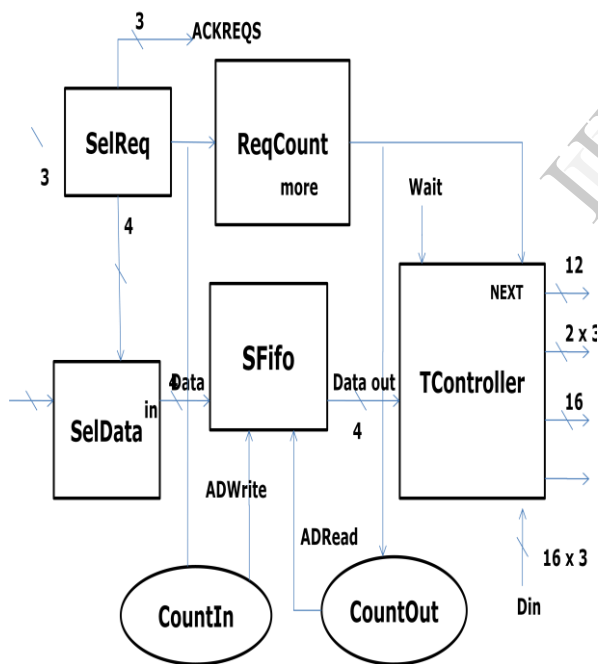


Fig.5 Internal structure of output port component

- SelReq accepts the request from the input side.
- ReqCount component is used to store the meaningful request record.
- The main work of SelData is to combine PLOC data and the input port number to form a meaningful request records.

- The output of SelData is written into the SFifo. This component used to avoid the overlapping of request record and provide priority mechanism.
- Tcontroller is the component which is actually responsible for to carry the packet from the output side to the external network where another router is situated.

4. Routing flow at output side

1. START.
2. The very first step is to check whether the output from input port is correctly received or not.
3. Then go on checking the meaningful request record till we get the full, correct and error free output.
4. Now perform the CRC poly checking.
5. The received CRC poly and the generated CRC poly should get matched. This tells that the received packet is error free and there is no loss of frames.
6. If this CRC checking fails then jump to 3.
7. Now remove the header from the received packet. That means remove the first word from the packet which indicates header of the packet.
8. Now the last step is to send the packet to respected output channel.
9. END.

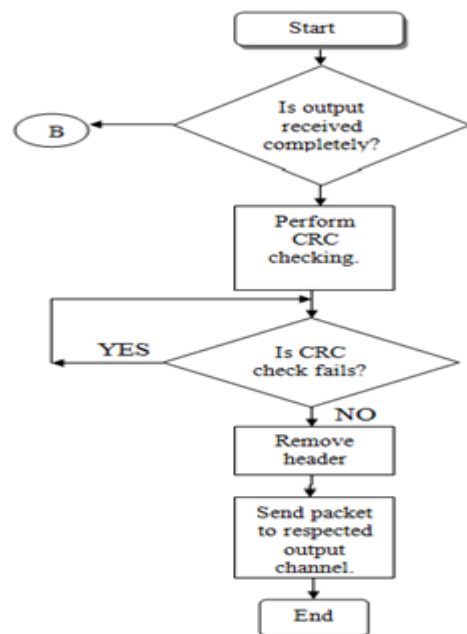


Fig.6 Flow chart of output side

V. SIMULATION RESULTS

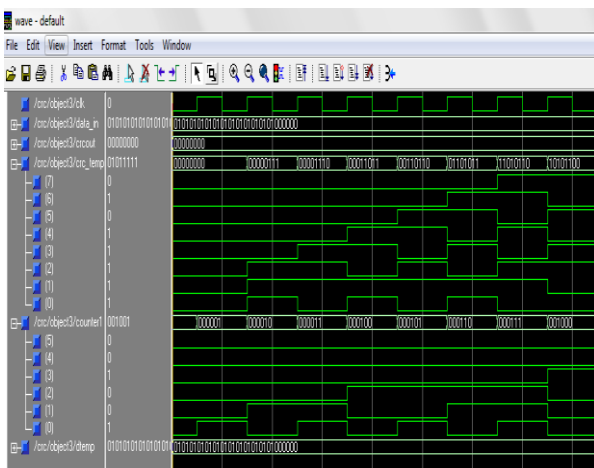


Fig.7 Simulation result for the CRC generation.

As per the simulation result (fig.7) when the clock and clock' event becomes 1 then FPGA will perform the CRC operations, at the same time counter will incremented by 1. When counter reaches to 32, temporary stored result will stored at crcout variable.

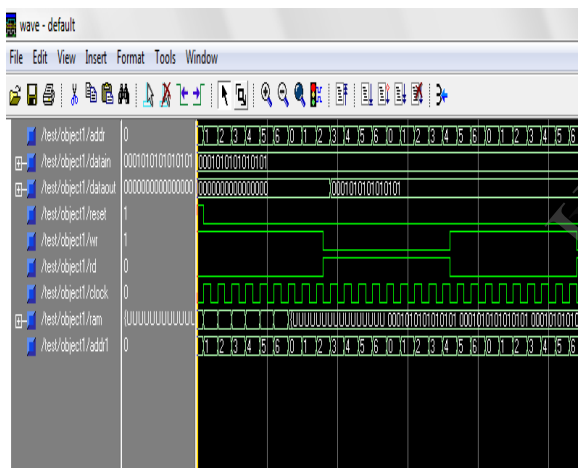


Fig.8 Simulation results for Frame Generation for RAM section.

In RAM as per the simulation result (fig.8) when the reset signal is high then there will not be any data transfer. If reset signal is low and write signal is high then data will write into the address, when there is read signal is high then data stored at addr1 will read from dataout signal.

VI. CONCLUSION

According to technology changes, in future we can modify the architecture for further improvements in a router. With the help of reprogramming ability implementation of the router in FPGA is possible. This thesis examines the possibilities of implementing the router chip in a programmable logic to allow quick and easy modification of hardware design for small research

computer, computers that are likely to undergo large amount of modification. The prototype of programming router can be used for educational purpose also.

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