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Design and Implementation of Fifteen Level Inverter for Solar PV Application

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Abstract: **- It is suggested to use a modern multilevel inverter with fewer power switches. This novel cascaded H-bridge multilevel inverter. Power generation from solar power plants is increasing daily to lessen its negative environmental effects. For the AC loads or to connect to the grid without impairing grid performance, the generated DC must be converted to AC. A multilevel inverter is an excellent choice because it produces an output voltage with a stepped waveform that is close to a sinusoidal and has less harmonic distortion. The harmonic distortion decreases as the number of levels rises, but at the same time, more switching devices and DC voltage sources are needed, which makes the system design and control more difficult.**

Key Words: Multilevel inverter, H-bridge, AC Load, DC Load, Harmonics, Switch, Waveform.

1. INTRODUCTION

The use of renewable energy sources for power generation is increasing quickly because of the rapidly shrinking fossil fuels and their adverse environmental impacts. Proper synchronization is a crucial need when several renewable energy units are coupled and integrated with the grid. As solar PV systems generate DC power, an inverter must be connected to produce the AC needed to connect to the grid [2]. The power fed into the grid contaminates the electrical system if the inverter's output contains harmonics. Thus, a good inverter design with minimal harmonic distortion is required [5]. Multilevel inverters are widely used these days compared to their range in voltage operation and function. By utilizing numerous diverse independent sources of dc voltage, the multilevel inverter generates the necessary output. By using a switching frequency and a rising number of DC sources, the inverter voltage output waveform is almost sinusoidal. Many dc sources result in minimal switching losses and low voltage stress [1]. Minimal Electro Magnetic Interference (EMI) output, high efficiency, minimal switching losses, high voltage operation capabilities, and ongoing multilevel inverter operation are all signs of this inverter's benefits. A three-level inverter serves as the root of the word "multilevel"[3]. Multilevel inverters are becoming more common in power electronic applications because they have a good ability to fulfil the increased demand for power. A consensus has been reached that the power electronics will take a main role in the future energy area. But which favorite type of grid-tied inverters for the future is still discussed. Dependent on the efficiency evaluation, the smaller inductance in the power loop will cause a higher efficiency, since the power loss caused by power device has become smaller and smaller [12]. Thus, it may be a good way to achieve high efficiency through decreasing the total inductance in the power loop.

Aiming to minimize the inductance of output filter of VSI, a recently new type of power filter named as the LLCL-filter was proposed and analyzed for the grid-tied VSI. Theoretically, compared with an LCL filter, an LLCL filter can save the total inductance. Due to the reason of familiarity, the conventional LCL filter is still used as the output filter benchmark for the comparison between several classical inverters. Typical full-bridge single-phase grid-tied inverters with the different power sources are introduced. Next, a new type of "buck in buck, boost in boost" grid-tied inverter is proposed, and the operating principle is illustrated through a half-bridge inverter with the equivalent circuits in the different working stages [10]. Then, the modeling is carried out with a small signal model method. Based on this, an indirect current control method is introduced, when the inverter is working in the "boost" stage.

2. SYSTEM ANALYSIS

2.1 Multilevel Inverter

Typical full bridge single phase inverter with different power sources is introduced due to some drawbacks then the typical three stage inverters was proposed. It is another kind of dual mode time sharing high efficiency inverter with full MOSFET switches and it has three power stages. Although three stages are adopted, the average efficiency can be over 98% under 1kW power operation. In boost stage over filtering takes place due to CL-CL filter and in buck stage the input LC filter may be a troublemaker in the control. For a conventional grid-connected PV generation system without transformers, there are usually two schemes for the power converters structure as follow. One is single-stage typical full bridge inverter in which multi-string PV panels are connected in series to meet DC voltage. The other is a two-stage PV generation system consisting of a front-end boost dc-dc converter and a backstage inverter. But the association of two-stage power inverter will result in high cost, low global efficiency, and complex control.

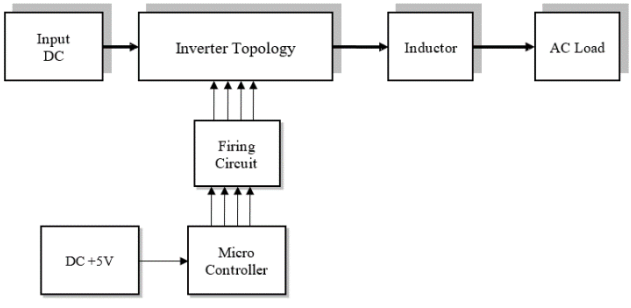

Fig 1: Existing Block Diagram

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2.2 Proposed System

Multilevel cascade inverters are used to eliminate the harmonics of THD, and the transformer required in case of conventional multiphase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. If the supply of each cell requires large number of isolated voltage and compare to the two types. The proposed Multilevel Inverter Topology has more advantages than the existing topologies as the number of switching devices and Total Harmonic Distortion are reduced. Therefore, the switching losses are also reduced, increasing an efficiency of the output. The proposed multilevel inverter requires a smaller number of switches and high efficiency and a smaller number of losses. Pulse Width Modulation (PWM) techniques are currently widely used due to their reduced computational requirement, simplicity, and robustness [9]. This multilevel inverter consists of three dc sources. Each source gives required voltage for each switch. The driver circuit requires 12 volts, pic micro-controller requires 5 volts and inverter circuit requires 24 volts of supply. The inverter circuit converts the current from DC to AC using rectifier [2]. The remaining driver circuit and microcontroller directly use dc voltages.

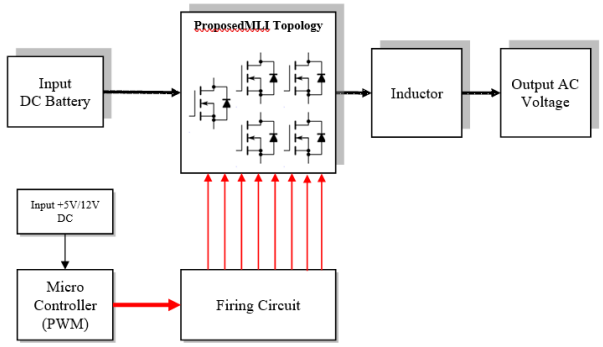

Fig 2: Proposed Block Diagram

The PWM switching frequency has to be much higher than what would affect the load (the device that uses the power), which is to say that the resulting waveform professed by the load must be as even as possible [18]. The rate (or frequency) at which the power supply must switch can differ greatly depending on load and application. In cascaded MLI using 8 switches we can obtain 7 levels 12 switches are required for 11 levels and so on. The proposed topology uses only 8MOSFET switches and three DC voltage Sources to obtain 15 levels [13]. In comparison with the conventional 15-level Inverter reduced number of switches used in this topology effectively reduces the switching losses and most importantly the circuit complexity. The DC voltage source magnitude is designed with binary forms of voltage such as V, 2V, and 4V respectively. The designed topology gives out 15-level output voltages; they are V_{dc}, $6V_{dc}/7$, $5V_{dc}/7$, $4V_{dc}/7$, $3V_{dc}/7$, $2V_{dc}/7$, $V_{dc}/7$, 0, $-V_{dc}/7$, $-2V_{dc}/7$,$-3V_{dc}/7$,$-4V_{dc}/7$,$-5V_{dc}/7$,-$6V_{dc}/7$ respectively(Output). Depending on the output voltage requirement, V can be chosen appropriately. For example, to obtain peak amplitude of 21 volt, the voltage sources required are 3-volt, 6 volt and 12 volt.

2.3 Proposed Inverter Topology

A newly developed 15-level inverter is shown. The DC-link voltage of the solar PV based boost converter is fed as a source to the proposed inverter. The proposed inverter comprises eight uni-directional switches and three sources of DC. In the proposed 15-level asymmetrical MLI, the switches are selected based on the strategy of avoiding short circuits in the specified path of current traversal. The initial level is obtained by conducting the switches S2, S3, S5, and S7, forming a closed path precisely without a short circuit. In this level of operation, the blocking voltage of switches is considered in calculating the total standing voltage. In the second level of operation, the switches S2, S3, S5, and S7 are in conduction.;

3. SWITCHING SEQUENCE

C	SW 1	SW2	SW 3	CH4	CH 5	CH 6	CH 7
1	0	1	1	0	1	0	1
2	0	1	1	0	1	1	0
3	1	0	1	0	1	0	1
4	1	0	1	0	1	1	0
5	0	1	1	0	0	1	1
6	0	1	1	0	0	1	1
7	1	0	1	0	0	1	1
8	0	1	0	1	1	0	1
9	0	1	0	1	1	1	0
10	1	0	0	1	1	0	1
11	1	0	0	1	1	0	1
12	0	1	0	1	0	1	1
13	0	1	0	1	0	1	1
14	1	0	0	1	0	1	1
15	1	0	0	1	0	1	0

Table 1: Switching Sequence Table

3.1 Switching Sequence Working

The inverter is proposed with asymmetrical DC input sources with a 1:2:5 ratio for generating 15-level output voltage levels, and source voltages are taken Vdc = V1 = 48V, V2 = 96V, and V3 = 142V respectively, shown the inverter switching states in Table., and by using the staircase PWM technique, produce gate pulses.

LEVEL 1:

The output voltage is the number of V2 + V3 in level 1; SW2, SW3, CH5, and CH7 switches are ON, and the remaining switches are OFF.

LEVEL 2:

The output voltage is −V1 + V2 + V3, the SW2, SW3, CH5, and CH6 switches are ON, and the remaining switches are OFF.

LEVEL 3:

The SW1, SW3, CH7, and CH5 switches are ON in level-3 and the remaining switches are OFF, and the output voltage is the amount of V3.

LEVEL 4:

The output voltage is the number of −V1 +V3 in level-4, the SW1, SW3, CH5, and CH6 switches are ON, and the remaining switches are OFF.

LEVEL 5:

The output voltage is the amount of V1 + V2 in level-5, the SW2, SW3, CH6, and CH7 switches are ON, and the remaining switches are OFF.

LEVEL 6:

The output voltage is the amount of V2 in level-6, the SW2, SW3, CH6, and CH7 switches are ON, and the remaining switches are OFF.

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LEVEL 7:

The output voltage is the amount of V1 in level 7, the SW1, SW3, CH6, CH7 switches are ON, and the remaining switches are OFF.

LEVEL 8:

The SW2, CH4, CH5, CH7 switches will ON in level-8 and the remaining switches are OFF the 0V output voltage.

LEVEL 9:

The SW2, CH4, CH5, CH6 switches are ON in level-9, and the remaining switches are OFF, the output voltage is −V1.

LEVEL 10:

The SW1, CH4, CH5, CH7 switches are ON in level-10, and the other switches are OFF, the output voltage is −V2.

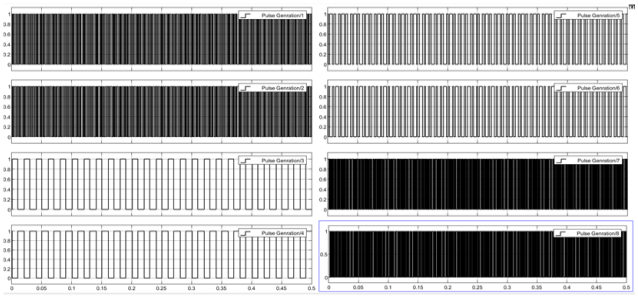

Fig 3: Pulse Generator

4. SIMULATION

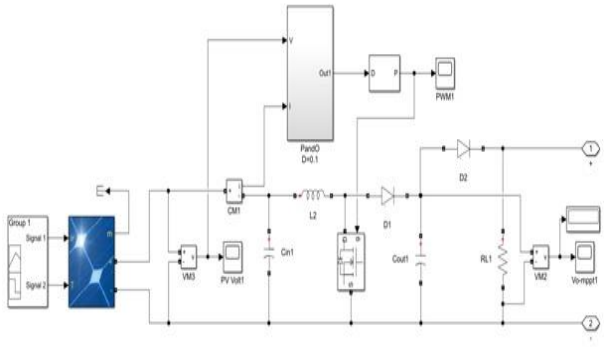

Fig 4: Simulation Diagram with Solar Panel

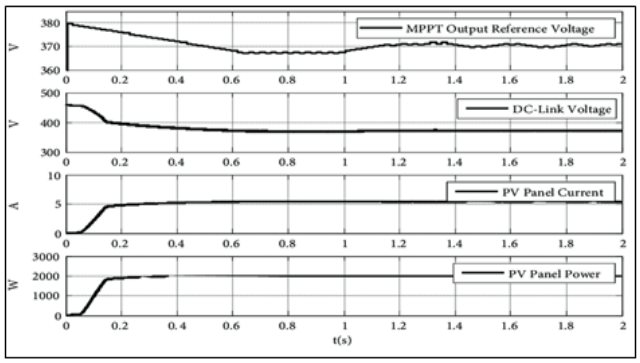

Fig 5: MPPT Output Waveform

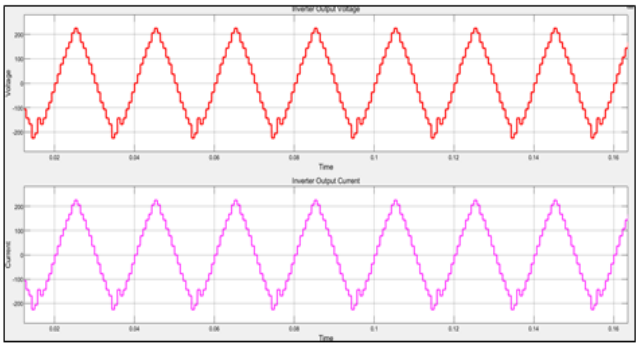

Fig 6: Simulation Waveform

5. HARDWARE DESIGN

Using the following generalized questions, the suggested inverter circuit parameters, such as the number of levels (NL), number of switches (NSW), number of DC sources (NSDC), and peak output voltage (VOP), can be calculated.

$$N_{SDC} = n$$

$$N_{SW} = (2^{n_{k1}+1}) + (2^{n_{k2}+1}) + \ldots\ldots\ldots + (2^{n_{kj}+1})$$

$$N_L = (2^{n_{k1}+1}-1) + (2^{n_{k2}+1}-1) \ldots + (2^{n_{kj}+1}-1)$$

$$V_{OP} = \left(\frac{2^{n_{k1}+1}-2}{2} + \frac{2^{n_{k2}+1}-2}{2} + \ldots\ldots + \frac{2^{n_{kj}+1}-2}{2} \right) \times Vdc$$

Where n and k for the proposed inverter are the numbers of sources and modules, respectively. The proposed inverter was simulated with MATLAB/Simulink and experimentally verified with the micro-Controller, as shown in circuit diagram. It shows the simulation output waveforms and THD is discussed in phase I. The controller is used to produce gate pulses with the driver technique of the staircase PWM. For the simulation and experimental, the 100ohm, 175mh, single-phase with 60V, 50W, and power factor 0.85 respectively were used as loads for the proposed inverter. Source voltages are taken Vdc = V1 = 12V, V2 = 24V, and V3 = 48V to attain maximum peak output voltage Vo= 60.05V. The proposed 15-level inverter is tested with linear loads for the robustness of the inverter.

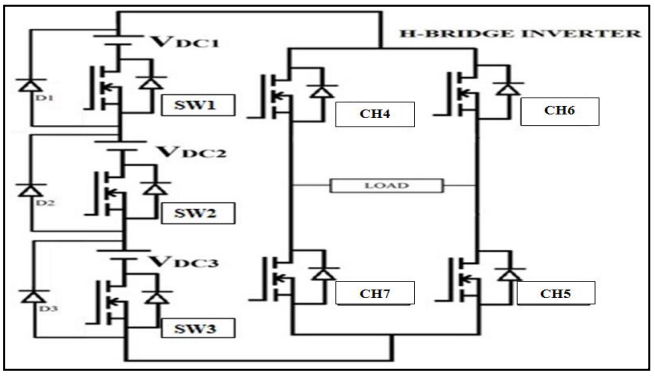

Fig 7: Circuit Diagram

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Fig 8: Hardware Image

7. CONCLUSION

A single phase 15 level reduced switch MLI topology is introduced by various types of operation are studied. A novel SPWM modulation approach is proposed and utilized a proposed topology; the simulation results are verified. The results for the proposed system are explained proposed MLI uses only 8 switches to give 15 levels output. It showed the simulation results that the THD for the Output voltages and current of the proposed system is low and compared to the existing. For low and medium power applications typical MLI cannot compete with standard UPS at lower-level configurations and to the circuit complexity.

A new 15-level inverter has been designed with a reduced number of components for DC applications were proposed in this work. The conventional boost converter produces a higher DC-link voltage and is fed to the inverter for AC stepped output waveform. The proposed inverter generates higher output voltage levels with a lesser number of circuit components with low THD-Experimentally tested the inverter with linear loads and well stable during dynamic circumstances and suits for grid-connected.

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