

Design and Implementation of Dual Output Forward Converter for Space Applications

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Abstract - DC-DC converters are extensively employed in spacecraft power supply applications. In this paper, a 60 W dual-output isolated forward DC-DC converter operating at a high switching frequency of 180 kHz has been designed as per the Specifications. Isolated configurations are preferred for space and defence systems due to galvanic isolation, reduced electromagnetic interference (EMI), and enhanced design flexibility. Simulation and hardware of the Converter has been implemented. The converter is designed to deliver regulated output voltages of 5V/10.5A and 3.3V/2A from an input bus of 65–70 V DC with an efficiency greater than 70%. A voltage feed-forward control technique is employed to achieve the required line regulation. A Low Dropout (LDO) regulator (LT1085) is used as a post-regulator for the 3.3V output. Protection circuits Such as inrush current limiting, under-voltage lockout, and over-current protection have also been incorporated. A hardware prototype was developed, tested, and validated under different input voltages and load conditions. The Simulation and Hardware results were found to be within the Specifications.

Keywords - Dual Output, Forward Converter, LDO Regulator, Line Regulation, Load Regulation, Protection Circuit, Switching Frequency, Voltage Feed-Forward.

I. INTRODUCTION

Reliable and efficient power conversion technologies are indispensable in the aerospace industry to maintain the uninterrupted operation of various spacecraft subsystems. DC-DC converters occupy a central role in supplying regulated power to on-board systems such as computers, communication units, and sensors, each of which operates at distinct voltage levels. The power converter topologies are Buck, Boost, Buck-Boost, Cuck, SEPIC, Flyback, and Forward converters [1]. Among these Converters, Forward converter has emerged as a preferred choice for low-to-medium power space applications owing to its superior reliability, galvanic isolation, high efficiency, compact structure, and inherent ability to step down voltage [1].

Switched Mode Power Supplies (SMPS) overcome the limitations of linear supplies, namely poor efficiency and limited voltage step-up capability [2]. The relentless drive by space research organisations towards lighter, smaller, more efficient, and highly reliable power supply units has intensified research in advanced DC-DC converter designs [2].

The present work focuses on a single-switch, dual-output forward converter rated at 60W for space applications, operating at a high switching frequency of 180 kHz and delivering two regulated DC outputs: 5 V at 10.5 A and 3.3 V at 2A from an input bus of 65–70 V DC. To achieve the required line regulation over the wide input voltage range and rapid response to input transients, a voltage feed-forward control technique is implemented in the primary side of the converter [3][4]. The UC2825 PWM controller implements this feed-forward mechanism by automatically adjusting the duty cycle in proportion to the input voltage. Linked inductor topology is implemented to avoid cross regulations between the two outputs. An LT1085 Low Dropout (LDO) regulator is employed as a post-regulator to get the 3.3 V output for very accurate regulation of the output. The Converter is designed to achieve an efficiency greater than 70%. A protection circuitry, encompassing inrush current limiting, under-voltage lockout (UVP), and over-current protection (OCP), has been designed and implemented to ensure robust operation in the harsh space environment.

II. BLOCK DIAGRAM

The block diagram of the proposed 60 W dual-output forward converter is shown in Fig. 1. The converter accepts a 65–70 V DC input bus, which is first passed through a differential and common-mode EMI filter to suppress conducted noise. An inrush current limiter protects the input source and power components from the high surge current that arises during start-up due to the discharge of input filter capacitors.

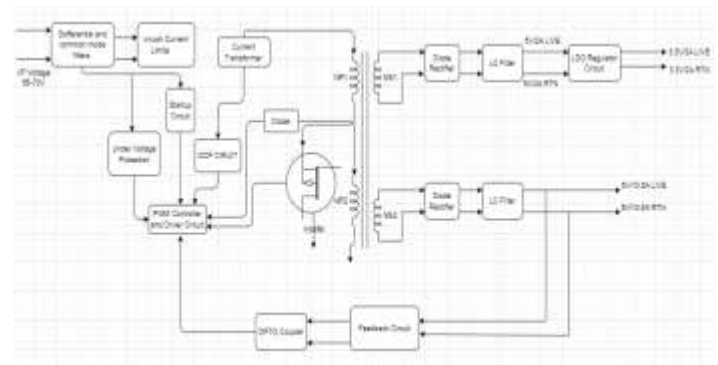


Fig. 1: Block Diagram of the Dual Output Forward Converter

A start-up circuit supplies the initial voltage required by the PWM controller (UC2825 PWM) until the auxiliary bias winding develops sufficient voltage. An under-voltage protection (UVP) circuit constantly checks the input supply and inhibits the switching activity if input voltage drops below the safe level. The MOSFET switch is powered by the UC2825 PWM controller with voltage feed-forward control, which dynamically adjusts the duty cycle in accordance to the instantaneous input voltage to achieve good line regulation. The high-frequency isolation transformer provides galvanic isolation and supplies energy to both secondary windings at the same time.

On the secondary side fast-recovery Schottky diode rectifier are used. Inductor and capacitor output filter (LC filters) suppress switching ripple to deliver smooth DC outputs. A coupled inductor topology on the output stage minimises cross-regulation between the two outputs, wherein a change in the load current of one output may unintentionally cause the voltage of another output to change. The 5V output is used as the primary feedback signal for the closed-loop regulation loop via an opto-coupler (PS2802) and the UC2825. The 3.3V output is post-regulated using an LT1085 LDO regulator for precise output voltage control. An over-current protection (OCP) circuit using current-sense transformers and comparators (LM158) continuously monitors the load current and disables the converter in the case of overcurrent or short circuit.

III. WORKING OF THE PROPOSED FORWARD CONVERTER

The Proposed Converter is shown in Fig. 2. The forward converter is an isolated DC–DC converter that transfers energy from the primary to the secondary during the ON period of the switching MOSFET (M1). When Mosfet is turned ON, the input voltage V_{in} is applied across the primary winding of the transformer. A scaled down version of this voltage appears across the secondary windings in accordance with the transformer turns ratio. Each secondary is carried out by Schottky rectifier diodes and transferred energy through the output LC filters to the loads. The UC2825 PWM controller automatically increases the duty cycle when V_{in} decreases and decreases the duty cycle when V_{in} increases, thereby compensating for input voltage variations in real time (feed-forward control).

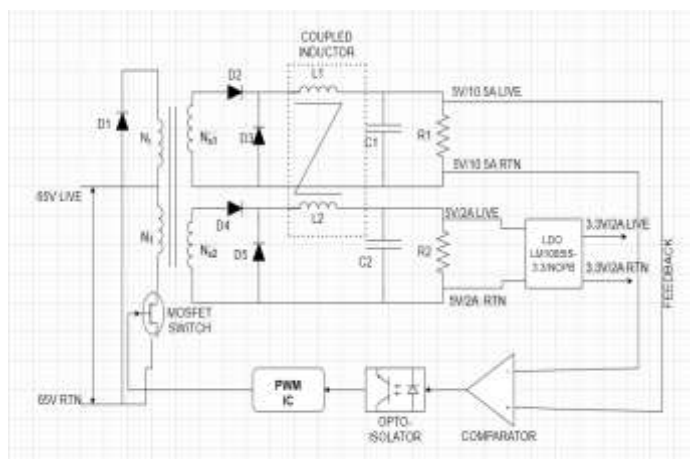


Fig. 2: Circuit Diagram of the of the Proposed Converter

When Mosfet is turned OFF, the energy stored in the transformer magnetising inductance is returned to the input source through the demagnetising (reset) winding and the associated reset diode. On the secondary side, the freewheeling diodes conduct to maintain continuous current through the output inductors. The stored energy in the output LC filters dissipates into the loads during the OFF period. Before the inductors de-energies completely, Mosfet turns ON again and the cycle repeats. The secondary 5V output is post regulated with the LT1085 LDO regulator for Output 2 (3.3V).

IV. SPECIFICATIONS AND DESIGN OF THE PROPOSED CONVERTER

The Specifications of the forward converter is shown in Table 1.

Table 1: Specifications of the Proposed Forward Converter

Parameter	Specification
Input Voltage	65–70 VDC
Output 1	5 V / 10.5 A
Output 2	3.3 V / 2 A
Total Output Power	60 W
Switching Frequency	180 kHz
Output Ripple Voltage	≤ 100 mV
Line Regulation	$\leq 1\%$
Load Regulation	$\leq 1\%$
Efficiency (Full Load)	$> 70\%$

A. Transformer Design

The most important part of the forward converter is the transformer. It provides galvanic isolation between the primary and secondary side. A high switching frequency of 180 kHz is selected to reduce the transformer core and winding dimensions. The Area Product (A_p) method is used to select the optimal core size, number of turns, and wire gauge [9].

The Area Product of the transformer core is calculated using:

Core Selection:

The optimum design is decided by the small size and lower dissipation of transformer, so Window Factor (K_w), Flux Density (B_m) & Current Density (J) values are assumed, for optimal design.

$$K_w = 0.4$$

$$B_m = 0.06 \text{ Tesla}$$

$$J = 4 \text{ Amp/mm}^2$$

$$\text{Efficiency} = 75\%$$

$$\text{Maximum duty cycle (D}_{\max}) = 0.45$$

$$\text{Switching Frequency (F}_{\text{sw}}) = 180 \text{ kHz}$$

$$\text{Output Power (P}_{\text{out}}) = 60 \text{ W}$$

$$A_p = \frac{\sqrt{D_{\max}} * P_{\text{out}} \left(1 + \frac{1}{\text{Efficiency}} \right)}{K_w * J * 10^{-6} * B_m * F_{\text{sw}}} \quad (1)$$

$$A_p = 5670.3992 \text{ mm}^4$$

An appropriate core will be selected which have Area product (A_p) greater than the calculated A_p . Hence, selected toroid Core: W374F TC, Material: F which will have Cross sectional Area, $A_c = 24 \text{ mm}^2$, Window Area, $A_w = 127 \text{ mm}^2$, $AL = 9.1 \text{ UH/1}$.

$$A_p = A_c * A_w \quad (2)$$

$$A_p = 3048 \text{ mm}^4$$

Turns ratio Calculation:

Number of Primary Turns (N_p) is calculated using the formula

$$N_p = \frac{(V_{in_{min}} * D_{max})}{B_m * A_c * 10^{-6} * F_{sw}} = 62.86 \text{ Turns} \quad (3)$$

Transformer ratio (T_{ratio}) of primary and secondary is given from the equation:

$$T_{ratio} = \frac{N_s}{N_p} = \frac{V_{out} + (V_D * D_{max})}{D_{max} * V_{in_{min}}} \quad (4)$$

Therefore, $T_{ratio} = 0.184$.

Number of Secondary Turns (N_s) is:

$$N_{s1} = T_{ratio} * N_p = 11.7771 \text{ Turns}$$

$$N_{s2} = T_{ratio} * N_p = 11.7771 \text{ Turns}$$

$$L_s = N_s^2 * A_L$$

$$L_{s1} = 0.018 \text{ H}$$

$$L_{s2} = 0.0018 \text{ H}$$

$$L_{nbias} = 0.0071 \text{ H}$$

Transformer ratio of bias winding ($T_{ratio_{bias}}$) is:

$$T_{ratio_{bias}} = \frac{V_{bias} + (V_{D_{bias}} * D_{max})}{D_{max} * V_{in_{min}}} \quad (5)$$

Therefore, $T_{ratio_{bias}} = 1.013$.

$$\frac{N_{bias}}{N_p} = T_{ratio_{bias}}$$

Number of Bias winding Turns $N_{bias} = 26.8964 \text{ Turns}$

Bias Winding Inductance, $L_{bias} = L_p = 0.0071 \mu\text{H}$

B. Output 1 Filter Design

Let, Output Voltage, $V_{out} = 5 \text{ V}$

Output Current, $I_{out} = 10.2 \text{ A}$

Minimum Duty cycle on secondary, $D_{min_s} = 0.45 * D_{min} = 0.3343$

Therefore, Output Filter Inductor (L) is calculated by using the equation:

$$L1 = \frac{V_{out_s} * (1 - D_{min_s}) * T_s}{2 * \Delta I_L * I_{out_s}} \quad (6)$$

$$L1 = 4.5324 \mu\text{H}$$

Therefore, Output Filter Capacitor (C) is calculated by using the equation:

$$C1 = \frac{(1 - D_{min_s}) * I_{out_s}}{8 * L * F_{sw}^2 * V_{D_{delta}}} \quad (7)$$

$$C1 = 56.66 \mu\text{F}$$

C. Output 2 Filter Design

Let, Output Voltage, $V_{out} = 3.3 \text{ V}$

Output Current, $I_{out} = 2 \text{ A}$

Minimum Duty cycle on secondary, $D_{min_s} = 0.45 * D_{min} = 0.3343$

Therefore, Output Filter Inductor (L) is calculated by using the equation:

$$L2 = \frac{V_{out_s} * (1 - D_{min_s}) * T_s}{2 * \Delta I_L * I_{out_s}} \quad (8)$$

$$L2 = 7.004 \mu\text{H}$$

Therefore, Output Filter Capacitor (C) is calculated by using the equation:

$$C2 = \frac{(1 - D_{min_s}) * I_{out_s}}{8 * L * F_{sw}^2 * V_{D_{delta}}} \quad (9)$$

$$C2 = 61.11 \mu\text{F}$$

D. MOSFET Selection

The MOSFET selection is governed by the maximum drain-to-source voltage stress, which includes the input voltage reflected across the transformer reset winding. With a 1:1 reset winding ratio, the peak MOSFET voltage is approximately $2 * V_{in_{max}} = 2 * 70 = 140 \text{ V}$. Including a safety margin of 1.5x, a MOSFET with VDS rating $\geq 200 \text{ V}$ is required. The BUY25CS12J-01 MOSFET, rated at 250 V and 12.4 A, was selected. This device offers low conduction losses, greater robustness under heat and radiation stress and is appropriate for space grade applications.

E. Secondary Diode Selection

Schottky diodes are chosen as the output rectifiers due to their virtually nil reverse recovery time, low forward voltage drop of about 0.45 V and strong current handling capacity. Output 1: 16CYQ100 (100 V, 16 A, space-grade Schottky) Output 2: PDS3200-13 rapid recovery Schottky rectifiers. All diode values were derated to 70% for dependable operation under transient and overstress circumstances [7].

F. LDO Regulator for Output 2

The LT1085 adjustable LDO regulator post-regulates the 3.3 V/2 A output. The LT1085 receives approximately 5 V from the secondary rectifier and regulates it down to 3.3 V. The output voltage is set by the external resistor divider ($R1 = 1.6 \text{ k}\Omega$, $R2 = 1 \text{ k}\Omega$) connected to the ADJ pin, using the internal

reference voltage of 1.25 V. This approach eliminates the need for a separate secondary winding for 3.3 V and significantly simplifies the transformer design while achieving very tight output regulation.

G. Protection Circuits

Three protection mechanisms are implemented. The inrush current limiter uses a MOSFET (IRFB600N25N3) and a soft-start RC network ($R_2 = 150\text{ k}\Omega$, $C = 1\text{ }\mu\text{F}$) to ramp up the gate voltage during the start-up gradually to limit the initial charge current of input capacitors. A 12 V Zener diode limits the gate voltage to safeguard the MOSFET.

The under-voltage lockout (UVP) circuit is built with an LM158 comparator, a resistor divider ($R_{105} = 91\text{ k}\Omega$, $R_{102} = 3.9\text{ k}\Omega$) for input voltage sensing and a hysteretic feedback resistor ($R_{101} = 510\text{ k}\Omega$) to eliminate chattering around the threshold. When the input goes below $\sim 28\text{ V}$ (reflected threshold), the comparator output drives the PWM controller shutdown pin, ending all switching activity.

The over-current protection (OCP) circuit uses two LT1001 comparators with an RC filter network (R_4 , R_5 , C_1 , C_2) to sense and filter the current transformer signal. A Schottky diode (1N5819) transmits the fault signal to the PWM controller's shutdown pin. Hysteresis is introduced via a positive feedback resistor to avoid nuisance trips from switching transients.

H. Summary of Design Outcomes

Table 2 summarizes the final design parameter values used in the hardware implementation.

Table 2: Design Outcomes of the Proposed Forward Converter

Parameter	Value
No. of Primary Turns (N_p)	64 Turns
No. of Secondary Turns (N_{s1} , N_{s2})	14 Turns each
No. of Bias Winding Turns (N_{bias})	27 Turns
Output Filter Inductor L1	5 μH
Output Filter Inductor L2	7 μH
Output Filter Capacitor C1	68 μF
Output Filter Capacitor C2	68 μF
MOSFET	(250V, 12.4A)
Secondary Diode	(100V, 16A Schottky)
Core Type	W374F TC Toroid, Material F

V. SIMULATION OF THE PROPOSED CONVERTER

The proposed dual output forward converter was simulated using industry standard tools, LTspice for design verification before the hardware manufacturing. Both simulators employ SPICE-based transient analysis engines, allowing accurate modelling of the switching transients, transformer coupling, and feedback control loop dynamics.

A. LTspice Simulation

The LTspice simulation model of the dual-output forward converter which is shown in Fig. 3, is constructed with the UC2825 PWM model, the switching MOSFET, transformer (modelled with coupling coefficient $K = 0.99$), Schottky rectifiers, LC filters, and the closed-loop feedback network. Simulations were run for input voltages of 65 V and 70 V DC. At $V_{in} = 65\text{ V}$, the converter delivers 5 V/10.5 A at Output 1 and 3.3 V/2 A (post-LDO) at Output 2. Similar regulated outputs are achieved at $V_{in} = 70\text{ V}$, demonstrating excellent

feed-forward line regulation. The output voltage starts from zero at $t = 0$ and rises gradually as the output capacitors charge through the transformer-rectifier-filter chain, reaching steady state within approximately 5–10 ms.

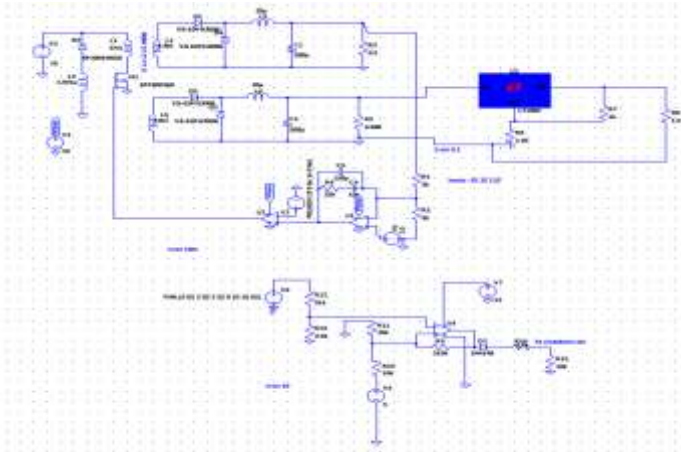


Fig. 3: Simulation Model of Dual Output Forward Converter Using LT Spice

VI. HARDWARE IMPLEMENTATION

A hardware prototype of the proposed 60 W dual-output forward converter was fabricated on a two-layer PCB. Surface-mount and through-hole components were combined to optimise PCB layout density for the intended space application form factor. The PCB incorporates six distinct functional sub-sections: input stage (EMI filter, ICL, UVP), power switching stage (MOSFET, driver), transformer stage, secondary rectification and filtering stage, PWM control and feedback stage, and the LDO post-regulator stage.

A. Circuit Description

Fig. 2, shows the functional circuit diagram of the proposed converter. The primary switch M1 (BUY25CS12J-01) is driven by the UC2825 PWM controller through a dedicated gate driver circuit that provides the required gate voltage and current slew rate. The transformer TR1 (W374F TC toroid, 180 kHz) provides galvanic isolation with a turns ratio ensuring the correct output voltages at maximum duty cycle ($D_{max} = 0.45$).

The secondary rectifier diodes (16CYQ100 and PDS3200-13) are arranged as a full-wave rectifier on each output secondary winding. The coupled output filter inductors (wound on a single core) reduce cross-regulation effects between the two outputs. Output capacitors (68 μF per output) filter residual switching ripple. Feedback from Output 1 (5 V) is sampled through a resistive divider, passed through an error amplifier (LM158), and transmitted to the primary controller via a PS2802 opto-coupler for galvanic isolation. The UC2825 adjusts the duty cycle accordingly.

B. PWM Controller (UC2825)

The UC2825 is a high speed PWM controller that is capable of running at up to 1 MHz and is ideal for this 180 kHz application. The device includes voltage-mode and current-mode control, under-voltage lockout (UVLO), soft-start, slope correction, and dead-time control. The oscillator frequency is set by external CT and RT components. The UC2825 starts switching when the VBIAS exceeds approximately 9 V, supplied initially by the start-up circuit and subsequently

maintained by the bias winding rectifier. The soft-start capacitor (SS pin) ensures a gradual duty cycle ramp during start-up to limit inrush effects.

C. Hardware Setup

The experimental hardware configuration comprises: K1 input connector (65–70 V DC input), external ON telemetry (5 V command signal), the PCB hardware board with all power and control circuits, a variable DC voltage source, a digital storage oscilloscope (DSO/CRO) for waveform capture, a precision multimeter for voltage and current measurement, and an electronic load for programmable load testing.

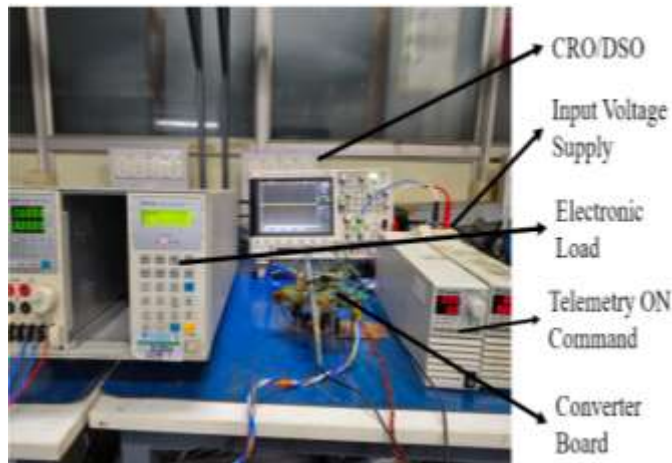


Fig. 4: Hardware Setup

The Hardware setup, Top view and Bottom view of PCB module is shown in Fig. 4, 5 and 6 respectively.

Thin-film surface-mount fuses (F1, F2) provide input protection. Colour-coded wiring and Kapton tape for cable management and insulation (selected for its superior thermal stability and suitability for aerospace applications) complete the assembly. Two D-sub connectors serve as standardised interfaces for power and telemetry signals.

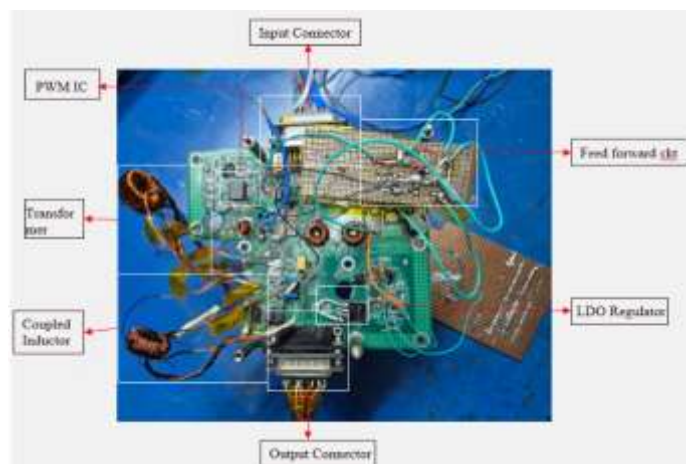


Fig. 5: PCB Top View of the Converter



Fig. 6: PCB Bottom View of the Converter

VII. RESULTS AND DISCUSSION

The Simulation and Hardware results are presented in this section.

A. Simulation Results

The Simulation results of the forward converter shown in fig. 7. When the input voltage is 65V, an output voltage of 5V and 3.3V and Output Current of 10.5A and 2A respectively is obtained across the output. The voltage attained complies with the design requirements.

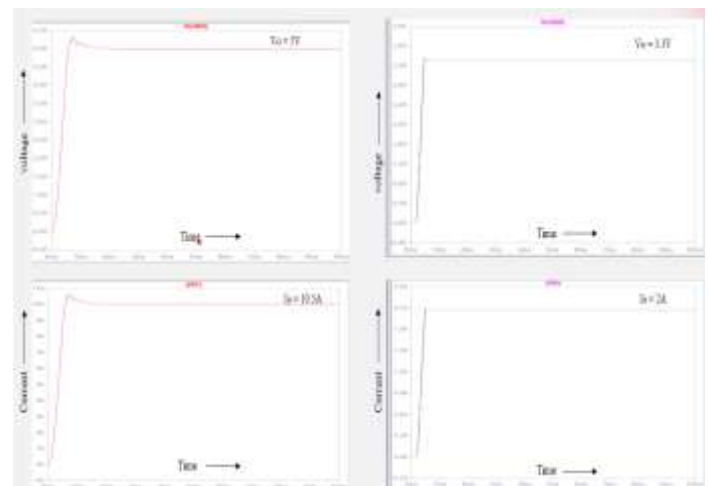


Fig. 7: Output voltage and current (Output I and Output II),
 input voltage 65V DC

The simulation result of Forward Converter is shown in below Fig. 8. Output voltage of 5V and 3.3V and Output Current of 10.5A and 2A respectively is obtained across the output when the Input Voltage is 70V. The voltage obtained is as per the design specifications.

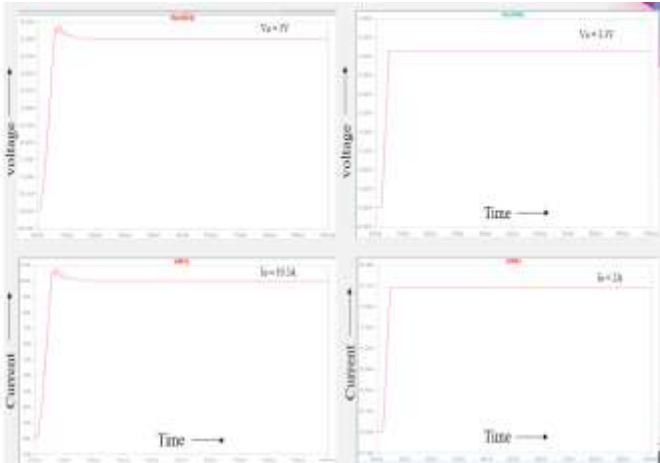


Fig. 8: Output voltage and current (Output I and Output II),- input voltage 70V DC

B. Hardware Results

The hardware prototype was tested over the complete input voltage range (65–70 V) and three representative load conditions: 10% (light load), 50% (half load), and 100% (full load). Results for output voltage regulation, voltage ripple, MOSFET drain voltage, efficiency, and line/load regulation are presented and analysed below:

i) Output Voltage Waveforms

The waveforms of Output1 and 2 at 10% Load are shown in Fig. 9 and 10 respectively. The following observations were made from the waveforms:

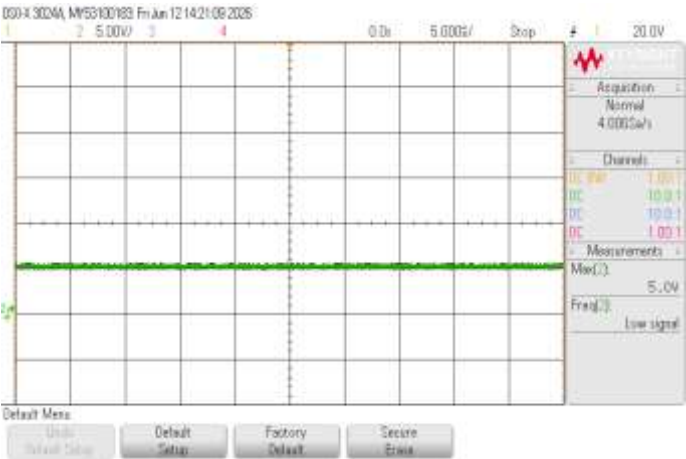


Fig. 9: Output 1(5V) for 10% load

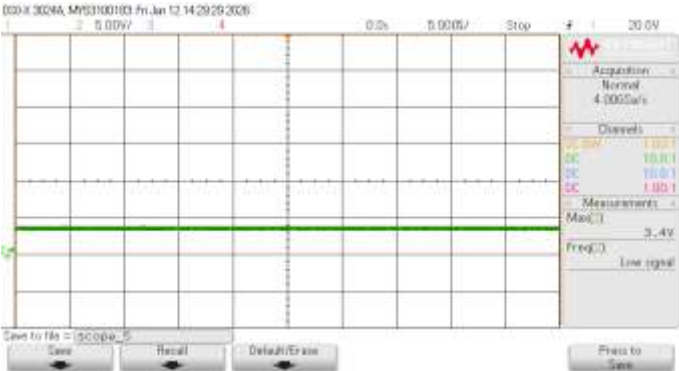


Fig. 10: Output 2(3.3V) for 10% load

A small steady-state offset of approximately 0.1–0.2 V above the target for Output 2 is attributed to component tolerances in the LDO resistor divider network and can be corrected by fine-tuning R1/R2 in the LT1085 feedback network.

ii) Output Voltage Results

Table 3 and Table 4 summarizes the measured output voltages for Output 1 (5 V) and Output 2 (3.3 V) at three input voltages and three load conditions.

Table 3. Output Voltage 1 (5 V Nominal) Measurement Results

Vin (V)	10% Load	50% Load	100% Load
65	5.008 V	5.011 V	5.010 V
68	5.008 V	5.012 V	5.011 V
70	5.007 V	5.011 V	5.011 V

Table 4. Output Voltage 2 (3.3 V Nominal) Measurement Results

Vin (V)	10% Load	50% Load	100% Load
65	3.31 V	3.31 V	3.30 V
68	3.31 V	3.31 V	3.31 V
70	3.31 V	3.31 V	3.304 V

The tables show that Output 1 is regulated from 5.007 V to 5.012 V for all input and load circumstances with only a 5 mV (0.1%) variance. Output 2 maintains a stable 3.30–3.31 V, confirming effective LDO post-regulation. The output voltage is within the specifications limits.

iii) MOSFET VDS Waveforms

The MOSFET drain-to-source voltage (V_{DS}) waveform characteristics at the three load conditions with V_{in} equal to 65 V is shown in Table 5.

Table 5. MOSFET V_{DS} Waveform Summary (V_{in} = 65 V)

Load Condition	Peak VDS (V)
10% Load	94 V
50% Load	148 V
100% Load	216 V

The peak VDS at 10% and 50% load (94 V and 148 V respectively) is well below the 250V Voltage rating (250V) of the chosen MOSFET (BUY25CS12J-01). The peak at 100% load is about 216V due to the larger energy stored in the leakage inductance and parasitic elements during switching. However this value is also below 250 volts rated V_{DS} , confirming safe operation. The V_{DS} waveforms are shown in Fig. 11,12 and 13.

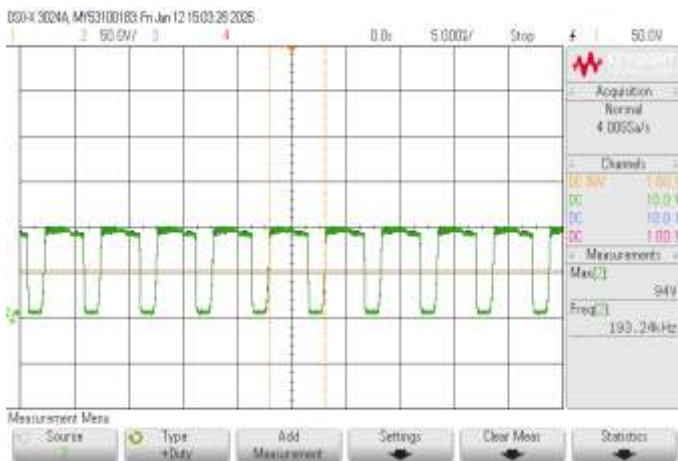


Fig. 11: V_{DS} at 10% Load

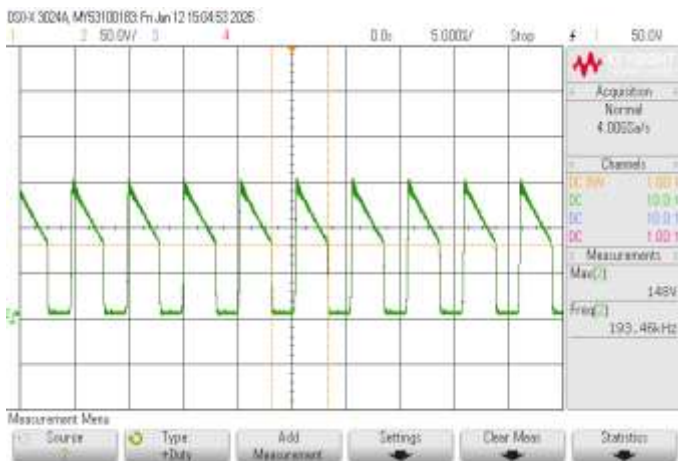


Fig. 12: V_{DS} at 50% Load

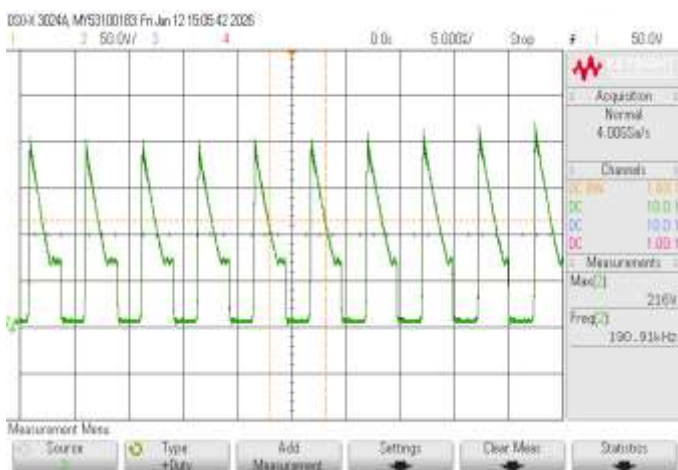


Fig. 13: V_{DS} at 100% Load

iv) MOSFET Gate-Source (V_{GS}) Waveforms

Fig. 14,15 and 16 shows the MOSFET gate voltage(V_{GS}) waveform of the proposed forward converter at 10%, 50% and 100% load respectively. It is observed that the waveforms are as per the required specifications.



Fig. 14: V_{GS} at 10% Load

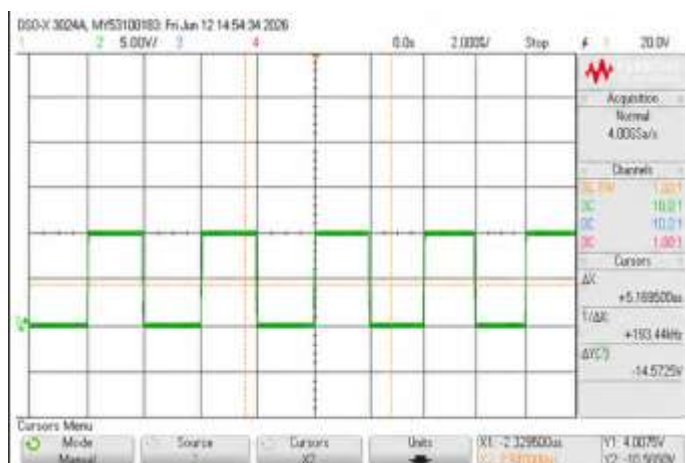


Fig. 15: V_{GS} at 50% Load

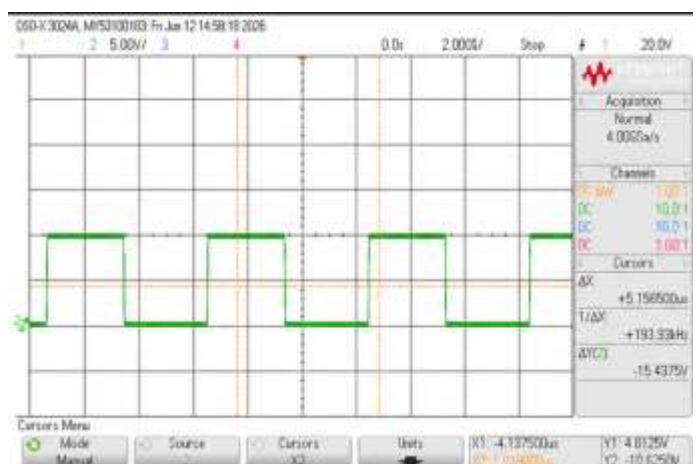


Fig. 16: V_{GS} at 100% Load

v) Output Voltage Ripple

Table 6 and Table 7 presents the measured peak-to-peak output ripple voltage for Output 1 and output 2 at the three input voltages and load conditions.

Table 6. Output Voltage Ripple for Output 1 (Peak-to-Peak, mV)

Vin (V)	10% Load	50% Load	100% Load
65	3.84 mV	10.4 mV	18.0 mV
68	5.2 mV	11.4 mV	23.6 mV
70	7.8 mV	14.4 mV	47.2 mV

Table 7. Output Voltage Ripple for Output 2 (Peak-to-Peak, mV)

Vin (V)	10% Load	50% Load	100% Load
65	2.72 mV	9.4 mV	16.0 mV
68	4.2 mV	11.4 mV	19.6 mV
70	6.8 mV	15.4 mV	40.3 mV

Maximum ripple is 47.2 mV for Output 1 (at Vin = 70 V, 100% load), which is well within the specification of 100 mV. As the input voltage and the load current was increased the ripple also increased. However the peak ripple were within the specification limits (100mV), indicating that the LC filter design is suitable for effective ripple suppression across the operating ranges.

Vi)Line and Load Regulation

Table 7 and Table 8 present the line and load regulation results respectively.

Table 7: Line Regulation Results (Specification: $\pm 1\%$)

Output	10% Load (%)	50% Load (%)	100% Load (%)
+5 V Output	0.00	0.02	0.06
+3.3 V Output	0.00	0.00	0.00

Table 8: Load Regulation Results (Specification: $\pm 1\%$)

Vin (V)	+5V Reg. (%) (20–100% load)	+3.3V Reg. (%) (3–100% load)
65	0.00	0.00
70	0.00	0.00

The Output1 line regulation is 0.06% at 100% load and 0.00% at 10% and 50% loads well within the $\pm 1\%$ specification. In Output 2, line regulation is 0.00% for all load conditions, indicating that the LDO post-regulator can suppress input voltage changes. The load regulation is 0.00% for both outputs at all input voltages. This indicate that the linked inductor topology and closed-loop feedback work well to accommodate load changes from 20% to 100% of rated current.

vii)Efficiency

Table 9 presents the measured converter efficiency at the three input voltages and load conditions.

Table 9: Efficiency of the Proposed Converter (%)

Vin (V)	10% Load	50% Load	100% Load
65	65%	75%	78%
68	67%	70%	78%
70	65%	71%	78%

All three input voltages reach a maximum efficiency of 78% at full load (100%). The efficiency is lower (65-67%) at light load (10%) because of higher switching losses and the static power drawn by the control circuitry constitutes a bigger portion of the output power. At 65 V and full load, the highest efficiency of 78% is achieved, indicating optimal operating conditions near minimum input voltage. The slight efficiency variation with input voltage is attributable to changes in MOSFET switching losses and transformer core losses with duty cycle variation.

The proposed work demonstrates dual-output capability with LDO post-regulation, coupled inductor topology, and a more comprehensive protection suite (ICL, UVP, OCP), making it better suited to multi-subsystem space power supply units.

VIII. CONCLUSION

This paper presents successful design and implementation of a high-reliability dual-output forward converter particularly for space applications. The Simulation and experimental were comparable. Evaluation demonstrated that the developed converter maintains the line and load regulation of less than 1% across all operating conditions. Operating from an input voltage range of 65V to 70V, the topology reliably delivers stable 5V and 3.3V outputs with a voltage ripple within 1%. Achieving an efficiency of 78%, the performance metrics satisfies all design specifications. The robust regulation and low ripple profile confirm that the proposed power supply is highly suitable for implementation in spacecraft power environments.

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