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Design and Implementation of CMOS based SRAM Memory Array using SVL Technique At 28nm Technology

P. Sri Charan
UG Student, Dept. of ECE,
CMR College of Engineering & Technology,
Medchal, Hyderabad, Telangana, India.

N. Sai Deepak
UG Student, Dept. of ECE, CMR College of Engineering & Technology, Medchal, Hyderabad, Telangana, India.

Vemula Panduranga
Associate professor, Dept. of ECE,
CMR College of Engineering & Technology,
Medchal, Hyderabad, Telangana, India.

***Abstract*: Random-Access Memory (SRAM), for decades, SRAM has been the most widely utilized memory technology. It can store information or data for as long as it desires. It is acceptable to call it a source of power since it is provided. Random-Access Memory employs latching circuitry to store data and preserve the bits MOSFETs help compensate for the SRAM cells. In addition, improvements withinside the System of Chip are essential. In this paper, we applied 28nm technologies to design a 64-bit low-power 7T SRAM Memory Array. SRAMs are extensively used in various registers, microprocessors, and perhaps other devices. Minimal memory banks, generalized computing applications, etcetera. We introduce the "self-controllable Voltage Level (SVL)" circuit. The number one purpose of the complete circuit is to decrease the standby leakage power of a 7T SRAM. We have also stimulated the read and write operations waveforms of the circuit. We also used SVL technology to analyze the power consumption between standard 7T SRAM cells and the leakage power and current parameters. The Cadence Virtuoso simulation tool was employed in our project.**

Keywords— Leakage current, Low power dissipation, static random-access memory (SRAM), and self-voltage level control (SVL).

I. INTRODUCTION

SRAM cell is a high-speed memory cell that is used for high-speed applications like buffers and caches. The reason SRAM is used in this application is that it is faster than DRAM which is also used as a memory cell but it is constituted of capacitors while the other hand SRAM is constituted of _transistors. Thanks to technological advancements we can now fabricate millions of transistors on a single chip. While this enabled us to achieve operations with reduced size, it is also important that their performance should be scaled according to the current needs. While this can be achieved with scaling there is an exponential increase in the leakage current which leads to increased power consumption thus decreasing the overall performance of the memory cell. Power utilization is also considered as of the main factors along with speed and cost. To overcome this, we employ an SVL (self-voltage level) circuit in connection with SRAM cells. In this paper we, will be looking at designing an 8x8 memory cell array consisting of 7T SRAM cells with the combination of SVL circuit with CMOS transistors at 28nm to overcome the extra power consumption because of the leakage current.
All the schema implementations are performed on cadence virtuoso at 28nm technology.

II.7T SRAM CELL

A 7T SRAM cell incorporates seven transistors: five NMOS transistors, two of which are access transistors, two of which are employed to manufacture cross-coupled inverters, and one of which is paired with a feedback transistor, It has a similar architecture to a 6T SRAM cell, but it incorporates an additional NMOS circuit wired as a feedback transistor.

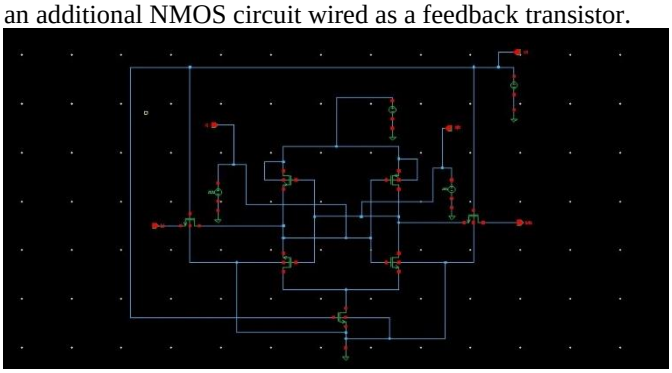

Figure 1: 7T SRAM memory cell

III. SVL METHODOLOGY

As an example, in the case of a battery-powered portable system, many power-saving methods are illustrated as in CMOS, you may get Threshold Voltage and Variable Threshold CMOS. This approach helped me decrease. It is effective to use a high Vt MOSFET switch that insulates the power supply.

When this strategy is employed, reminders and flip-flops have the disadvantage of not being saved data. In other strategies, an adjustable threshold voltage uses CMOS and decreases power by enhancing power. The data will be skewed.

The following are the downsides of this technique Power usage and large-scale issues. As a result, a mechanism referred to as self-voltage level (SVL) is suggested. Inactive mode, the circuit allows for full supply. The voltage as well as the lower supply voltage. It is also possible to lower the gate leak current.

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It generates power when the circuit is in an idle state. a low voltage and a comparatively high voltage "OFF MOSFET" decrease V sub through the "ON" control. As a result, Vth rises. As a result, the subthreshold current falls. SVL circuits are classified into three types.

The first circuit represents the upper SVL circle, The second circuit is the lower SVL circuit and the third circuit represents a combination of both. This technique is suitable for standby mode lines such as leakage power is less than other Techniques.

IV. 7T SRAM CELL INCLUDING SVL METHOD PROPOSED

A 6T Static random memory cell and an additional NMOS transistor Cell are included in the 7T SRAM mobileular. This additional transistor is positioned inside the floor direction to reduce leakage while the cellphone is in standby mode. Q, BLB, and BL alternatively charged as well as discharged, as well as the phrase wire throughout the additional transistor, to write 1 to the ground terminal output.

One more PMOS transistor may be switched on, yielding 1 at q b, and q can be charged to 0 via the NMOS transistor. Likewise, if q is 1 and q b is 0.

A. READ OPERATION.

To conduct the research procedure, the SRAM phrase line must not be controlled. Memory must first contain some data to conduct a read operation. Consider memory with q is 1 and memory with q is 0.

Add a word line to the head of the line. If the available voltage across the node is Vdd 1, the bit and bit b output traces are charged first. Because each q and bit line are too high, In the circuit, there is no discharge. When q is 0, there is a voltage divergence between "q" and the terminal voltage at b, which drives the voltage at b to collapse.

The circuit discharges as a result of the power passing through it. The bl and bit blb are combined with a sense amplifier. As of result, when the bit line is lower, the outcome is Finally, the answer is 1.

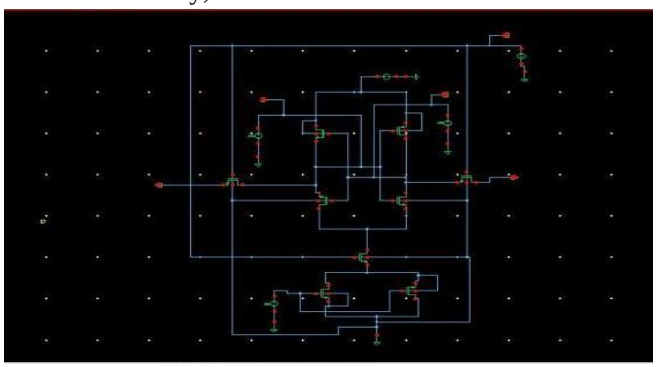

Figure2: Schematic for reading Operation using SVL

B. WRITE OPERATION

Let us use q as 0 and q' as 1 in the read operation. The word bit is remarkably high, allowing you to do write operations. Input lines for write operations are b and a bl'. Connect pin b to the ground initially because you have command over the bit line.

As a result, a voltage divergence among q' and b can be achieved. p1 must be higher than P2 in addition to writing 1 to the Memory cell. This may be accomplished by adjusting the ratio of the transistor. Finally, q equals 1. Following the operation q as 1, the first q as 0 occurs, followed by the Memorization success in the SRAM cell.

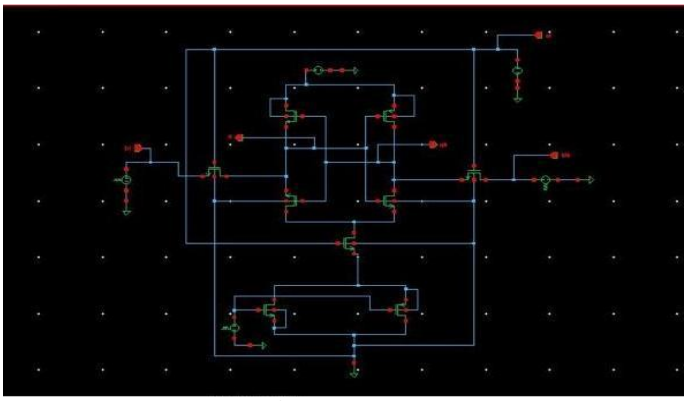

Figure 3: Schematic for writing Operation using SVL

C. SENSE AMPLIFIER

We use a sense amplifier for the read function for the SRAM cell this sense amplifier is an important aspect of the memory cell since it is used to read data from the cell and this operation has to be fast and accurate for the efficient working of the memory cell, for this reason, we will be using a current sense amplifier which gives us about 20% faster sensing speed compared to commonly used voltage sensing it also the current sense amplifier spent around 16-19% lower power than that of the voltage sense amplifier, but its construction is complicated.

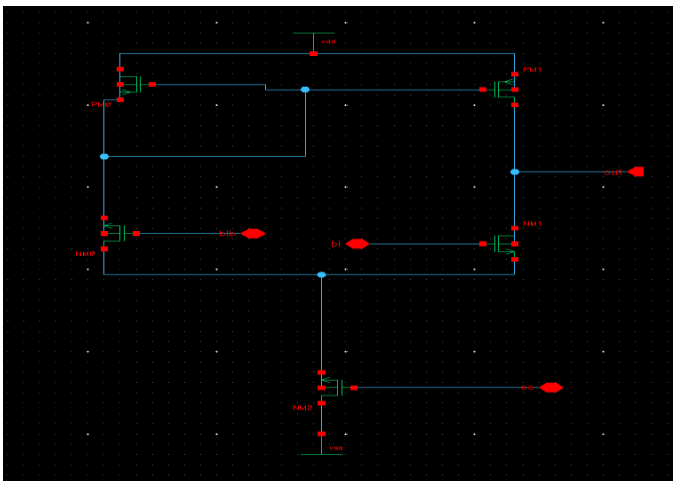

Figure 4: Sense Amplifier

D. PRECHARGE CIRCUIT

The precharge circuit is a critical component that is used in an SRAM memory cell array construction, it's before we begin operations on the memory cell, our responsibility is to charge the bit lines bl, blb to the greatest voltage possible., to achieve this we will be using a precharge circuit which is schema is depicted below

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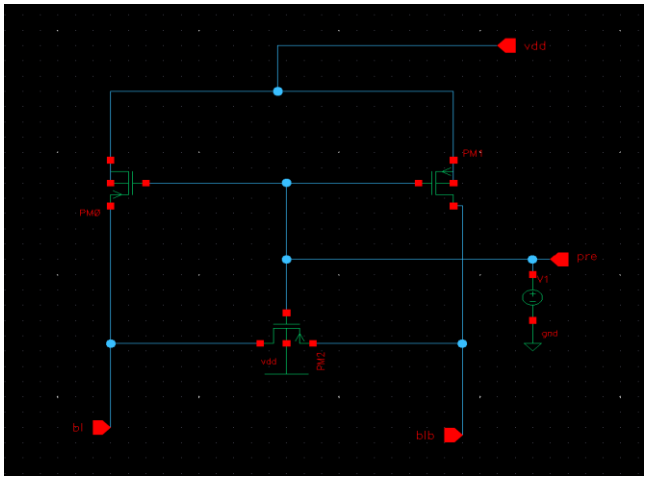

Figure 5: Precharge circuit

E. Row Decoder

The decoder is a crucial component of the SRAM cell array. since it is used to select a single memory cell that has to be operated on the 3:8 decoder is used as row decoder and column decoder for our 8X8 memory cell array this has 3 input lines and 8 output lines which are fed to the memory array.

Row and column decoders work together to pick a specific memory cell in the memory array. The row decoder is used to pick a specific row in the memory array that must be activated by connecting to the memory cell's worldline. The figure below shows the designed 3:8 decoder and its truth table to select a single cell by using different combinations.

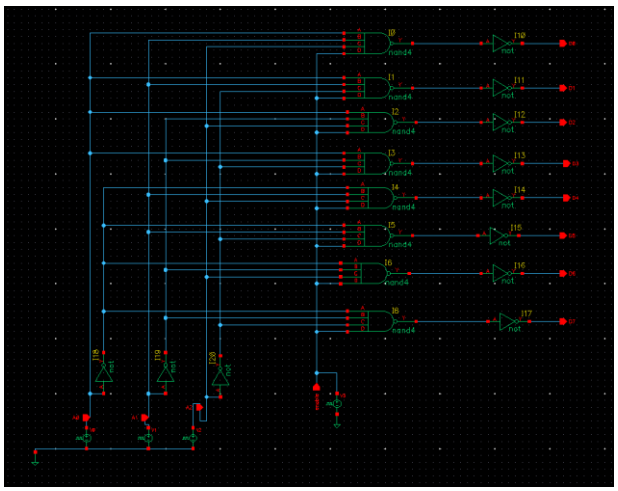

Figure 6: 3X8 Decoder

F. Driver Circuit

The Write Driver is responsible for writing data into memory. The driver's task is to get the b and bl bars towards the ground so that the alternate function may begin. Word line(wl) enabled controls whether the Write Driver has access to the bit line. The term enable is used in the upper area of the circuit to allow the driver to work. It is divided into two NMOS transistors that are linked fascinatingly one after the other. In the upper section, there are two major inverter junctions.

To begin, two logics are assigned to the two points of the junction: 0 and 1. The bit line next to the 0 logic is discharged first, followed by a logic flip. As a result, the bit line and bit line b bars are discharged to the ground. Its main task is to keep a low connection to the ground.

As a result, the bit line and ground, as well as the bl and ground, have no voltage imbalance

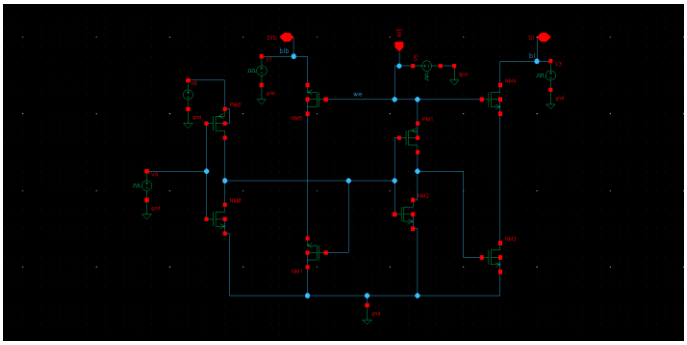

Figure 7: A driver circuit

G. 8*8 ARRAY LOGIC

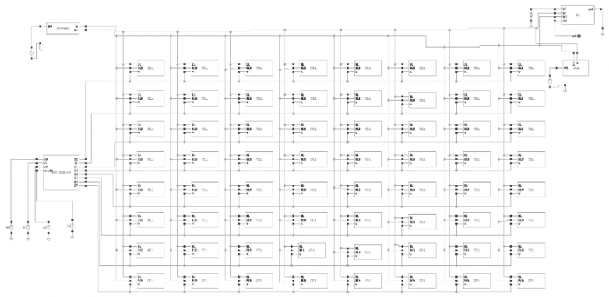

Figure 8: Schematic of 8x8 memory array

The array is fabricated via 28nm technology. The basic 8X8 Memory Array, seen above, can carry 64 bits of data. There are eight pre-charge circuits and eight write circuits in each column. Eight sensing amplifiers, and eight drivers These eight rows and columns. To choose a certain row, a 3:8 Row decoder is employed. As a result, just one cell is active at any given time, allowing us to do certain tasks. Procedures to read and write.

V. SIMULATION RESULTS

We compared the findings to a conventional 7T SRAM memory cell utilizing the SVL Technique with a standard 7T SRAM cell.

Parameter Name	7T SRAM	7T SRAM(SVL)
Power consumption	Read-0.771uW Write-0.063uW	Read-0.435uW Write-0.049uW
Current consumption	Read-0.514uA Write-0.107uA	Read-0.311uA Write-0.0375uA
Leakage power	35.2nW	19.32nW
Leakage current	50.26nA	27.6nA

Table 1: Comparison between Standard 7T SRAM and 7T SRAM Using SVL Technique

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In the above table, we have seen tremendous change in the parameters when we compared using the SVL technique. While using a 7T SRAM with SVL, we can plainly observe that it is more efficient.

VI. CONCLUSION

After generating the schemas in the cadence virtuoso and simulation the components. It is observed that the 7T SRAM cell with an SVL circuit has shown a very drastic decrease in the less leakage in comparison with the normal 7T SRAM cell even though it results in a slight increase in the area of the cell it compensates through its lower current leakage reduction which results in lesser power utilization.

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