Design and Implementation of Clock and Data Recovery Circuits for High Speed Serial Data Communication Links

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Abstract— The unquenchable thirst for high speed serial data communication requires the operation of transmission links at speed in Gigahertz range. Maintaining the signal integrity at such speed is a tough task. This paper presents the design and implementation of high speed phase lock loop based clock and data recovery circuit. The CDR architecture is realized using a conventional 45nm digital CMOS technology and operates between 900Mbps to 1.2Gbps data rate. The entire circuit is designed with single 1.1V power supply. The overall power consumption is estimated as 2.4mW at 1.0GHz sampling rate and the VCO locking time is found to be less than 10ns.

Keywords—CDR circuits, PLL, 45nm CMOS technology.

I. INTRODUCTION

The increased use of internet for audio and video transmission has led to global demand for high speed data communication links. The data are transmitted by the transmitter without any accompanying clock and the receiver needs to sample the data by recovering clock at their end synchronously. In high speed system, the data are corrupted by various noises, internally and externally in the link between transmitter and receiver. Due to this, jitter and skews are formed at the receiver. Thus there is a need of CDR circuit to recover the data received from corrupted signal and also to extract the accompanying clock information. This is done by the receiver by phase aligning the reference clock to the transitions of the incoming data. The CDR here is realized using phase lock loop. A PLL is essentially negative feedback loop that locks clock phase and frequency of input data to the reference signal.

The two main functions for performing CDR are:

- Frequency detection
- Phase alignment

A. Frequency Detection

It is a process where frequency is retrieved from incoming data. The time difference between two consecutive edges on data stream is detected.

B. Phase Alignment

Phase alignment is a process where phase of a signal with is matched with another. In CDR circuits the phase of clock recovered is aligned with the incoming data.

Figure 1 is the block diagram of CDR circuit based on phase lock loop. Here, Data is the input signal. If the sampling rate of input Data changes, the phase frequency detector (PFD) detects the phase and frequency differences between input reference signal and the feedback signal. It then generates error signals namely up and down signals.
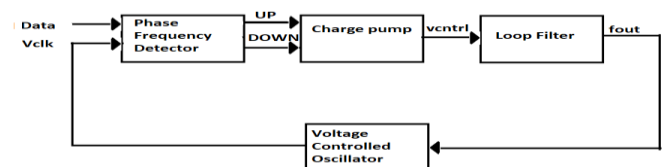

Fig. 1. PLL based CDR circuits

The UP and DOWN signals generated from the PFD is sent to the charge pump. The amount of charge to the loop filter is increased or decreased by the charge pump. The signal from charge pump is filtered by the loop filter and that is used to control the voltage controlled oscillator (VCO). The charge either speeds up or slows down the voltage controlled oscillator. The loop continues this process until the phase difference between the input reference signal and the feedback signal is zero or constant, that is the locked state. After the loop has achieved a locked state, the output of each component stays constant even though the process continues. The output signal has the same phase and frequency as the input reference signal.

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II.   PROPOSED ARCHITECTURE

The proposed architecture of various components used in the CDR circuit is discussed here.

A. Hogge Detector

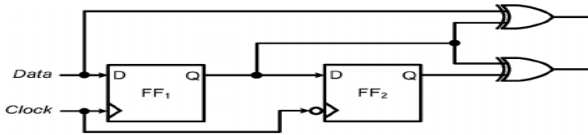Here we have adopted Hogge phase detector as shown in Figure 2.

Fig. 2.   Hogge Detector

This detector has two Master Slave D-Flip Flops and two E-XOR gates. The output of D flip flop will be delayed copy of input signal. The first D flip flop named FF1, generates delayed version of incoming data at positive edge of the clock synchronously.

The output from this FF1 is XORed with incoming data and this gives up signal. The down signal is generated using FF2 and XOR gate. Here 2 Delayed Flip Flops are used to avoid data pattern dependency problem. The reference pulses appear on the data edge and have fixed pulse width and data pattern dependency is avoided.
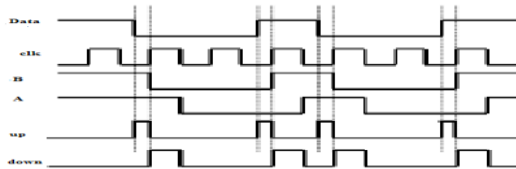

Fig. 3.   Waveform of Hogge detector

To get a better understanding, waveform of Hogge detector is illustrated in Figure 3. Signal B changes at clock edges. UP = Data XOR B gives pulses whose width are the phase difference between data and clock, and DOWN signal is given by A XOR B. The circuit produces UP and DOWN pulses for each data transition providing edge detection. Width of the output pulses varies linearly with input phase difference, suggesting that the circuit is linear PD under locked condition. The explicit edge detection which is carried out by DFF and XOR gate avoid skew in the decision circuit.

B. Charge Pump

Charge pump is the next stage to hogge detector. The simple block diagram of charge pump is shown in Figure 4.
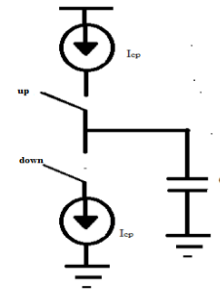

Fig. 4.   Charge pump

It is an electronic switch controlled from Hogge detector. The functionality of the charge pump is to translate the up and down signals from the Hogge detector to control the voltage that will control the voltage controlled oscillator (VCO). It is a DC to DC converter and uses capacitors to store the charges. It consists of two current sources. These current sources are switchable and used to drive the capacitive load. The main purpose of charge pump is to get analog signals suitable to control VCO from logic states of Hogge detector. The output of charge pump is given to loop filter which integrates the charge pump with the VCO.

C. Loop Filter

The loop filter shown in Figure 5 is the main component of PLL. It is necessary to choose the resistors and capacitor value correctly to lead the loop to locked state quickly.
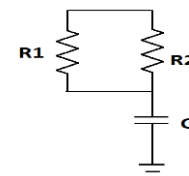

Fig. 5.   Loop Filter

Improper values lead the loop to oscillate for long without reaching the locked state. Small variations in the input data may cause the loop to unlock if loop filter fails.

D. Voltage Controlled Oscillator

An oscillator is a system that generates a periodic output. It is an independent device which takes no input signal. A voltage-controlled oscillator (VCO) is an electronic oscillator where its oscillation frequency is controlled by a voltage input. Here we have used CMOS ring oscillator as shown in Figure 6.
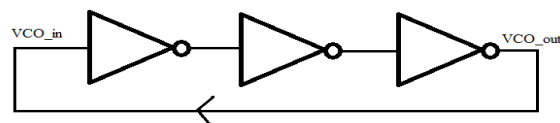

Fig. 6.   ring oscillator

The ring oscillators have a high frequency tuning range and small area consumption. The applied DC voltage controls the frequency of oscillation, while modulating signal can also be given to the VCO to cause frequency modulation. The

frequency of oscillation must be tuneable for the phase of a PLL to be adjustable. In inverter ring oscillator, the frequency can be adjusted by controlling the supply voltage. The function of the voltage controlled oscillator is to generate the clock signal at its output, the frequency of which can be changed by varying the input control voltage.

III.   PROJECT RESULTS

The output waveform of Hogge detector which consists of MSDFF and XOR is show in the figure 7 for input Data frequency of 1Gbps. The final output of the entire Phase Locked Loop based Clock and Data Recovery Circuit from the feedback of 11 stages VCO can be seen Figure 8 and Figure 9 shows the final layout of CDR circuits.
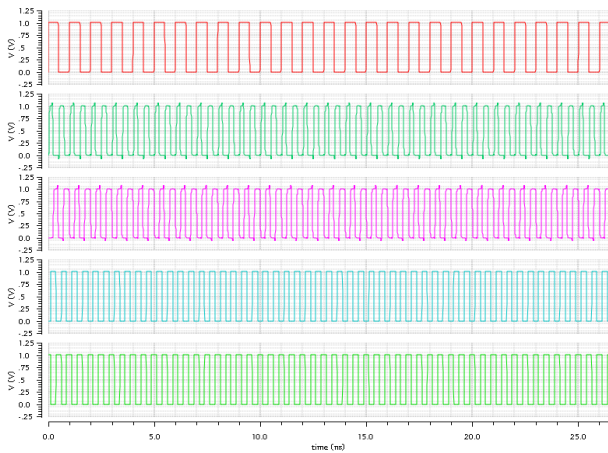

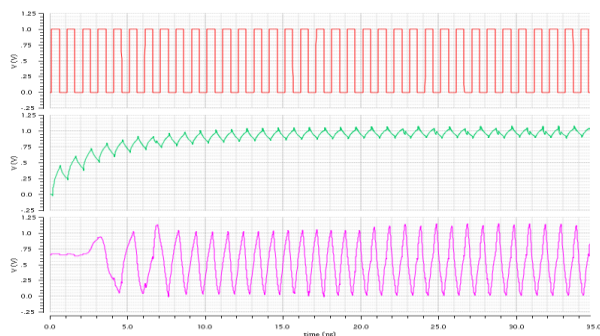Fig. 7.   Waveform of Hogge Detector
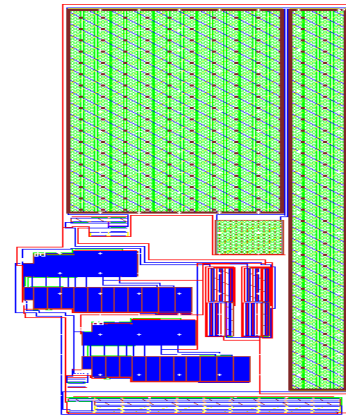

Fig. 8.   CDR Output Waveform

Fig. 9.   Layout of CDR Circuit

IV.   CONCLUSION

This paper presents an introduction to the PLL-based clock and data recovery circuits. The entire circuit is implemented at the transistor level. The design specifications are given in the Table 1.

TABLE I.   DESIGN SPECIFICATIONS

VLSI EDA Tool	Cadence Virtuoso
Technology	45nm
Power SUpply	1.1v
Locking TIme	<10 ns
Power	2.4mw
Operating range	900MHz to 1.2 GHz

V.   FUTURE SCOPE

The different components can be improved upon to have less noise, jitter and faster locking time at higher speeds. This would involve using different implementations such as the dual loop CDR, DLL and the digital CDR. The PLL based CDR offers good input jitter rejection but has stability issues. The DLL doesn't have jitter peaking or stability issues but has a limited phase capture range. Thus, a particular architecture should be chosen depending on the requirements.

- Use of lower process design technologies (22nm, 7nm) would yield better results.

- Designing newer architecture for greater data rates.

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