Design and Implementation of Built in Self Test (BIST) forVLSI Circuits using Verilog

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***Abstract*— Due to the rapid scale of integration in Integrated Circuit designs which has reached submicron technologies, testing has evolved to be a critical factor. Design engineers who do not design systems with full testability in mind open themselves to the increased possibility of product failures and missed market opportunities. In such a scenario where conventional testing approaches are often ineffective and insufficient, BIST has proven its worth.**

BIST is a design technique that allows a circuit to test itself. In this project the test performance achieved with the implementation of BIST is proven to be adequate to offset the disincentive of the hardware overhead produced by the additional BIST circuitry. The technique can provide shorter test time compared to an externally applied test and allows the use of low cost test equipment during all stages of production. The concept was designed and implemented with Xilinx ISE 14.2.

Keywords—LFSR, MISR, BIST controller.

I. INTRODUCTION

Testing plays a vital role in production and packaging of all consumer goods in this case VLSI circuits. A commodity has to be tested and certified OK by the producer before it is shipped to a consumer. However testing of VLSI components is far more different and complicated with respect to other consumer goods. As the scale of Integration rises rapidly the complexity of circuits also rises exponentially where testing methodologies are also forced to become far more complex. Testing of a normal VLSI circuit mainly involves application of test vectors to the Circuit under Test (CUT) and Analyzing the response. Under normal conditions, an equipment like ATE (Automatic Test Equipment) is used for these purposes. However the bulkiness of the equipment along with time constraints have proved them to be a liability rather than an asset. In this context we propose through this paper an Automatic On-Chip testing methodology-Built in Self-Test abbreviated as BIST which is a technology whose future scope extends to Self-Healing and other real time applications that involves high end error detection and testing.

A. *Why is Digital Testing Important ?*

The term Digital Testing is defined as “testing a digital circuit to verify that it preforms the specified logic functions in proper time.”[1].There are some fundamental differences that make VLSI circuit testing more important step to assure quality, compared to classical systems which includes the following,

1) The chip implementation has grown to sub-micron technologies integrating millions of trasistors and the speed of operations has crossed rates of GHz. This has further resulted in hardwares with very high complexities.Evidently, with more levels of integration there is a possibility of more number of faults.Just when a technology matures and faults tend to decrease, a new technology based on lower sub-micron devices evolves, thereby always keeping testing issues dominant.[1]

2) In case of detection of faults in a traditional system it is diagnosed and repaired. However, in case of circuits, on detection of a fault the chip is binned as defective and scrapped (i.e., not repaired). In other words, in VLSI testing chips are to be binned as normal/faulty so that only fault free chips are shipped and no repairing is required for faulty ones.[1].

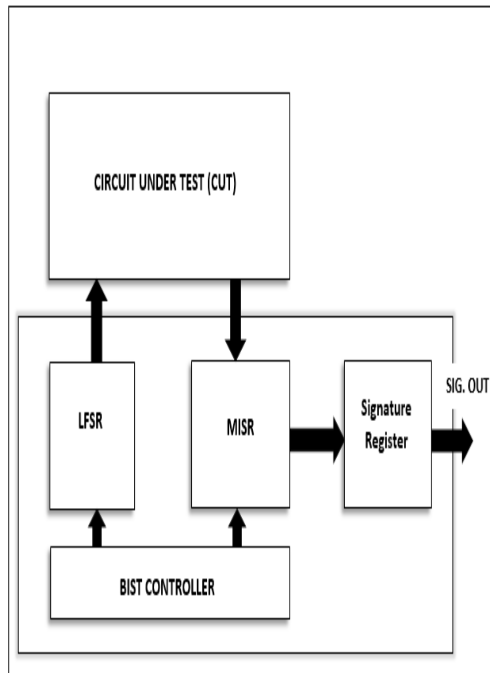
B. *Why BIST ?.*

ATE or Automatic Test Equipment is one among the conventionally used testing mechanisms. Several drawbacks of ATEs are rectified or enhanced through the implementation of BIST. These include, reduced testing and maintenance cost, reduced cost of Automatic Test pattern Generator (ATPG), reduced storage and maintenance of test patterns, Capability of testing multiple units in parallel, shorter test application times and the ability of the system to test at functional systems speeds and reducing the bulkiness of the systems.[2]

II. BIST ARCHITECTURE

The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. The test pattern generatorgenerates the test patterns for the CUT which is a Linear Feedback Shift Register LFSR, the response analyzer is a Multiple Input Signature abbreviated as MISR and the BIST controller which controls the LFSR and the MISR by makingNecessary decisions on what the bit length should be according to the CUT. The basic architecture is shown in Fig 1.

Fig.1 BIST ARCHITECTURE



A. *PATTERN GENERATOR or LFSR*

Test Pattern Generator(TG) and Response Monitor(RM) are often implemented by simple, counter-like circuits, especially linear-feedback shift registers (LFSRs).The LFSR is ann-bit shift register which pseudo-randomly scrolls between 2^n-1 values. It is a shift register formed from standard flip-flops, with the outputs of selected flip-flops being fed back (modulo-2) to the shift register's inputs. Like a binary counter, all 2^n-1 states are generated, but in a "random" order that is repeatable. The exclusive-OR gates and shift register act to produce a pseudorandom binary sequence (PRBS) at each of the flip-flop outputs. By correctly choosing the points at which we take the feedback from an n -bit shift register we can produce a PRBS of length $2^n - 1$, a maximal-length sequence that includes all possible patterns (or vectors) of n bits, excluding the all-zeros pattern.The all zeros case is not possible in this type ofLFSR because if the seed is all 0 state, then the LFSR will be stuck at all 0 state as the feedback logic is XOR gates.[3]

When used as a TG, an LFSR is set to cycle rapidly through a large number of its states. These states, whose choice and order depend on the design parameters of the LFSR, define the test patterns. In here we use the principle of Pseudo Random Pattern generation.[2].A string of 0's and 1's is called a pseudo-random binary sequence when the bits appear to be random in the local sense, but they are in someway repeatable.This pattern type, however, has the potential for lower hardware and performance overheads and less design effort than the preceding methods. In pseudorandom test patterns, each bit has an approximately equal probability of being a 0 or a 1[2].

For the ease of understanding we design a 3 bit LFSR given by the polynomial equation$x^3 + x^2 + 1$.

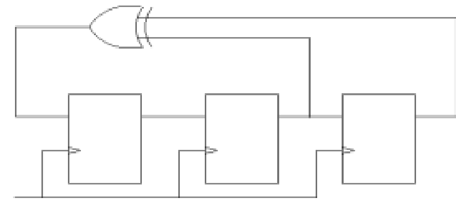


Fig 2 3-bit LFSR [3]

The feedback is done so as to make the system more stable and free from errors. Specific taps are taken from the tapping points and then by using the XOR operation on them they are feedback into the registers. The maximal length sequence of a 3 bit LFSR has been given in the following table 1.

Clock	$Q0_{t+1} = Q1_t \oplus + Q2_t$	$Q1_{t+1} = Q0_t$	$Q2_{t+1} = Q1_t$	Q0Q1Q2
1	1	1	1	7
2	0	1	1	3
3	0	0	1	1
4	1	0	0	4
5	0	1	0	2
6	1	0	1	5
7	1	1	0	6
8	1	1	1	7

Table 1Maximal-length sequence for the 3-bit LFSR[3]

B. *RESPONSE ANALYZER or MISR.*

An MISR or Multiple Input Signature Register performs the signature analysis in the system. Signature analysis is important because good and faulty circuits generate different signatures. The signature values are compared in the end to affirm if the CUT is to be certified tested OK.

The Pseudo-Random Pattern Generator generates the necessary patterns which are fed as inputs to the CUT. The response of the CUT is fed to an MISR. The MISR compacts all outputs into one LFSR thus reducing the amount of hardware required to compress a multiple bit stream.There are several ways to connect the inputs of LFSRs to form an MISR.Since the XOR operation is linear and associative, (A⊕B) ⊕C = A ⊕(B ⊕C), ,as long as the result of the additions are the same then the different representations are equivalent. If we have an n -bit long MISR we can accommodate up to n inputs to form the signature [3]. MISR can be generated using the similar equation used in the case of an LFSR i.e. $x^3 + x^2 + 1$.

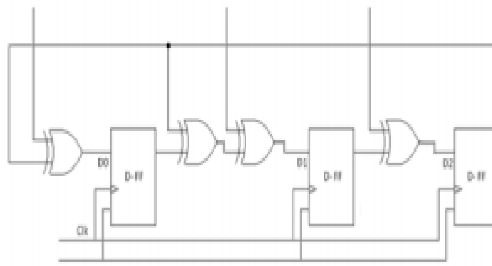


Fig 3 .MISR with 3 input and 3 output bits [3]

C. CIRCUIT UNDER TEST

The circuit under test is the test circuit which is placed for testing. Initially a perfectly working circuit is placed in the chip socket which is placed off-chip with respect to the parent chip housing the LFSR, MISR, Signature register and the BIST controller. Once there is a need of testing the required circuitry is connected to the parent chip and is run.

D. BIST CONTROLLER

The Controller controls the LFSR and the MISR according to the specification of the CUT. LFSRs and MISRs of necessary bit sizes are already stored in the LFSR and MISR sections. Before connecting the CUT the number of inputs and outputs of the CUT are specified. Accordingly the Controller calls the required bit-sized LFSR and MISR.

E. SIGNATURE REGISTER

The Signature register stores signature values generated by the MISR. Finally by comparing the signature value generated by a good and faulty circuit are compared to verify f the CUT is good or faulty.

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III. HOW THE SYSTEM WORKS ?

The Clock and reset inputs are given as input to the parent chip. The necessary bit lengths are also given as inputs to the Controller. A faultless circuit is placed initially in place of the circuit under test. The system is run and a signature value is generated for the circuit. Another circuit of the same type-say a faulty circuit- is provided at the CUT and the system is run. Another signature value is generated. If the signature values of both the circuits matches then the CUT is faultless. On the contrary if they don't match then it is evident that there is a fault present in the newly introduced circuit.

A. Simulation Results

1) The simulation results for getting the signature value keeping the check value =0 and running the functionality circuit has been given below in fig 4.The result for check value =1 running the test circuit to verify if the signature value is the same as in fig 4 is illustrated in fig 5.

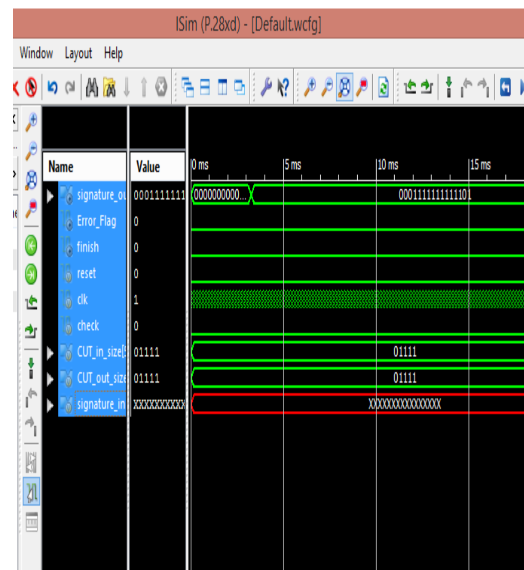

Fig 4

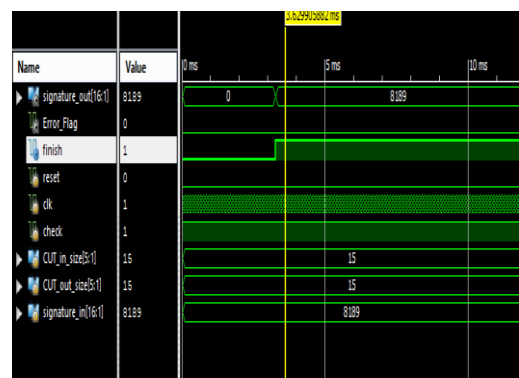

Fig 5.

The RTL schematic of the entire testing block is shown in Fig. 6 and that of the BIST controller alone is shown as per the fig 7.

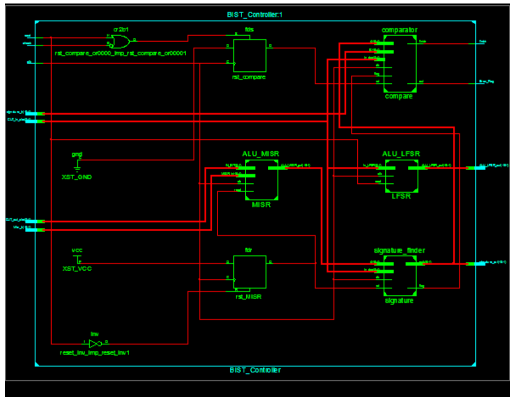

Fig 6.

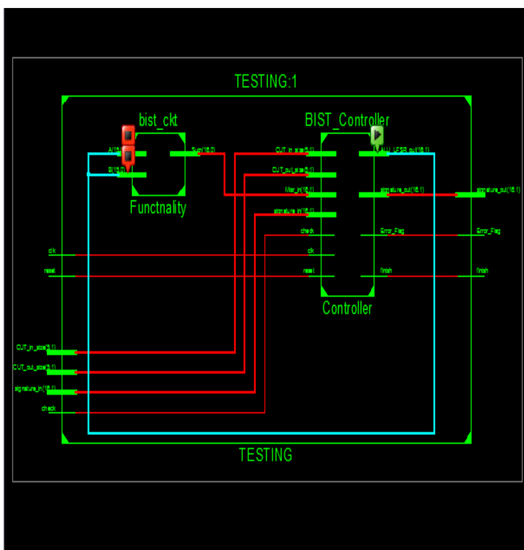

Fig 7

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