Design and Implementation of ALU Chip using D3L Logic and Ancient Mathematics

Mohanarangan S
PG Student (M.E-Applied Electronics)
Department of Electronics and Communicaiton Engineering
Sri Venkateswara College of Engineering
Pennalur, India

Dr. G. A Sathishkumar
Professor
Department of Electronics and Communicaiton Engineering
Sri Venkateswara College of Engineering
Pennalur, India

***Abstract* — Central Processing Unit (CPU) is the heart of personal Computer, which is converts data into information and set of electronic circuitry that executes stored data instructions. Major parts of any Central Processing Unit(CPU) is Arithmetic Logic Unit(ALU), Memory Unit and Control Unit(CU). Arithmetic Logic Unit(ALU) is the integral part of computer processor, that perform arithmetic and logical operations. Control Unit(CU) is the part of the hardware that's directly communicates with other parts of the hardware. A Proposed new logic family of low power dynamic logic called Data Driven Dynamic logic(D3L). In this logic family, the synchronization clock has been removed from P transistor and maintaining one or more clock signal. Vedic Mathematics is the ancient mathematics which has a unique technique of calculations. It is based on 16 Sutras which are discovered by Sri Bharti Krishna. Urdhva Tiryakbhyam sutra's eliminates the unwanted multiplication steps thus reducing the hardware complexity in terms of area and speed and hence reducing the propagation delay in processor chip. We implement a 64-bit ALU chip design Vedic multiplier based on Urdhva-Tiryagbhyam Sutra. A Proposed Driven Dynamic logic(D3L) and Ancient mathematics plays a vital role in Central Processing Unit(CPU) and Arithmetic Logic Unit(ALU) design, a great extent when it comes to very low power consumption implementation of Central Processing Units, Microprocessors and Signal processing in satellite GPS based systems Disaster management system.**

Keywords—Data Driven Dynamic Logic; D3L; System On Chip; Vedic Mathematics; Urdhva Triyakbhyam Sutra

I. INTRODUCTION

Arithmetic Logical Unit is the very important subsystem in the Central Processing Unit and digital system design. An Arithmetic Logic Unit (ALU) is an integral part of a computer processor. It is one of major part of Central Processing Unit which perform arithmetic and logic operations. Bit-widths of ALU are frequently required in very large-scale integrated circuits (VLSI) from processor to application specific integrated circuits (ASICs). ALU is getting smaller and more complex nowadays by using normal AND, OR, NAND etc.., Existing implementation of ALU chip design based on logic gate circuit design comparatively slower because, normal logic gate consumes more power, area and delay.

This paper proposes two methods of designing ALU chip. First, designing a ALU chip using Transistor logic families of CMOS circuits. Second, Implementation of ALU chip using Vedic Mathematics based on Urdhva- Tiryagbhyam Sutra. A New ALU chip design is proposed using D3L logic and Vedic mathematics operations which is based on Urdhva Tiryakbhyam sutra's. The proposed ALU chip design and its performance metrics of speed, power consumption, delay and area were compared with the existing ALU designs using schematic editor DSCH and layout editor Microwind and simulation of Verilog HDL program using Modelsim. This paper is organized as, section 2 and 3 are deals with brief discussion on ALU design using Data Driven Dyanamic Logic (D3L) and Vedic mathematics. The proposed architecture of ALU chip and its implementation methodology is dealt in section 4. Discussion on result is stated in section 5. Section 6 concludes the work with the scope for the future enhancement.

A. Features of ALU

We have designed the 64-Bit ALU which certain features as follows:

- Low-power CMOS Process Technology
- Total 16 arithmetic operations like add, subtract, multiplication, plus, shift, plus 12 others
- Total 16 logic operations like XOR, AND, NAND, NOR, OR, plus 11 others
- Capable of active-high and active-low operation.
- Full carry look-ahead for high-speed arithmetic operation.
- Arithmetic operations expressed in 2s complement notation.

B. MAJOR PARTS OF ALU

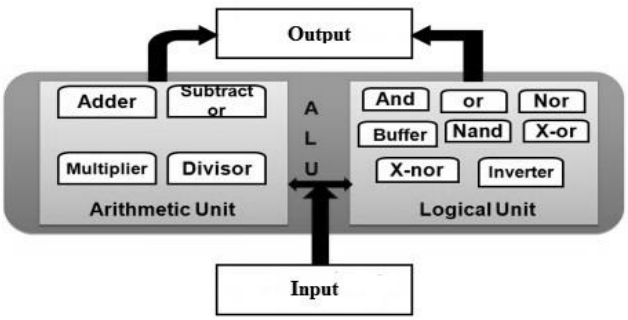


Fig. 1 Basic Arithmetic Logic Unit

Arithmetic Block

It is used to perform arithmetic operations such as addition, subtraction, multiplication and comparison. The core

of the arithmetic block is an adder, subtract, multiplier and Divisor. In the architecture presented in Figure 1.1, the adder uses half adder and full adder.

Logic block:

It is used to perform simple bit wise logic operations such as AND (masking), OR and XOR, XNOR, NAND, NOT and etc.

Multiplexers:

MUX is a digital switch and also called a data selector. It allows digital information from number of sources to be routed onto a single output line. The basic multiplexer has several data-input lines (2^n) and a single output line (n). The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n inputs and n selection lines whose bit combinations determine which input is selected. Therefore, MUX is "many into one" and it provides the digital equivalent of an analog selector switch.

II. PROPOSED ARCHITECTURE OF ALU USING DATA DRIVEN DYNAMIC LOGIC (D3L)

In dynamic logic, either the Pull Down Network (PDN) or the Pull Up Network(PUN) of static logic is removed. In this logic style, the inputs given during precharge phase must be low. The conclusion is that if the gate can be precharged with a set of input data, then there is no need for a clock signal. Such a case of using data for precharging other than clock signal for precharging is known as Data-Driven Dynamic Logic or D3L.

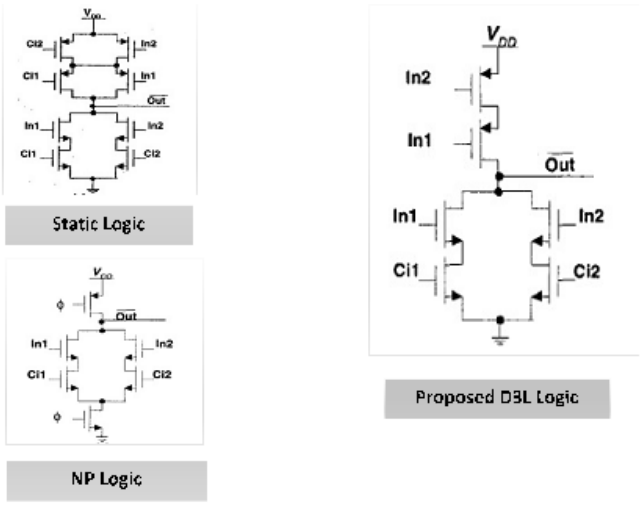


Fig. 2 Introduction of Proposed D3L Logic

In D3L the clock signal is replaced by one or more inputs. Static cmos logic utilizes pmos transistors in the pull up network and nmos transistors in the pull down network. The important characteristic of cmos logic is low power dissipation. But the number of transistors is more and static logic is comparatively slower. Unlike static logic, dynamic logic uses a clock signal and hence there is clock power dissipation. Data Driven Dynamic (D3L) logic reduces clock power dissipation in dynamic circuits. The question is whether Data Driven Dynamic Logic (D3L) logic can be used in place of static logic to improve the performance. In this project, an ALU which is a commonly used processing element was chosen. A one bit ALU was first implemented using static CMOS logic to obtain power dissipation, delay and area. Then ALU was implemented using D3L logic to obtain power dissipation, delay and area. Then a four bit ALU was implemented using both the logics. The performance was compared and conclusion was made such that D3L logic has better performance than static logic. we describe D3L design concept. In creation of conventional dynamic logic, a set of conditions is imposed on dynamic blocks. These conditions are arranged such that the logic transistors stay in *off* state during the precharge time. This condition is necessary for correct operation at the beginning of the evaluation phase and prohibits the output node from accidental discharge. In D3L, we use these existing conditions to find a replacement for the clock signal.

A. DESCRIPTION:

In general, for D3L designs, when we have a function *F in the* sum-of- products form

$$F = \sum_{i=1}^{n} P_i \qquad (1.1)$$

The minimum **Pi** (the P; with a minimum number of literals) is selected in such a way that:

- If in the precharge phase, all of inputs have a low value (the Domino condition), the minimum Pi is used to replace the clock in PUN and the main function is made in PDN.
- If in the precharge phase, all of the inputs have a high value (the NP-CMOS condition) the minimum P, is used to replace the 5 in PDN and the main function is made in PUN.

B. ARCHITECTURE

The design of a 64 bit ALU considered here is assumed to perform eight functions that include two basic arithmetic operations such as Addition, Subtraction and six logic operations such as NOR, NAND, OR, AND, XOR, and Invert. Different transistor logics are employed for different functions based on the advantages offered by each logic families. The criteria for selecting different logic families for optimum performance of the ALU are discussed below. The very important part of the ALU which determine the overall performance of the design is the full adder for the arithmetic operations. The basic logic circuit of the full adder is the EXOR logic gate. The subtraction operation can be performed as addition of negative numbers. The negative number can be derived using inverters the output of which is one's compliment and input carry to the LSB is made logic one to obtain the two's compliment of the subtrahend. An efficient method using multiplexer is employed for the ALU design which uses less power as well as delay. Multiplexers are also tested for good zeros and ones at the output.

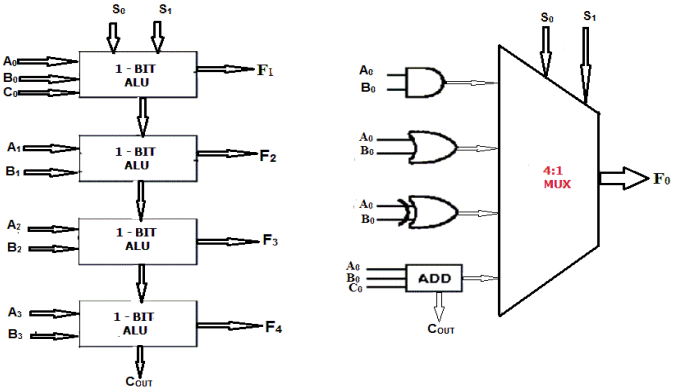


Fig. 3 Proposed 4 bit ALU Block Diagram.

The block diagram of a four bit ALU derived using four single bit ALUs performing four functions is shown in fig. 3. Each module of the 16 bit ALU is designed individually to give the optimum overall performance i.e. to minimise overall delay and power consumption. The basic logic operations are implemented using the conventional CMOS logic gates. The 8 to 1 Multiplexer to select one among 8 arithmetic and logic operations is implemented using D3L logic. It gives the advantage of reduced area. As the multiplexer is always operational, reduced delay and power consumption is preferred over other parameters.

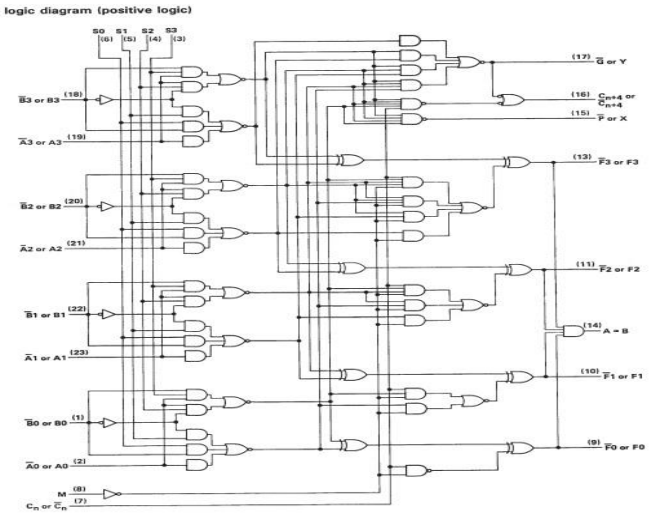


Fig. 4 64-bit ALU Logic Diagram

III. PROPOSED ARCHITECTURE OF ALU USING DATA DRIVEN DYNAMIC LOGIC (D3L) AND ANCIENT VEDIC MATHEMATICS

Urdhva-Tiryagbhyam is one of the sutra from 16-Vedic sutras which performs the multiplication operation of two decimal numbers. Urdhva-Tiryagbhyam is the general shortcut formula applicable to all cases of multiplication of one number by another number. "Urdhva" means vertically and "Tiryagbhyam" means crosswise therefore it is also called as Vertically and Crosswise Algorithm.

A. RULE:

"Vertically and cross wise"

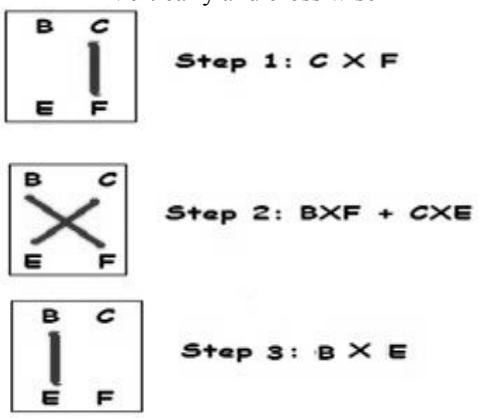


Fig. 5 Urdhva Tiryagbhyam for two-digit Multiplication

IV SIMULATION AND IMPLEMENTATION

A. SIMULATION RESULT OF D3L LOGIC

Individual arithmetic circuits such as Adder, Subtractor, and logic functions such as AND and OR are independently verified at transistor and gate level Each of the modules are then integrated to form a single bit ALU initially. The single bit ALU circuit is simulated to determine its propagation delay and power consumption. The single bit Arithmetic logic units are appended to obtain a 4 bit Arithmetic logic unit and further extended to 16 bit ALU and 64 bit ALU.

Microwind and DSCH Software from Microwind Inc. is used for the design and simulation of the circuits at IC layout level upto 45nm process technology. Microwind IC Layout editor integrates the frontend and backend chip design into an integrated flow, accelerating the design cycle with reduced design complexities. It tightly integrates mixed signal implementation with digital implementation, transistor level extraction, circuit simulation and verification. Performance parameters like area, power consumption and propagation delay can be analyzed conveniently using this software. The Verilog file of the validated circuit schematic in DSCH is extracted and complied in Microwind to obtain the IC layout using specific process technologies. The parasitic capacitance, inductance, resistances and crosstalk between adjacent paths have been considered while carrying out simulations, by varying the W/L of the PMOS and NMOS transistors for design optimization. The design is simulated using an 8pF capacitive load.

A. 4 Bit ALU

The power and delay report from the simulations are recorded and analysed. An optimum 4 bit ALU IC layout is developed and its architecture is verified using the schematic editor DSCH in different CMOS process technologies. The IC chip level simulation is carried out using Microwind.

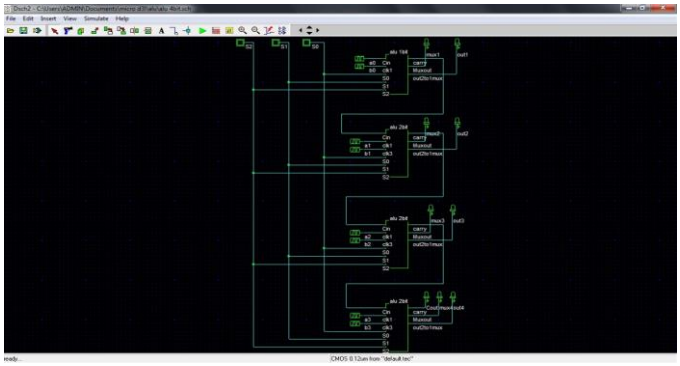


Fig. 6 Schematic Diagram For 4-Bit ALU

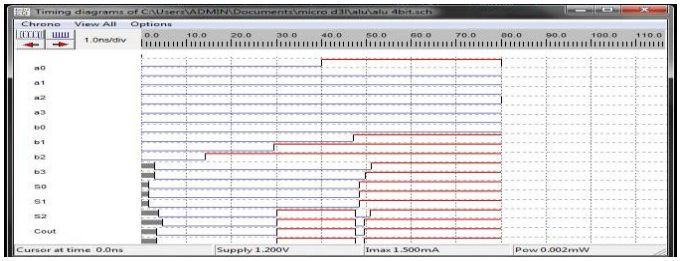
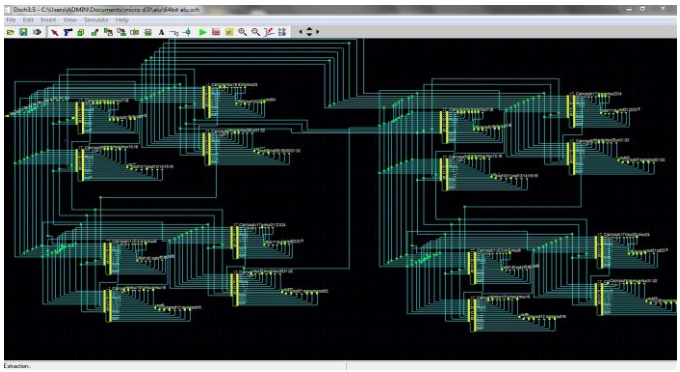


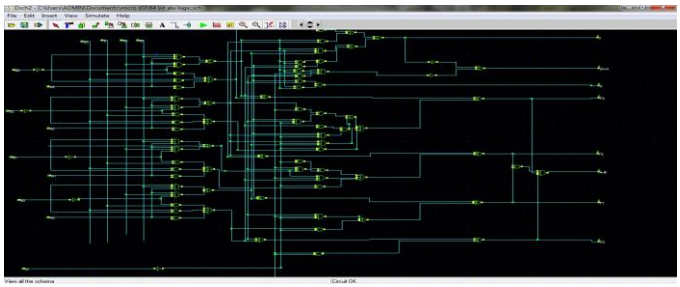
Fig. 7 Simulation Result For 4-Bit ALU

B. 64 Bit ALU

After comparing 4 bit logic ALU and ALU using D3L logic, 16 bit ALU was considered. For design entry, 4 bit logic and D3L ALU was converted into symbolic form. AND, OR, NOT gates and Full Adder were converted into symbols to obtain a block as shown in Fig.1.7. Each block represents 16 bit ALU. Four blocks were used to implement 16 bit ALU. Working is similar to that of 4 bit ALU.



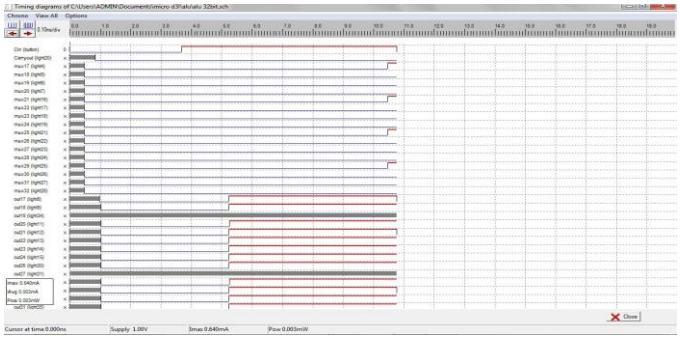
a. D3L Logic – 64 bit ALU



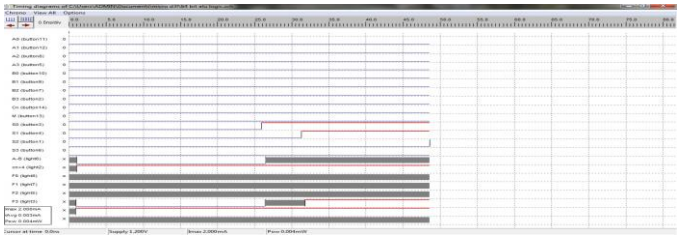
b. Logic gates – 64 bit ALU

Fig. 8 Comparison of D3L and Logic Gates Schematic Diagram for 64 bit ALU

The power and delay report from the simulations are recorded and analyzed. An optimum 64 bit ALU IC layout is developed and its architecture is verified using the schematic editor DSCH in different CMOS process technologies. The IC chip level simulation is carried out using Microwind.



a. D3L Logic – 64 bit ALU



b. Logic Gate – 64 bit ALU

Figure 1.7 Comparison of D3L and Logic Gates Circuit waveform for 64 bit ALU

As carrier density in PMOS is less compared to NMOS, the width of the PMOS transistors are chosen higher than NMOS so that the rising and falling time is balanced.

The PMOS and NMOS W/L chosen are:

PMOS: W=0.525; L=0.070
NMOS: W=0.140; L=0.070

B. IMPLEMENTATION OF ANCIENT MATHEMATICS

Simulation Result for 16 BIT ALU Description

A	Input data 4 bit
B	Input data 4 bit
Gclk	Global clock
Clk	clock frequency of multiplier
Clr	reset signal which forces output = 0
Clken	enable signal, must be 1 to produce output
Dataout	output 16 bit
S0	select line input from control unit
S1	select line input from control unit

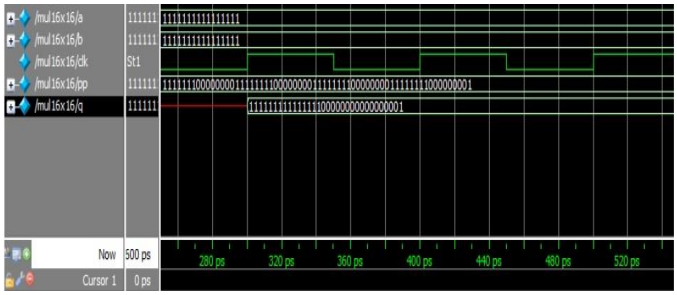


Figure 1.8 Simulation waveform for 16 bit ALU by ModelSim

V RESULT AND DISCUSSION

Simulation results of 64 bit ALU using D3L is tabulated below. The result below shows the critical path delay and the Power Delay product of the 64 bit ALU using D3L Logic proposed in this paper gives improved performance compared to logic gates and CMOS logic.

TABLE I. PERFORMANCE COMPARISON OF 4 BIT ALU

Parameters	**Difference Logic**		
	Logic Gates	***CMOS Logic***	***D3L Logic***
Power Dissipation	8.975nW	3.555nW	2.4250nW
Delay (ns)	2.840ns	2.750ns	1.826ns
Area (number of transistors)	592	232	180

B. POWER DISSIPATION

In CMOS technology, Power dissipation is the most critical parameter for portability & mobility and it is classified into dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue when the circuit is inactive or is in a power-down mode.

C. SPEED

Vedic multiplier is faster than Booth Multiplier and array multiplier. As the number of bits increase from 16 bits to 64 bits, the timing delay is greatly reduced for Vedic multiplier as compared to other types of multipliers. Vedic multiplier has the greatest advantage as compared to other type of multipliers over regularity of structures and gate delays. Delay in Vedic multiplier for 16 bits number is 32 ns while the delay in Booth and Array multiplier are 38ns and 44ns respectively. Thus this multiplier shows the highest speed among conventional multiplier. It has this advantage than others types to prefer a best multiplier.

D. AREA

The area needed for Vedic square multiplier is very small as compared to other multiplier architectures i.e the number of devices used in Vedic Square multiplier are 259 while Booth and Array Multiplier is 592 and 495 respectively for 16 bits number when implemented on Modelsim.

TABLE II. PERFORMANCE COMPARISON OF 64 BIT ALU

Parameters	**Difference Logic**		
	Logic Gates	***CMOS Logic***	***D3L Logic***
Power Dissipation	4.000nW	3.555nW	3.000nW
Delay (ns)	530.11ns	275.0ns	240.6ns
Area (number of transistors)	1024	854	728
Technology	45nm	45nm	45nm

VI CONCLUSION AND FUTURE WORK

In VLSI design process, area, power and delay are the important factors that determine the performance of any circuit. Logic gates and CMOS Logic has the disadvantages of using more power consumption and large area. The proposed design is designed to reduce the area, power and delay that occur in the existing design. The result obtained from the proposed ALU that is implemented using D3L Logic shows better performance in terms of area, power and delay. As a result of the proposed design, it requires very less number of gates. The area of the proposed design shows a decrease for 4, 16 and 64-bit sizes which indicates success of the method and not a mere tradeoff of delay for area and power consumption. In this paper we proposed a novel architecture for the 16x16 bit Multiplier and a 64 bit ALU which provides somewhat better results as compare to the available Vedic multiplier or all other Multiplier. Proposed design can also be used for optimizing performance of Speed, Power consumption and delay in ALU.

ACKNOWLEDGMENT

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