

# Design And Implementation of AES Algorithm with Biometric Key Schedule to Improve Security

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**Abstract**— Hardware Security plays a vital role in most of the applications such as net banking, e-commerce, etc. Cryptography is linked with the process of converting ordinary plain text into indistinct text and vice versa. Symmetric key algorithms i.e., Advanced Encryption Standard (AES), and Data Encryption Standard employs the same key for encryption and decryption. The proposed Bio-Metric 256-bit AES algorithm is highly utilized in terms of Key management for enhance the security. The enhancement has been done by selecting the various pixels from an image. This in turn results in a power reduction by a FPGA implementation. The entire process of the proposed implementation was done by using Virtex-7 FPGA. We used Xilinx software with the help of Verilog HDL .The expected output was collected and the simulation waveforms are verified.

**Keywords**—Advanced encryption ,Data encryption, FPGA, Verilog HDL, Bio metric image.

## I.INTRODUCTION

In these modern-days, block ciphers plays a major role in encryption technologies. Here ,the role of substitution-boxes is used to transform the normal text data to generate cipher-text data randomly with some appropriate disorder to confuse the attackers. We all know that the robustness and security of block ciphers will depends upon cryptographic strength of basic s-boxes .Because, these s-boxes are the most capable components which taken the responsible to fetch the randomness and to make the system complex to improve the security system that can confuse the attackers. Many concepts have been explored to build the strong s-boxes. In this paper, we have given a detailed knowledge of key generation with high security. This modular approach consists of three tasks i.e., modular inverses, new transformation and permutation. In this new approach ,we fixed the drawbacks in the existing system, such as non linearity and uniformity to demonstrate cryptographic potentiality. To this, an image encryption process is also implemented in the S-box to perform the shuffling of pixels, replace with strong statistical and differential encryption performance.

In today's technological life the data and information communication is considering as treasure to the individual or organization. If the privacy of the information is not secured, then the information will use for mischievous purposes. In

present era, the innovations in technology is increasing the size of data transmission through the internet. So, the private information have to be secure from the invaders. These methods will be more helpful to protect our data.

The cryptographic algorithms are one of the best method for protection of the data because it obtained from mathematical methods and set of calculations to convert messages to make hard to decode the original code. These methods helps to key generation and to secure the confidential data. Stream ciphers alters the data in a bit wise manner, the block ciphers converts the data into blocks which compress the large number of bits or bytes at the same time. These days ,block ciphers are considering as most effective tool for protection of data. protection. Advanced encryption, Data Encryption are the examples of block ciphers. The implementation of block ciphers are simple than stream ciphers. The SP network-based block ciphers are a type of block cipher that is commonly used. Thus, when utilizing block ciphers, the sender and receiver of the data encrypt and decrypt the data using the same key.

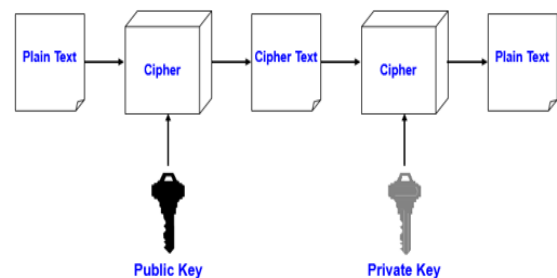


Fig. 1. Block diagram of an AES algorithm

A static s-box is used in each round of block cipher. It allows data analyses attack and eventually captures the sub keys using inverse sub byte. In this paper, we proposed a simple design and implement with low cost to existing AES to Dynamic s-box.. To make S-box as dynamic ,the current AES S-Box and new produced S-Boxes are employed to implement dynamic S-box.

The remaining part of this project work is mentioned as follows: The existing system are discussed and how to implement the key previously in section II.. In Section-III emphasizes the proposed implementation of key generation using bio-metrics. The section IV includes the suggested method synthesis results as well as other existing AES approaches and comparison between them. The suggested method is also included in the updated Modified key generation to complete AES metrics and

to validate the findings using post-synthesis simulated result. Additionally, the suggested design Synthesized on Various FPGA boards for various performance analyses. Section V&VI explains about the advantages and applications. Section VII brings the paper to a Conclusion

## II. EXISTING METHOD

So many technologies was implemented earlier to improve security , such as multi level AES transformation units are used for maximizing the confusion metrics during encryption process and the Combinational circuit is used for S-box implementation which will increase security. S-box is modified as one way mapping function. In this, the S box values are directly accessed from memory which leads more power consumption and path delay overhead and by using Cryptosystem-Key management is a major issues which will be the major cause in hacking. Although they created the key by adding 128 bits to 128 bits to make it as 256 bits which gives the high security ,the key leakage may happen sometimes at the time of decryption at receiver end. .By using this method the complexity is high and efficiency is also less. To overcome these drawbacks we implemented the proposed system.

## III. PROPOSED METHOD

The prime objective of this proposed method is to increase the efficiency and to reduce the complexity. We demonstrate how a key size used and number of rounds will increase the computation complexity. To maximize the security and increase the resistance level cipher key length is need to increase. And to narrow down the design complexity without compromising the security different transformations can be used. In this paper 256 key size is used for AES and also incorporate different combination of transformations for each round for low complexity with improved randomness over cipher text conversion method. To overcome the key management problem associated to AES core digital biometric based fully automated key generation scheme is introduced. This auto key generation follows hierarchical steps which includes different level of confusion metrics for AES.

In a single image, there will be a greater number of Pixels available. So, Possibility to find out the pixels what we are using as key is highly complex one. Even though if someone find out the pixels count as well as pixel's location, they need to know the arrangement of pixels. The KEY origination is kept as a secret. So to hack the data is very tough.

### A. Key generation by using the Biometric image

In this method first we have to convert the biometric image to digital image. i.e., made up of pixels. We can generate the key by using the following algorithm i. Selecting the location of the pixel. ii. By using random generator we have to concatenate the number and iii. We have to integrate the value. So, it randomly generates one key. By using the key we can encrypt the data. No one knows how the key was generated and they cannot know the arrangement of pixels. For decryption ,the encrypted data will transform back by giving cipher text with the help of the key we can get the plain text. It will use the same

cryptographic keys at both sender end and receiver end.By using this method there is no need to remember and store the key to encrypt the data. This method gives more security than the existing system. Randomly we can change the key according to our wish. So that, there is no possibility to hack the data ,this method gives more accuracy and less complexity.

### B. Cipher text

Cipher text is nothing but the information has to be hidden by giving some additional data to the original which cannot be read by human. The data is decrypted by using the key. There are two ways to implement the cipher text i.e, Stream Ciphers and Block ciphers. In stream ciphers the text is encrypted by using bit by bit or byte by byte. By using the block ciphers it encrypts by using blocks. Each block is operated independently. In cryptography the cipher text plays an important role to protect our data from the invaders.



Fig 3a. Biometric image

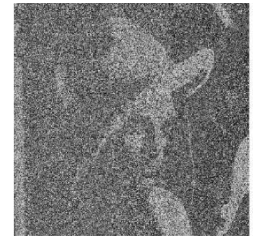


Fig 3b. Encrypted image

### C .Random generator

The random generator will generates the random number with the help of AES algorithm .This AES algorithm deals with four operations .i.e., Sub Bytes, Add Round Key , Mix column, Shift Rows..256-bit AES encryption block is implemented in 14 rounds. For each round it will do the four operations .Round 0 consists of only Add round Key operation. Round 14 consists of Sub Bytes, Shift Rows and Add Round Key operations, which need 3 clock cycles. Rounds 1 to 13 consists of all the four operations. We do a distinct operation in each clock cycle. Hence once the hardware has been implemented for all four operations we can use the same hardware for all the 14 rounds. None of the four operations shares the same clock cycle. The sequence of round operation with specific sequence of 4 operations to complete the AES encryption. The AES method is a serial process. i.e., the first round output is connected to the second round and it will be the input for it. Hence, we can use the same hardware for each round. The data structure of 128-bit matrix. Each column consists of 4 elements of 8 bits each, so in total we have 32 bits per word.

Round 0	01 cycle
Round 1 to 13	52 cycles
Round 14	03 cycles
Total	56 cycles

Fig.4 Cycles required in Each Round

We are using 14 rounds for both encryption and decryption. The cipher text after encryption will be transmitted across the channel. At the receiver end ,we will use the same key which used before in the encryption. Data

include message to be encrypted, cipher text and the decrypted message.

S box	Shift	Mix	Cycle
Sub_0	-	Mix_0	1
Sub_1	Shift_0	Mix_1	2
Sub_2	Shift_1	Mix_2	3
Sub_3	Shift_2	Mix_3	4
Sub_0	Shift_3	Mix_0	5
Sub_1	Shift_0	Mix_1	6
Sub_2	Shift_1	Mix_2	7
Sub_3	Shift_2	Mix_3	8
Sub_0	Shift_3	Mix_0	9
Sub_1	Shift_0	Mix_1	10
Sub_2	Shift_1	Mix_2	11
Sub_3	Shift_2	Mix_3	12
Sub_0	Shift_3	Mix_0	13
Sub_1	Shift_0	Mix_1	14
Sub_2	Shift_1	Mix_2	15
Sub_3	Shift_2	Mix_3	16
Sub_0	Shift_3	Mix_0	17
Sub_1	Shift_0	Mix_1	18
Sub_2	Shift_1	Mix_2	19
Sub_3	Shift_2	Mix_3	20
Sub_0	Shift_3	Mix_0	21
Sub_1	Shift_0	Mix_1	22
Sub_2	Shift_1	Mix_2	23
Sub_3	Shift_2	Mix_3	24
Sub_0	Shift_3	Mix_0	25
Sub_1	Shift_0	Mix_1	26
Sub_2	Shift_1	Mix_2	27
Sub_3	Shift_2	Mix_3	28
Sub_0	Shift_3	Mix_0	29
Sub_1	Shift_0	Mix_1	30
Sub_2	Shift_1	Mix_2	31
Sub_3	Shift_2	Mix_3	32
Sub_0	Shift_3	Mix_0	33
Sub_1	Shift_0	Mix_1	34
Sub_2	Shift_1	Mix_2	35
Sub_3	Shift_2	Mix_3	36
Sub_0	Shift_3	Mix_0	37
Sub_1	Shift_0	Mix_1	38
Sub_2	Shift_1	Mix_2	39
Sub_3	Shift_2	Mix_3	40
Sub_0	Shift_3	Mix_0	41
Sub_1	Shift_0	Mix_1	42
Sub_2	Shift_1	Mix_2	43
Sub_3	Shift_2	Mix_3	44
Sub_0	Shift_3	Mix_0	45
Sub_1	Shift_0	Mix_1	46
Sub_2	Shift_1	Mix_2	47
Sub_3	Shift_2	Mix_3	48
Sub_0	Shift_3	Mix_0	49
Sub_1	Shift_0	Mix_1	50
Sub_2	Shift_1	Mix_2	51
Sub_3	Shift_2	Mix_3	52
Sub_0	Shift_3	Mix_0	53
Sub_1	Shift_0	Mix_1	54
Sub_2	Shift_1	Mix_2	55
Sub_3	Shift_2	Mix_3	56
Sub_0	Shift_3	Mix_0	57
Sub_1	Shift_0	Mix_1	58
Sub_2	Shift_1	Mix_2	59
Sub_3	Shift_2	Mix_3	60
Sub_0	Shift_3	Mix_0	61
Sub_1	Shift_0	Mix_1	62
Sub_2	Shift_1	Mix_2	63
Sub_3	Shift_2	Mix_3	64
Sub_0	Shift_3	Mix_0	65
Sub_1	Shift_0	Mix_1	66
Sub_2	Shift_1	Mix_2	67
Sub_3	Shift_2	Mix_3	68
Sub_0	Shift_3	Mix_0	69
Sub_1	Shift_0	Mix_1	70
Sub_2	Shift_1	Mix_2	71
Sub_3	Shift_2	Mix_3	72
Sub_0	Shift_3	Mix_0	73
Sub_1	Shift_0	Mix_1	74
Sub_2	Shift_1	Mix_2	75
Sub_3	Shift_2	Mix_3	76
Sub_0	Shift_3	Mix_0	77
Sub_1	Shift_0	Mix_1	78
Sub_2	Shift_1	Mix_2	79
Sub_3	Shift_2	Mix_3	80
Sub_0	Shift_3	Mix_0	81
Sub_1	Shift_0	Mix_1	82
Sub_2	Shift_1	Mix_2	83
Sub_3	Shift_2	Mix_3	84
Sub_0	Shift_3	Mix_0	85
Sub_1	Shift_0	Mix_1	86
Sub_2	Shift_1	Mix_2	87
Sub_3	Shift_2	Mix_3	88
Sub_0	Shift_3	Mix_0	89
Sub_1	Shift_0	Mix_1	90
Sub_2	Shift_1	Mix_2	91
Sub_3	Shift_2	Mix_3	92
Sub_0	Shift_3	Mix_0	93
Sub_1	Shift_0	Mix_1	94
Sub_2	Shift_1	Mix_2	95
Sub_3	Shift_2	Mix_3	96
Sub_0	Shift_3	Mix_0	97
Sub_1	Shift_0	Mix_1	98
Sub_2	Shift_1	Mix_2	99
Sub_3	Shift_2	Mix_3	100

Fig 5.Operation of Mix block

S box	Shift	Mix	Cycle
Sub_0	-	Mix_0	1
Sub_1	Shift_0	Mix_1	2
Sub_2	Shift_1	Mix_2	3
Sub_3	Shift_2	Mix_3	4
Sub_0	Shift_3	Mix_0	5
Sub_1	Shift_0	Mix_1	6
Sub_2	Shift_1	Mix_2	7
Sub_3	Shift_2	Mix_3	8
Sub_0	Shift_3	Mix_0	9
Sub_1	Shift_0	Mix_1	10
Sub_2	Shift_1	Mix_2	11
Sub_3	Shift_2	Mix_3	12
Sub_0	Shift_3	Mix_0	13
Sub_1	Shift_0	Mix_1	14
Sub_2	Shift_1	Mix_2	15
Sub_3	Shift_2	Mix_3	16
Sub_0	Shift_3	Mix_0	17
Sub_1	Shift_0	Mix_1	18
Sub_2	Shift_1	Mix_2	19
Sub_3	Shift_2	Mix_3	20
Sub_0	Shift_3	Mix_0	21
Sub_1	Shift_0	Mix_1	22
Sub_2	Shift_1	Mix_2	23
Sub_3	Shift_2	Mix_3	24
Sub_0	Shift_3	Mix_0	25
Sub_1	Shift_0	Mix_1	26
Sub_2	Shift_1	Mix_2	27
Sub_3	Shift_2	Mix_3	28
Sub_0	Shift_3	Mix_0	29
Sub_1	Shift_0	Mix_1	30
Sub_2	Shift_1	Mix_2	31
Sub_3	Shift_2	Mix_3	32
Sub_0	Shift_3	Mix_0	33
Sub_1	Shift_0	Mix_1	34
Sub_2	Shift_1	Mix_2	35
Sub_3	Shift_2	Mix_3	36
Sub_0	Shift_3	Mix_0	37
Sub_1	Shift_0	Mix_1	38
Sub_2	Shift_1	Mix_2	39
Sub_3	Shift_2	Mix_3	40
Sub_0	Shift_3	Mix_0	41
Sub_1	Shift_0	Mix_1	42
Sub_2	Shift_1	Mix_2	43
Sub_3	Shift_2	Mix_3	44
Sub_0	Shift_3	Mix_0	45
Sub_1	Shift_0	Mix_1	46
Sub_2	Shift_1	Mix_2	47
Sub_3	Shift_2	Mix_3	48
Sub_0	Shift_3	Mix_0	49
Sub_1	Shift_0	Mix_1	50
Sub_2	Shift_1	Mix_2	51
Sub_3	Shift_2	Mix_3	52
Sub_0	Shift_3	Mix_0	53
Sub_1	Shift_0	Mix_1	54
Sub_2	Shift_1	Mix_2	55
Sub_3	Shift_2	Mix_3	56
Sub_0	Shift_3	Mix_0	57
Sub_1	Shift_0	Mix_1	58
Sub_2	Shift_1	Mix_2	59
Sub_3	Shift_2	Mix_3	60
Sub_0	Shift_3	Mix_0	61
Sub_1	Shift_0	Mix_1	62
Sub_2	Shift_1	Mix_2	63
Sub_3	Shift_2	Mix_3	64
Sub_0	Shift_3	Mix_0	65
Sub_1	Shift_0	Mix_1	66
Sub_2	Shift_1	Mix_2	67
Sub_3	Shift_2	Mix_3	68
Sub_0	Shift_3	Mix_0	69
Sub_1	Shift_0	Mix_1	70
Sub_2	Shift_1	Mix_2	71
Sub_3	Shift_2	Mix_3	72
Sub_0	Shift_3	Mix_0	73
Sub_1	Shift_0	Mix_1	74
Sub_2	Shift_1	Mix_2	75
Sub_3	Shift_2	Mix_3	76
Sub_0	Shift_3	Mix_0	77
Sub_1	Shift_0	Mix_1	78
Sub_2	Shift_1	Mix_2	79
Sub_3	Shift_2	Mix_3	80
Sub_0	Shift_3	Mix_0	81
Sub_1	Shift_0	Mix_1	82
Sub_2	Shift_1	Mix_2	83
Sub_3	Shift_2	Mix_3	84
Sub_0	Shift_3	Mix_0	85
Sub_1	Shift_0	Mix_1	86
Sub_2	Shift_1	Mix_2	87
Sub_3	Shift_2	Mix_3	88
Sub_0	Shift_3	Mix_0	89
Sub_1	Shift_0	Mix_1	90
Sub_2	Shift_1	Mix_2	91
Sub_3	Shift_2	Mix_3	92
Sub_0	Shift_3	Mix_0	93
Sub_1	Shift_0	Mix_1	94
Sub_2	Shift_1	Mix_2	95
Sub_3	Shift_2	Mix_3	96
Sub_0	Shift_3	Mix_0	97
Sub_1	Shift_0	Mix_1	98
Sub_2	Shift_1	Mix_2	99
Sub_3	Shift_2	Mix_3	100

Fig 6. Generation of key by using random generator

By using this random generator some values will produce randomly that will concatenate to the pixel location and then it will forms the key. The whole process is done in the process of pipelined structured method. It will gives more accuracy to generate the key.

#### D. PIPELINED STRUCTURED METHOD

In this project we used pipelining method .Pipelining is nothing but processing the data as input in continuous method without waiting for the current process to complete. In many processors pipelining concept was used in many ways. Here we are using registers to store the current output . So, instead of immediately transmitting each round's output to the next round, we now utilise a register that acts as a internal register.. Since the current rounds' value is stored in the register the next input to the current round can be given as the current output is obtained.

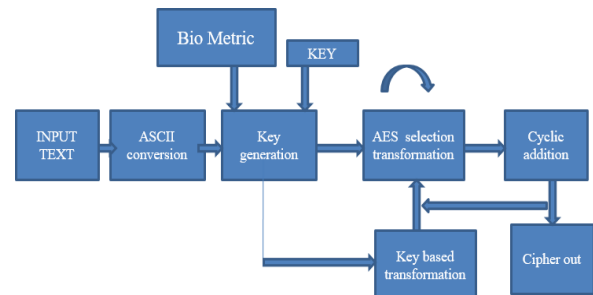


Fig 7. Pipelined structured method

The following diagram explains that the biometric image converts to the hexadecimal values that will take as the input and it will transforms to the ASCII conversion ,by using ASCII conversion the key will become more secure. In the next step the cipher text will be added by using AES algorithm method which gives the high security to the key and then the key will generates. By the help of key we can encrypt our data in secure manner.

#### E. VERILOG HDL

Today Verilog is the best language in the digital systems. Because it simplifies the process and the language is also easily understandable .Most of the designers are choosing the Verilog HDL as it permits to designs in the top-down or bottom-up methods. With the help of this we can perform the large circuits as it gives the RTL schematic along with the technology schematic methods. So that we can easily understand our circuits how we are designing. It creates the levels of abstraction which will hide the details of implementation and the technology. So many languages were introduced before such as system Verilog and VHDL .But these languages are complex when compare to Verilog. That's why most of the designers will choose the Verilog language .The syntax of Verilog is also simple and it is similar to C language so that it will easily understandable. Verilog is case sensitive and all the keywords are in the lower case. It has a facility to mix up the level of abstractions freely. For using Verilog, Xilinx is the good software to design the large circuits easily .It supports to design and to evaluate with boards such as FPGA , Microprocessor etc., It is flexible to adapt the new technologies.

#### F. MATLAB

For converting the image to digital format ,MATLAB is the best tool .As the name indicates it is nothing but Matrix laboratory which deals with matrixes. As it is well integrated it is easily understandable and also easy to perform the tasks. Most of the designers will choose this MATLAB because it performs image to data conversion easily and also easily understandable. For digital image processing matlab is very helpful as it provides the signal processing in easy way and also to analyze the data. Another reason to choose matlab is it controls the devices as well as the systems and also it provides the workflow by giving commands. It will also used for wireless communications, which will helps to eliminate the designing problems. In this project we used MATLAB.



#### IV. RESULTS AND DISCUSSION

The proposed AES algorithm and existing AES algorithm both are functionally verified by using Xilinx 14.7 version. The proposed design has better area when compared to existing design without degrading the other factors. In the proposed method while we are using dynamic key it will decrease the area, improve the performance of the architecture.

##### RTL Schematic:

The below fig 8. Depicts the RTL schematic of the proposed architecture that is synthesized in Xilinx ISE 14.7 version tool. It shows the internal components that exists in the structure.

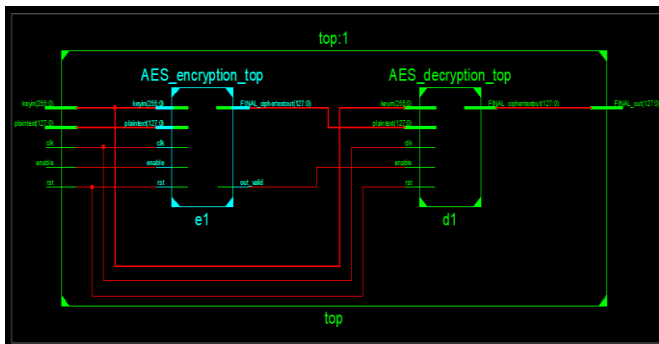


Fig 8.RTL Schematic diagram

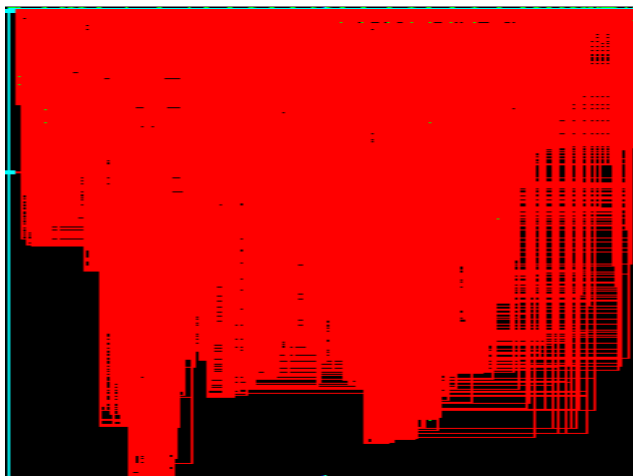


Fig 9. Technology Schematic diagram

**Simulation Results:** Output waveformsThe below figures are the simulation results of proposed structure which is implemented.

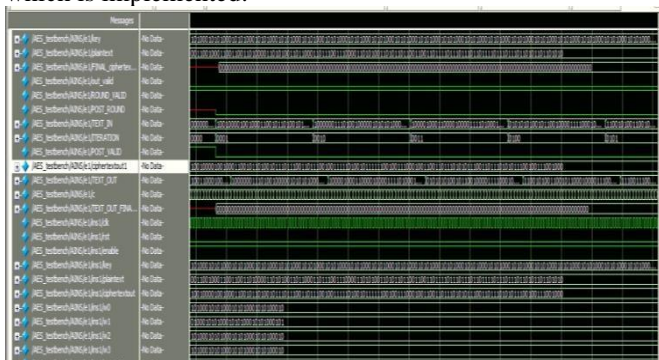


Fig.10.a. Input text in &out without ASCII

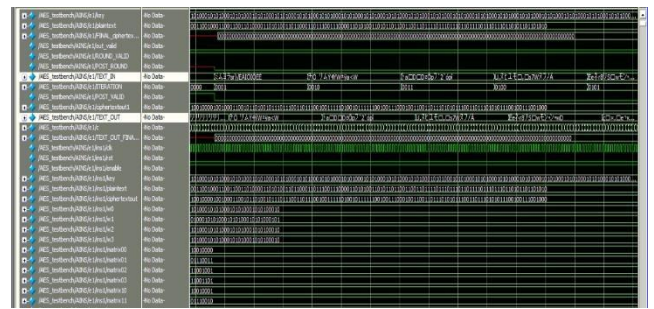


Fig 10 b. Input text in &out with ASCII

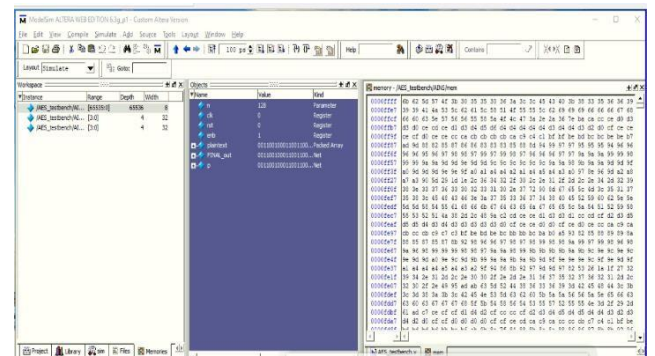


Fig 10c Combination of numbers by converting into pixels

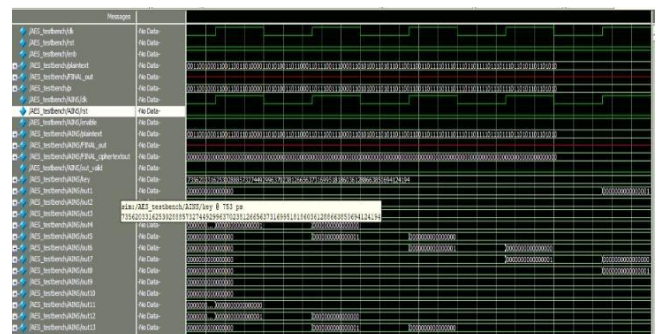


Fig 10 d. Generation of Key

In fig 10 a. the input text data is in the form of numerical values after adding the ASCII values to the input text we can get the different values with the help of the random generator i.e.,in Fig 10b.In Fig 10c,it is the hexadecimal values after we convert the biometric image to pixels .When we select one random number in pixels and it will concatenate with the ASCII value then it will generates the key which will be highly confidential ,the waveform in the Fig 10d. By using this key the data will encrypt as secure as possible.

**Evaluation of Area, Delay report:**

	Area	Delay
Existing	5706	33.346ns
Proposed	5279	13.377ns

Table1.Accuracy of existing & proposed methods.

The above Table 1 shows the comparison between existing and proposed structures of AES implementation

## V. ADVANTAGES

- a. The complexity of the system is low .
- b. Outer level security is high.
- c. Data rate in very high
- d. It is able to process high level cipher in any real time data.
- e. It has less area.

## VI. APPLICATIONS

- a. It can be used in Wireless Security
- b. It can be used Processor security
- c. It can be used for File encryption

## VII. CONCLUSION

This paper presents a generalized design and a practical implementation of AES algorithm with key extracted from biometric. Instead of using static key, the proposed method had better performance in terms of security. The proposed AES and existing AES algorithm both are functionally verified by using Xilinx 14.7 version. The above results shows that the proposed design consists of less area and less delay when compare to the existing design. By using the proposed system the data will be more confidential.

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