

Design and Implementation of 4x4 Vedic Multiplier using Cadence

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Abstract - Multipliers play an important role in today's digital signal processing and various other applications. Multiplier acts as a key block element in high speed arithmetic logic units, microcomputer, image processing etc. Multiplication process basically requires more hardware resources and computation time than addition and subtraction process. In the recent years growth of the portable electronic is forcing the designers to optimize the existing design for better performance. Vedic mathematics have sixteen sutras but "Urdhva-Triyagbhyam" is mainly used. Vedic method for multiplication which is different from the process of normal multiplication is presented. This paper proposes the design of Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. Urdhva-Triyagbhyam is the most efficient algorithm that gives minimum delay for multiplication for all types of numbers irrespective of their size. To enhance speed numerous modifications over the standard modified booth algorithm, Wallace tree methods for multiplier design have been made and several new techniques being worked upon. Amongst these Vedic multipliers based on Vedic mathematics are currently under focus.

Key Words: Vedic Multiplier, Urdhva-Triyagbhyam, arithmetic logic units, Power Consumption, Delay, speed.

1. INTRODUCTION

Algorithms like Array multiplier, Booth multiplier, Bit serial multiplier, Carry save multiplier, Modified booth multiplier and Wallace multiplier can perform multiplication. In Array multiplier, combinational logic is used for multiplication of two binary numbers. This multiplier performs product of all bits at once due to which it is faster multiplier but it requires large number of gate which makes it not economical. In Carry save adder bits are processed one by one to add carry in adder. So it depends upon previous carry which increases its execution time as number of bits increases. In Wallace tree, three bit signals are passed to one bit full adder as input. Output of these inputs, sum is passed to the next state full adder which is at higher position. Because of high speed of operation layout of the Wallace tree multiplier is not possible. To overcome the drawback of these multipliers, Vedic Multiplier is proposed.[2,6] As the common digital signal processing algorithms spend most of their time multiplying, the processors spend a lot of chip area in order to make the multiplication as fast as possible. Hence a non-conventional yet very efficient Vedic mathematics is used for making a high performance multiplier. Vedic Mathematics deals mainly with various Vedic mathematical formulae and their applications for carrying out large arithmetical operations easily.

1.1 Objective

The objective of this project is to

- Reduce the number of steps in multiplication process.
- Reduce the computational delay.
- Enhance the speed of addition by using MUX based adder.
- Reduce power consumption.
- Reduce memory utilization.

2. LITERATURE SURVEY

Y.Rama Lakshmana, G.Challa Ram, "Area efficient modified Vedic multiplier" The paper describes the design of high speed Vedic multiplier that uses BEC(binary to excess converter) to add the partial products. The main advantage of BEC adder is, uses it uses less number of logic gates than the N-bit ripple carry adder which in turn reduces the power consumption and time delay. There is a comparison between array multiplier and Vedic multiplier. Implementation is done in Xilinx 12.2 on Spartan6 3E kit.

Saji.M.Antony, Dr.Rajeshwari Pandey, "To Design High Speed Vedic Multiplier" This paper describes the comparison of Vedic Multiplier with other conventional multipliers. The proposed design gives much less delay. Implementation is done in Xilinx ISE 14.7.

M.A.Sayyad, D.N.Kyatanavar, "Optimization for Addition Partial Products in Vedic Multiplier" In this paper they have designed Vedic Multiplier by using different adders like ripple carry adder and carry look ahead adder and compared it with array multiplier. Power Dissipation has been reduced. Implementation is done in Xilinx ISE 13.1.

Kush Kumar, Vishesh Tyagi, "A State-of-the-Art Study on multipliers: Advancement and Comparison" In this journal there is a comparison between various multipliers like array multiplier, booth multiplier, Vedic Multiplier. Considering the parameters like speed, area, power consumption they have shown that Vedic Multiplier.

3 VEDIC MULTIPLIER

The proposed Vedic Multiplier is based on the Vedic Multiplier formulae (sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. Apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on some algorithm, is discussed below:

3.1 Urdhva Tiryabhyam sutra

The multiplier is based on an algorithm Urdhva Triyakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Triyakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done and then, concurrent addition of these partial products can be done. Thus parallelism in generation of partial products and their summation is obtained using Urdhva Triyakbhyam. The algorithm can be generalized for $n \times n$ bi number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures.

3.2 Vertically and crosswise technique

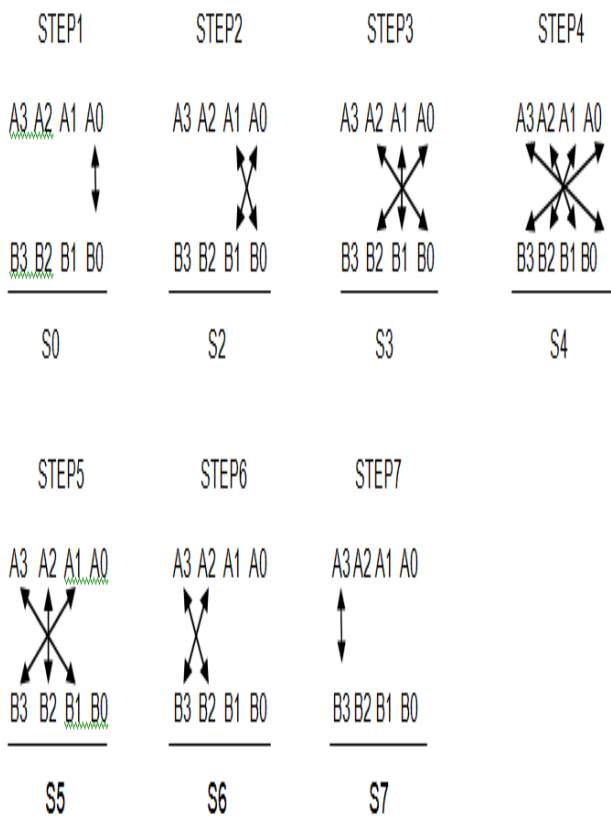


Figure 3.1: Vertically and Crosswise Technique

- Step1: $S_0 = A_0 * B_0$
- Step2: $S_1 = A_1 * B_0 + A_0 * B_1$
- Step3: $S_2 = A_2 * B_0 + A_0 * B_2 + A_1 * B_1$
- Step4: $S_3 = A_3 * B_0 + A_0 * B_3 + A_2 * B_1 + A_1 * B_2$
- Step5: $S_4 = A_3 * B_1 + A_1 * B_3 + A_2 * B_2$
- Step6: $S_5 = A_3 * B_2 + A_2 * B_3$
- Step7: $S_6 = A_3 * B_3$

Finally the output is: $S_0S_1S_2S_3S_4S_5S_6$

As the number of steps are reduced in UT algorithm compared to Array Multiplier, this technique will be more efficient for designing a Multiplier.

Now we will see how this algorithm can be used for binary numbers. For example,

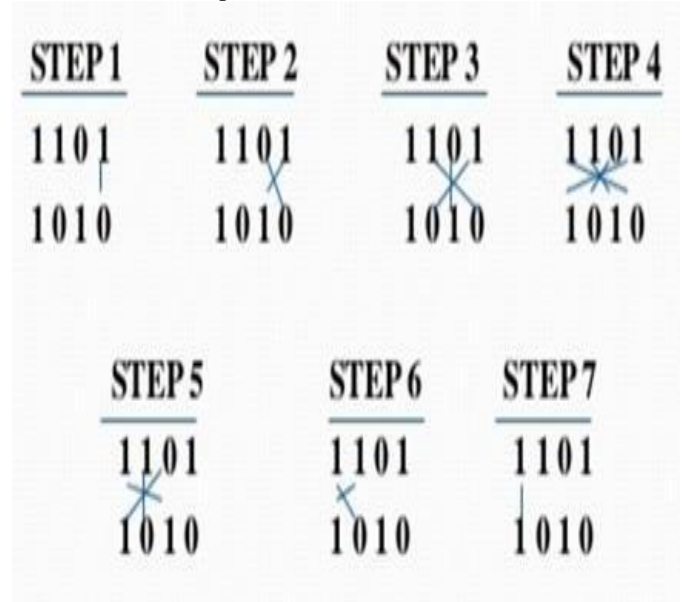


Figure 3.2: Using Urdhva Tiryakbhyam for Binary numbers

3.3 4 x 4 Vedic Multiplier

Here, rather than following sequential expansion, the expansion tree has been changed to Wallace tree resemble the other the same, along these lines diminishing the degrees of expansion to 2, rather than 3. Here, two lower bits of q_0 pass legitimately to yield, while the upper bits of q_0 are taken care of into expansion tree. The bits being fed to addition tree can be further illustrated by the diagram in fig3.3.

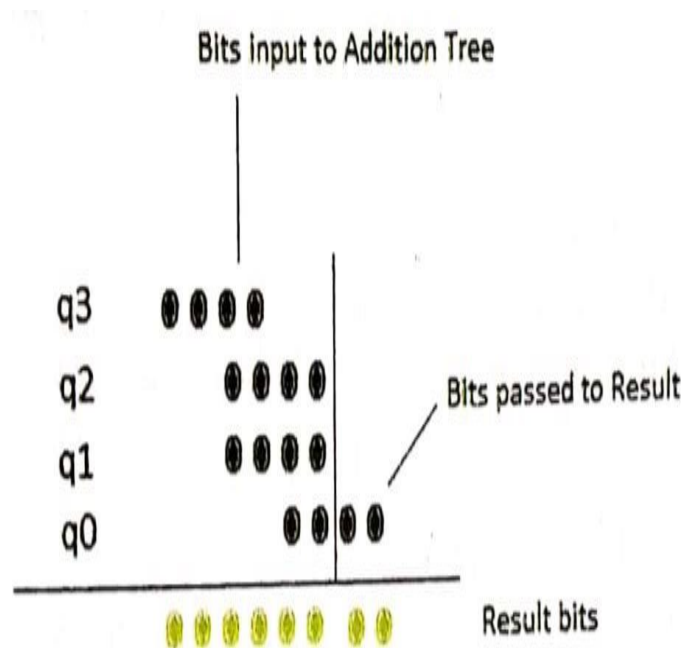


Fig. 3.3: 4x4 block partial products addition process.

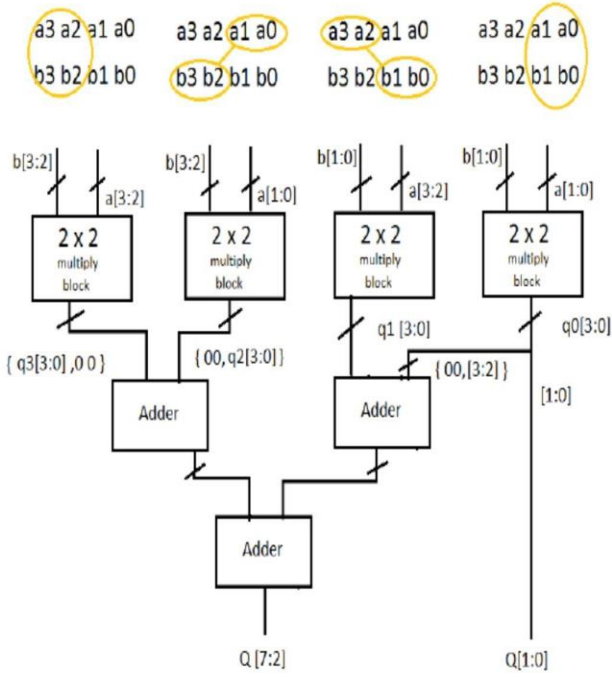


Fig 3.4: 4x4 Vedic Multiplier

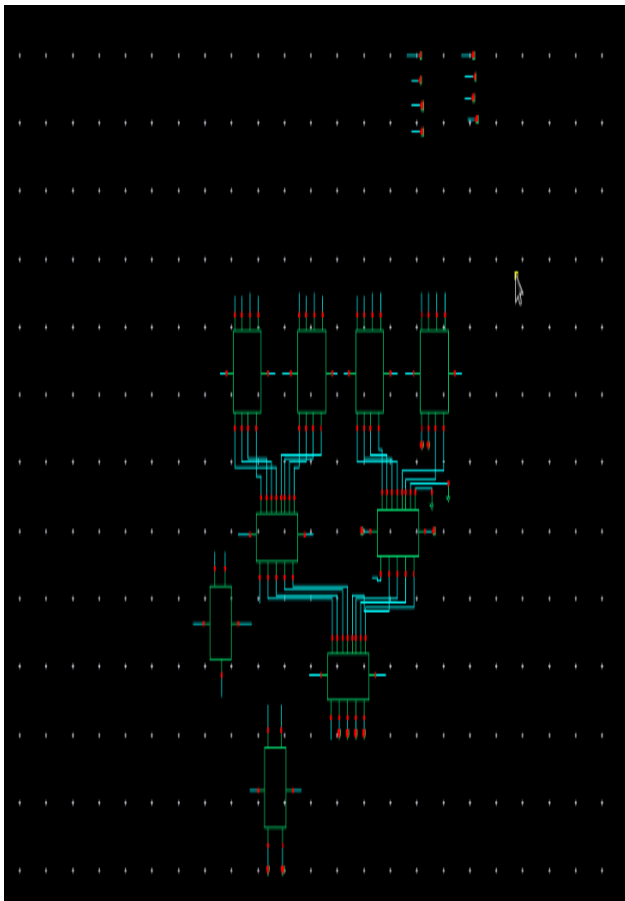


Fig.3.5. Schematic of 4x4 Vedic Multiplier

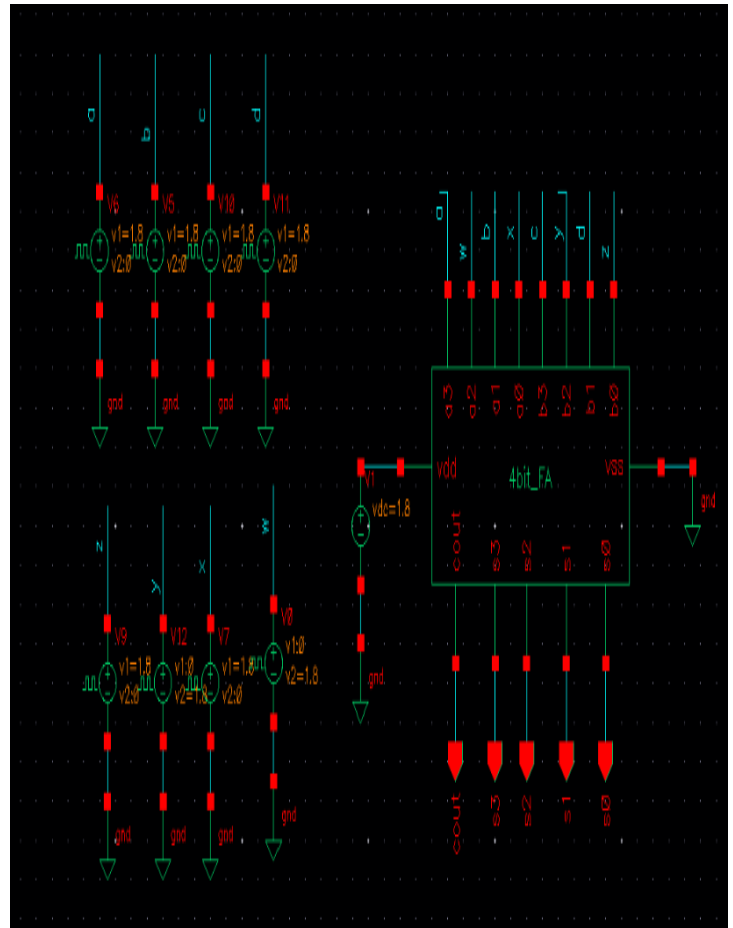


Fig.3.6 Waveforms of 4x4 Vedic Multiplier Setup.

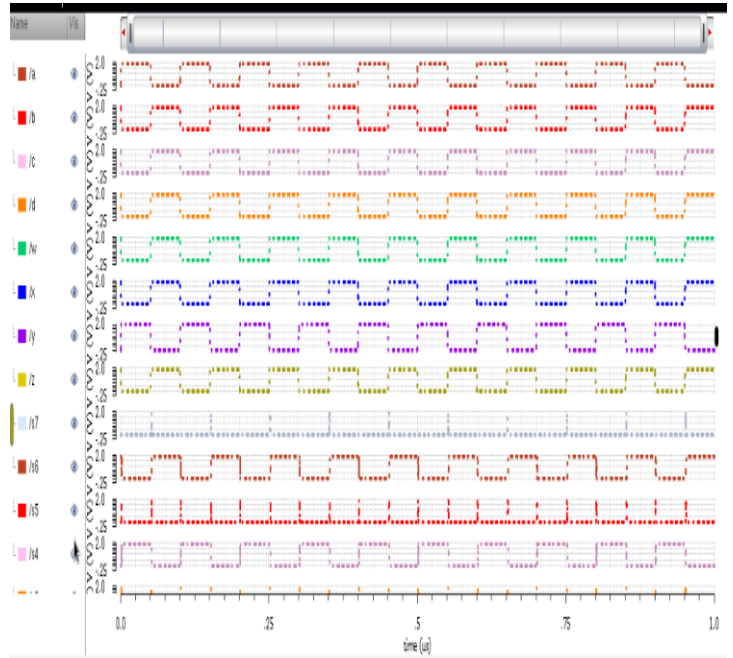


Fig.3.7 Output waveforms of 4x4 Vedic Multiplier.

4. CONCLUSIONS

4x4 Vedic Multiplier is implemented using modified full adder. Multiplexer is used in modified full adder for efficient addition. As the number of steps in multiplication is reduced, delay is reduced and hence speed of the multiplier increases. Vedic Algorithm like Urdhav Tiryagbhyam is best suited for high speed application and where area is a major constraint. MUX based adder is best suited for less power consumption applications.

DSP application modules like MAC require multipliers which can work on real time data at high clock rates which can be achieved with Vedic Multipliers. Ease of implementation of the design shows that complex modules for DSP and image processing can be simplified using Vedic algorithm.

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BIOGRAPHIES



Dr. Savita Sonoli completed B.E (E&CE), from BVBCET, Hubli, M.Tech (IE) from NITK, Surathkal, and Ph.D (Embedded Systems) from SK University, Ananthpur. She has 24 years of teaching experience, 18 years of research and 19 years of administration. At Present, working as Vice Principal & Head, E&CE Dept., RYMEC, Ballari. Worked as VTU BOE and LIC member. BOS member of E&CE Dept., SVCE, Bangalore, and as a Guest faculty. Member for professional bodies, IEEE, ISTE, IEI, ISOI, IAENG, ISCA, ISRASE & IEAE. Organized and attended many Workshops, FDPs and STTPs. Guided 12 M.Tech students, currently guiding 5 research scholars under VTU and one scholar is awarded with Ph.D under VTU. Published 42 Technical papers in National \ International journals \ Conference having good impact factor and indexed in Scopus and Google scholar and received awards for best paper. Reviewer for National / International journals and worked as a chair person for conferences. Received funds from VTU, KSTA, KSCST for projects and for organizing national level workshops and symposium. Received award for Best Projects guided. Major ongoing project funded is VGST, GOK for 20 Lacs. Visited Michigan & Wisconsin states of USA as GSE team member and Alumni meet at Dallas, USA.



Sahana Desai, completed BE(ECE) in Ballari Institute of Technology and Management. I am currently pursuing M tech in Digital communication and Networking at RYMEC, Bellary. Interested in communication domain and have done projects regarding home automation using microcontrollers and also in VLSI.