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Design and Implementation of 4-Bit ALU for Low-Power using Adiabatic Logic based on FINFET

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Abstract **- With the aggressive scaling of device technology, the leakage power has become the main part of power consumption, which seriously reduces the energy recovery efficiency of adiabatic logic. In this paper, a novel low-power adiabatic logic based on FinFET devices has been proposed.ALU is the core of all microprocessors. Now a days ALU is getting more complex and smaller in size to make the development of smaller and most powerful computer systems. An ALU which acts as core part of CPU is a combinational digital electronic. The design of 4-bit ALU, performs three arithmetic and four logical operations. The four arithmetic operations include ADD,SUBTRACT and COMPARE. The four logical operations such as AND, OR, XOR and NOT. For validating the proposed idea we have also designed power gated adiabatic inverter circuits using techniques like ECRL. In the implementation of adiabatic logic FinFET based ALU , it is possible to operate at lower operating voltages because FinFET has lower threshold voltages, power consumption is expected to be reduced and speed performance is expected to be improved.**

Keywords-FinFET,4-Bit ALU, Adiabatic Logic, ECRL

I. INTRODUCTION

The integrated chip technology has revolutionized the world of electronics in which MOS transistors have played a vital role in enhancing performance of integrated devices. In order to achieve high density and performance, MOS devices are continuously being scaled from last two decades[11].We have multi-gate field-effect transistors (FETs) such as planar double-gate FETs and FinFETs as a possible scaling path for low power digital CMOS technologies. The difficulties in shrinking the size of traditional bulk transistor give rise to the development of a new device architecture in which two gates, one on each side of the body, are used per device. Although early doublegate faced manufacturing challenges associated with vertical structure more recently, double-gate devices called FinFET or wrap around FETs that are compatible with standard CMOS. FinFET offers distinct advantages for scaling to very short gate lengths. Fabrication of FinFET is similar to that of conventional MOSFETs and holds a greater similarities with SOI devices. These devices could be more beneficial than three terminal devices since the threshold voltages can be adjusted by biasing the back gate terminal which tends to reduce sub-threshold leakage current and improve the slope factor.

There are limits to the scalability of the individual devices and as process technologies continued to shrink towards 20 nm, it became impossible to achieve the proper scaling of various device parameters. Those like the power supply voltage, which is the dominant factor in determining dynamic power were particularly affected. It was found that optimising for one variable such as performance resulted in unwanted compromises in other areas like power. It was therefore necessary to look at other more revolutionary options like a change in transistor structure from the traditional planar transistor[8].

One of the key issues is that as technologies use smaller feature sizes, the source and the drain of the MOS devices used encroach into the channel, making it easier for leakage current to flow between them and also making it very difficult to turn the transistor off completely.

Scaling of conventional CMOS devices below will create short channel effects like Vt roll-off and drain induced barrier lowering. The other issues are increasing leakage current, sub threshold leakage gate direct tunneling leakage and hot carrier effects. The gate leakage causes increased power consumption. For example, for inverter the power consumption is directly proportional to gate switching frequency, total load capacitance and fraction of gate switching. The leakage current is dependent on substrate and oxide current leakage. The problem of dynamic power is reduced using FinFET device since the charging and discharging of CL takes place with higher magnitude when compared to CMOS as the leakage current is suppressed. To overcome these issues a new device methodology for the processing element design is proposed using FinFET technology. The advantage of FinFET technology are higher drain current and switching speed, less than half the dynamic power requirement less static leakage current.

The static CMOS logic is the previously known popular robust one, but it has a major debit of leakage current and slow performance. Here, dynamic logic style is the high-performance circuit with low power dissipation, but that compromises with its robustness. In subthreshold logic, circuit works with a supply VDD which is lesser than threshold of transistor. In saturation region, CMOS logic consumes more power as compared to same logic operating in subthreshold region. n order to cut down dynamic power expenditure, the adiabatic logic can be used which has strong inversion without affecting noise immunity.

This paper is organized as follows. The literature survey that discusses on the ALU Design and FINFET technology carried our previously are presented in Section II. The working

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principle, applications and advantages of FinFET Technology are discussed in Section III. The proposed methodology of the 4-bit ALU Design is presented in Section IV and the schematic and simulation results of the arithmetic and logical operations of the ALU are discussed in Section V. Finally, conclusions are drawn in section VI.

II. LITERATURE SURVEY

Nirmal et aI.[1] proposed Double gate transistors (FinFETs) are the substitutes for bulk CMOS evolving from a single gate devices into three dimensional devices with multiple gates (double gate, triple gate or quadruple-gate devices). The main drawback of using CMOS transistors are high power consumption and high leakage current. Enormous progress has been made to scale transistors to even smaller dimensions to obtain fast switching transistors, as well as to reduce the power consumption. Even though the device characteristics are improved, high active leakage remain a problem. Leakage is found to contribute more amount of total power consumption in power- optimized FinFET logic circuits. This paper mainly deals with the various logic design styles to obtain the Leakage power savings through the judicious use of FinFET logic styles. They have demonstrated that the rich diversity of design styles, made possible by independent control of FinFET gates, can be used effectively to reduce total active power consumption in digital circuits.

Utkarsh Tripathi et al. [2] designed an adder circuit in which full adder CMOS is included, are designed using MOSFET in 32nm Technology length and in FinFET Technology with 28 transistors in MOSFET and FINFET. Then, they are simulated using HSPICE and the performance parameters of adder such as average power and delay are determined in both FinFET and MOSFET counterpart. It is observed that FINFET gives best results in the form of Average Power consumption and delay. DGFETs have emerged as a possible solution to continue technology scaling. Among DGFETs, FinFET have emerged as the most viable solution due to their ease of fabrication.

Scaling of the standard single-gate bulk MOSFETs faces great challenges in the nanometer regime due to the severe short-channel effects that cause an exponential increase in the leakage current and enhanced sensitivity to process variations. Multi-gate MOSFET technologies mitigate these limitations by providing a stronger control over a thin silicon body with multiple electrically coupled gates. Double-gate FinFET is the most attractive choice among the multi-gate transistor architectures because of the self-alignment of the two gates and the similarity of the fabrication steps to the existing standard CMOS technology. New latches and flip-flops based on independent-gate FinFETs are proposed in this paper S.A.Tawfik et al.[3] to simultaneously reduce the power consumption and the circuit area. With the proposed independently biased double-gate FinFET sequential circuits, the active power consumption, the clock power, the leakage power, and the circuit area are reduced by up to 47%, 32%, 42%, and 20%, respectively, while maintaining similar speed and data stability as compared to the standard sequential circuits with tied-gate FinFETs in a 32-nmFinFET technology.

Independent control of front and back gate in double gate (DG) devices can be used to merge parallel transistors in noncritical paths. This reduces the effective switching capacitance and, hence, the dynamic power dissipation of a circuit. However, efficient design of large-scale circuits with DG devices is not well explored due to lack of proper modeling and large-scale design simulation tools. A Datta et al.[4] they proposed several low-power circuit options using independent gate FinFETs. They developed semi analytical models for different FinFET logic gates to predict their performance. An efficient circuit synthesis methodology comprised of proposed low-power logic options in FinFET design library has been developed. Results show about 8.5% area savings and 18% power savings over conventional FinFET technology for ISCAS85 benchmark circuits in 45-nm technology with no performance penalty.

For the first time, they have proposed a novel bottom spacer fin-shaped field-effect-transistor (FinFET) structure for logic applications suitable for system-on-chip (SoC) requirements. The proposed device achieved improved short-channel, power delay, and self-heating performance compared with standard silicon-on-insulator FinFETs. Process aspects of the proposed device are also discussed in Mayank Shrivastava et al.[5]. Physical insight into the improvement toward the short-channel performance and power dissipation is given through a detailed 3-D device/mixed-mode simulation. The self-heating behavior of the proposed device is compared with standard FinFETs by using detailed electro-thermal simulations. The proposed device requires an extra process step but enables smaller electrical width for self-loaded circuits and is an excellent option for SoC applications.

Shivani Chopra et al. [6] provides an overview of the issues faced by the downscaling of MOS devices. For retaining growth in device density, the scaling issues like the power supply and threshold voltage scaling, hot carrier degradation, gate oxide tunneling, random doping fluctuation, high electric field, parasitic resistance and capacitance, source to drain tunneling, short-channel effect should be well understood. A possible way for the microelectronics industry to keep up the high-density pace is to shift from the traditional MOSFET based standards to one based on nanostructures at the molecular level.

CMOS technology scaling has been a basic key for continuous progress in silicon-based semiconductor industry. Scaling is followed by Moore's Law since few decades which provided simple rules for transistor design to increase circuit density and speed. The improved circuit performance and density enable more complicated functionality, since more transistors can be integrated on one single chip. However, as device scaling continues for the 21st century, it turns out that the historical growth, doubled circuit density and increased performance followed by Moore's Law cannot be maintained only by the conventional scaling theory. Increasing leakage current does not allow further reduction of threshold voltage, which in turn prevents further supply voltage scaling for the speed improvement. Higher electric fields generated inside of the transistor worsen device reliability and increase leakage currents. Moreover, the required high channel doping causes

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significant challenges such as mobility degradation and random dopants induced threshold voltage fluctuations.

As the device scaling is approaching its physical size limitations, various researches have been actively carried out to find an alternative way to continue Moore's law. The technology cycle is getting slow down due to increasing power consumption, process variation, and fabrication cost. Nowadays device scaling tradeoffs between performance and power consumption, therefore technological innovations which can achieve high performance through very low power are required. If some efforts are being made to maintain the advanced CMOS technology, it cannot go beyond few decades. Hence emerging devices should be considered in order to comply with technology developments in the near and far future.

Today's major concerns in designing VLSI circuits have been the amount of power dissipated by these circuits. The Adiabatic logic technique is becoming an answer to the problem of power dissipation. The term 'Adiabatic' refers to the change of state that occurs without the loss or gain of heat. The adiabatic switching technique reduces the power dissipation during switching events. But, adiabatic circuits highly depend upon power clock and parameter variations. In this paper Preeti Bhati et al.[7], mux, one bit sum and carry adder are designed and simulated on cadence Virtuoso using 180nm technology. In an analysis PFAL is compared with conventional CMOS logic on the basis of frequency and supply voltage. The proposed technique shows the reduction of power dissipation as compared to the conventional CMOS design style. And results analysis accomplishes that adiabatic logic can be used for the implementation of relatively large, complex circuits that dissipate less energy than conventional CMOS designs.

In Jitendra Kanungo et al.[8],they have analyzed the energy performance of a complete adiabatic circuit/system including the Power Clock Generator (PCG) at the 90 nm CMOS technology node. The energy performance in terms of the conversion efficiency of the PCG is extensively carried out under the variations of supply voltage, process corner and the driver transistor's width. They have proposed an energy-efficient singe cycle control circuit based on the two-stage comparator for the synchronous charge recovery sinusoidal power clock generator (PCG). The proposed PCG is used to drive the 4-bit adiabatic Ripple Carry Adder (RCA) and their simulation results are compared with the adiabatic RCA driven by the reported PCG. They have also simulated the logically equivalent static CMOS RCA circuit to compare the energy saving of adiabatic and non-adiabatic logic circuits. In the clock frequency range from 25 MHz to 1GHz, the proposed PCG gives a maximum conversion efficiency of 56.48%. This research work shows how the design of an efficient PCG increases the energy saving of adiabatic logic.

Adiabatic logic circuits offer significant reduction in power dissipation when compared with static CMOS. Subthreshold adiabatic logic is a new energy recovery logic. In P.Kalyani et al.[9],the efficiency of all logic gates with this novel logic is compared with conventional counterpart. The performance of each logic gate circuit and energy consumption is studied in terms of different technologies, supply voltages and operating frequencies. The proposed circuits are designed and simulated using CADENCE technology. The simulation results shows that the subthreshold adiabatic logic saves more than 90% of power compared to static CMOS.

Akash Agrawal et al. [10] reviews the different adiabatic logic families. Different logic gates have been implemented using different logic families and using proposed DCDB-PFAL logic at different frequencies and for different values of dc voltages for the new logic circuit. Finally a combinational circuit 2:1 MUX has also been implemented for the proposed and the conventional logic. From the simulation of existing logic families we have seen that PFAL logic family provides much lower power dissipation as compared to ECRL and 2N- 2N2P logic family. And from the simulations carried out in this paper we have seen that the proposed DCDB-PFAL logic circuits it offers significant power reduction over all other logic families and achieves even better performance and much lower power dissipation than PFAL logic family. It can be seen from different graphs plotted, that as the dc voltage is varied between 0.1V to 0.3V, power first decreases up till around 0.25V and then increases gradually. The proposed DCDB-PFAL logic can be used in devices which need ultralow power for their working such as hearing machine, pacemaker and other medical purpose devices. As the quest for ultra-low power circuit designs goes on increasing, these improved circuit technologies would prove to be very useful in serving the need for ultra low power circuit designing.

III. FinFET TECHNOLOGY

3.1 Overview:

FinFETs are quasi-planar field-effect transistors. The working principle is same as that of planar MOSFET. Figure 3.1 shows the structure of a FinFET. The gate shawls around the fin. The channel is formed perpendicular to the plane of the wafer. Its length is shown as LG. This is the reason that the device is termed quasi-planar. The effective width of a FinFET is 2nHfin, where n is the number of fins and Hfin is the fin height. Multiple fins led to make a high on-current transistor. FinFET width is quantized, in terms of number of fins. Some key design factors like performance, power and functionality, profound on ratio are also dealt. Beyond the technology-driven benefits offered by FinFETs, circuits can also benefit from the double gate structure of FinFETs to further optimize power and performance. FinFET leads to some interesting designs by means of etching out the top part of the device that achieves independent gate structure.

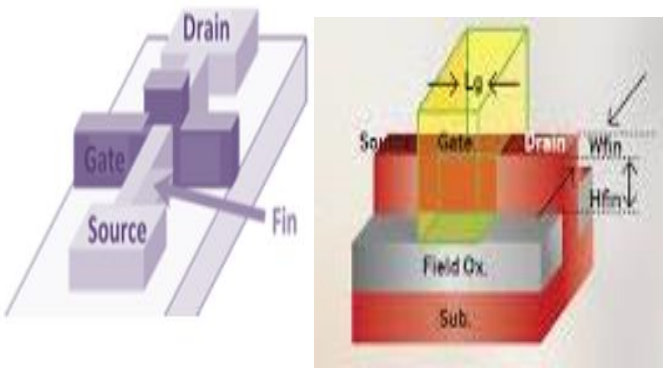

Figure 3.1 Structure of the FinFET

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3.2 Working Principle of FinFET

The working principle of a FinFET is similar to that of a conventional MOSFET. The MOSFET can function in two modes: enhancement mode and depletion mode for both p-channel and n-channel MOSFETs. The channel shows maximum conductance when there is no voltage on the gate terminal. As the voltage changes to positive or negative, the conductivity of the channel reduces.

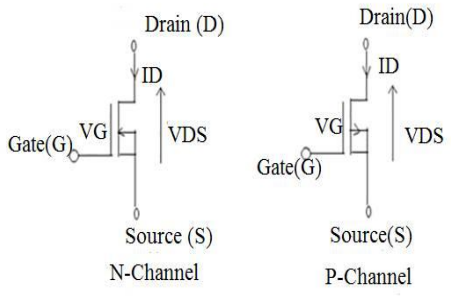

Fig.3.2 Depletion mode MOSFET

In enhancement mode of MOSFET, when there is no voltage on the gate terminal, it does not conduct. Unlike the depletion mode, in enhancement mode, the device conducts better when there is more voltage on the gate terminal. The main aim of the MOSFET is to control the flow of voltage and current between the source and drain terminals. A high quality capacitor is formed by the gate terminal. The gate is composed of the silicon oxide layer, the p-body silicon and gate metallization and the p-body silicon. This capacitor is the most vital part. The semiconductor surface at the below oxide layer which is located between source and drain terminal. This is inverted from p-type to n-type by applying a positive or negative gate voltage respectively. When a small amount of voltage is applied to this structure (the capacitor), keeping gate terminal positive with respect to source, a depletion region is formed. This depletion region is formed at the interface between the silicon and the SiO2.The positive voltage applied attracts electrons from the source terminal, the drain terminal as well as the n+ source. This forms the electron reach channel. If voltage is applied between the source and drain terminals, current will flow between source and drain terminals. The concentration of electrons is controlled by the gate voltage (Vg).

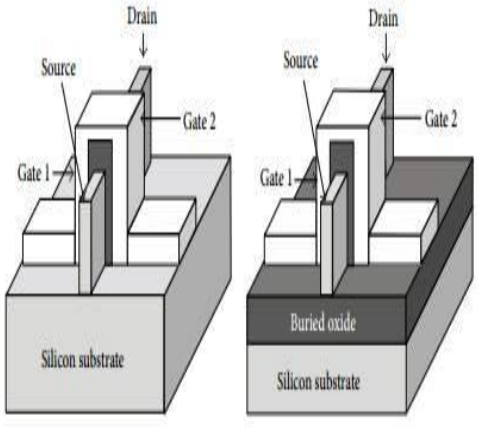

Fig 3.3 Cross sectional view of FinFET

If a negative voltage is applied, a hole channel will be formed under the oxide layer. Now, the controlling of source to gate voltage is responsible for the conduction of current between source and the drain. If the gate voltage exceeds a given value, only then does the conduction begins.

3.3 Advantages of FinFET

The advantages of the FinFET is shown in Table -I.

Table I. Advantages of FinFET

FINFET ADVANTAGES	
PARAMATER	**DETAILS**
Power	Much lower power consumption allows high integration levels. Early adopters reported 150% improvements.
Operating voltage	FinFETs operates at a lower voltages as a result of their lower threshold voltage.
Feature Sizes	Possible to pass through the 20nm barrier previously thought as an end point.
Static leakage current	Typically reduced by up to 90%
Operating speed	Often in excess of 30% faster than the non-FinFET versions.

3.4 Applications of FinFET

- Low power design in digital circuit, such as RAM, because of its low off-state current.
- Power amplifier or other application in analog area which requires good linearity.
- World leader in smartphones, Samsung Electronics has incorporated FinFet in its 14nm processors (Exynos7 Octra). This processor is used in the latest Samsung smartphone, the Samsung Galaxy S6.
- In 2020,along with Samsung, Apple, Intel and TSMC Samsung and TSMC are ramping up 5nm and various half-nodes offerings. 3nm is in R&D. This technology will benefit all smartphones as it will speed up the phone.

IV.PROPOSED SYSTEM

4.1 Objective

Design of portable devices required with less power consumption, lesser area and increased speed of operation The leakage power is increasing where the technology related with CMOS process which is to be reduced by implementing the same using adiabatic logic on FinFETs. To design the 4-bit ALU with three arithemetic operations(ADD,SUBTRACT, COMPARE(^{1}A<B ^{2}A>B) and four logical operations(AND, OR, XOR, NOT) using FinFET Technology.

4.2 Overview of the Proposed ALU

In digital electronics, an arithmetic logic unit (ALU) is a digital circuit that performs arithmetic and bitwise logical operations on integer binary numbers. The designed ALU circuit performs addition/subtraction and comparator operations and some of the logic functions.

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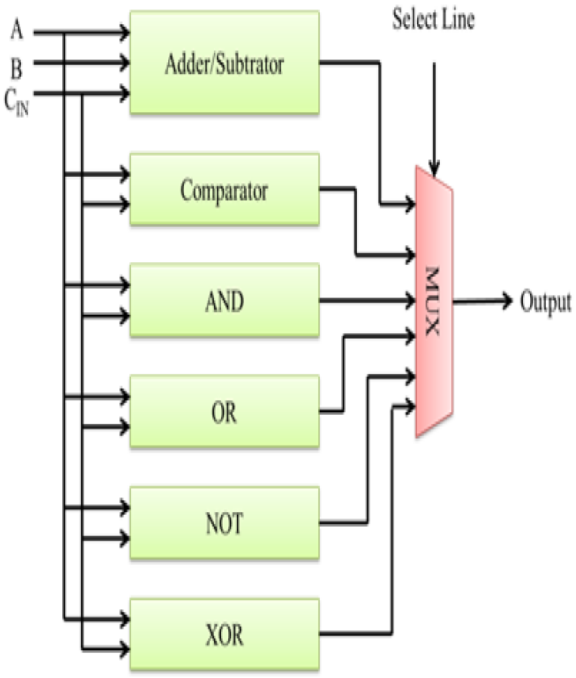

Fig 4.1Block Diagram of the Proposed ALU

The overall block diagram of the proposed ALU is in shown in Figure 4.1. In the above diagram, full adder/subtractor has 3 inputs so we take three inputs namely A, B and Cin. Other than adder/subtractor all the operations only needs 2 inputs. The functions are selected by multiplexer with select line and then we obtain the output.

4.3 Design of 4-bit ALU

4-bit ALU is designed by cascading four 1-bit ALU blocks. Each 1-bit ALU is composed of the following three components:

l. Arithmetic 4: 1 multiplexer,
2. Logical 4:1 multiplexer,
3. 2:1 multiplexer to select either arithmetic or logical operation

Each bit uses three multiplexers and one full adder. The detailed block diagram of 4-bit ALU is shown in figure 4.2.

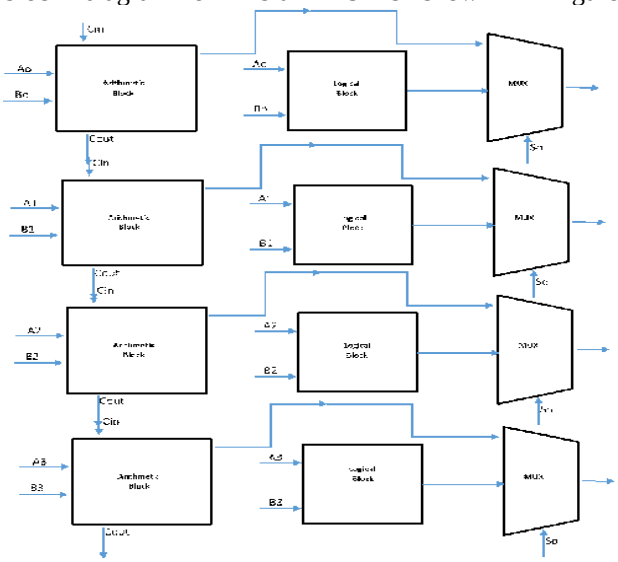

Fig 4.2 Detailed Block Diagram of 4 Bit ALU

The 4: 1 multiplexers have two select inputs SO and SI. The MUXs are used to provide the proper input signal for the adder circuit depending on the operation being performed on the proper input signal and also to pass the output of the full adder to 2:1 multiplexer for further selection. The select line S2 used for 2: 1 MUX for selecting the arithmetic function (S2=O) and logical function (S2=1), as shown in table II.

Table II. Operation of ALU

S2	S1	S0	Operation
0	0	0	Addition
0	0	1	Subtraction
0	1	0	Compare(A<B)
0	1	1	Compare(A>B)
1	0	0	AND
1	0	1	OR
1	1	0	EXOR
1	1	1	NOT

4.3. Arithmetic Operations

Arithmetic or arithmetics is the oldest and most elementary branch of mathematics. It consists of the study of numbers, especially the properties of the traditional operations between them addition, subtraction, multiplication and division. Arithmetic is an elementary part of number theory, and number theory is considered to be one of the top-level divisions of modern mathematics, along with algebra, geometry and analysis. The designed arithmetic logic unit does the arithmetic operations of addition, subtraction and comparison operations. The comparator consists of lesser, greater and equal operations.

4.4 Logic Operations

A digital Logic Gate is an electronic device that makes logical decisions based on the different combinations of digital signals present on its inputs. Digital logic gates may have more than one input but generally only have one digital output. Individual logic gates can be connected together to form combinational or sequential circuits, larger logic gate functions. The proposed ALU circuit does various logic operations such as AND, OR, NOT and XOR. Each and every gate structure replaced with FinFET.

4.5 Multiplexers

Multiplexers are used to combine data from different sources to one single data. The select lines helps the mux to select a particular input to be switched as an output.. In this study, 2:1 MUX and 4:1 MUX, were designed and simulated. The 2:1 MUX is designed with 2 inputs, 1 select line, and an output. A 4:1 MUX is designed with 4 inputs, 2 select lines and an output.

4.6 Validation using Adiabatic Approach

Adiabatic circuits are low power circuits that use "reversible logic" to conserve energy. Unlike traditional, that dissipate energy throughout change, adiabatic circuits commit to conserve charge by following 2 key rules: Never activate a transistor when there's a voltage potential between the supply and drain. Never put off a semiconductor unit once current is flowing through it. Adiabatic logic based full adders has been proposed and then this can be compared with the XOR and the XNOR based full adders.

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4.6.1 Efficient Charge Recovery Logic (ECRL):

A pair of pull-down Nmos network and pull-up Pmos network forms the logic in ECRL. Both pre-charge and assessment (evaluation) are conducted concurrently in this technique. It removes diodes use and thus has less energy dissipation. It has weak zero logic due to the threshold voltage of Pmos. Therefore, the ECRL circuit has less noise-margin. Figure shows the ECRL adiabatic logic overall block diagram. A simple inverter circuit implementation using the ECRL adiabatic logic is shown in the figure 4.3.

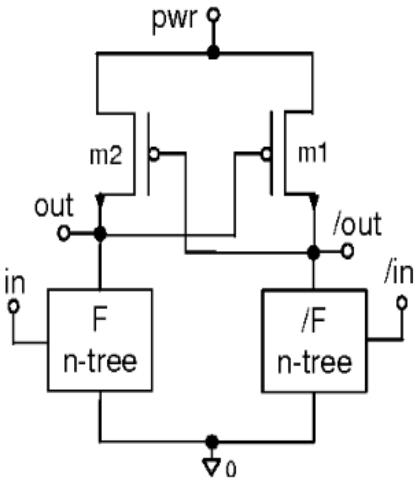

Figure 4.3.ECRL logic based Inverter Circuit

Power clock used in adiabatic technique, comprises of four different phases. These are:

(i) Evaluate (E) - In E interval, i.e., in the evaluation phase, the outputs get evaluated from the stable input signal.
(ii) Hold (H) - During H interval, i.e., the Hold phase, the output is kept stable to provide input to the next stage.
(iii) Recovery (R) - During R interval, i.e., the recovery phase, the energy gets recovered and
(iv) Wait (W) - W interval, i.e., the wait interval provides symmetry.

IV.RESULTS AND DISCUSSIONS

Each 1bit ALU have an Arithmetic block and logical block. The arithmetic block has adder, subtractor and comparator given to 4:1 MUX. The schematic of the arithmetic block and the output of the corresponding circuit is shown in the fig 5.1 and fig 5.2 respectively.

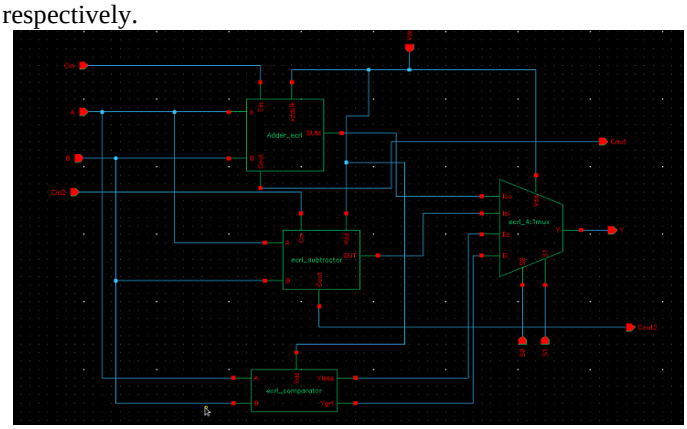

Fig 5.1 Design of Arithmetic block

Fig 5.2 Simulation results of Arithmetic block

The logical block has AND, OR, NOT and XOR operators given to 4:1 mux. The schematic of the logical block and the output of the corresponding circuit is shown in the fig 5.3 and fig 5.4 respectively.

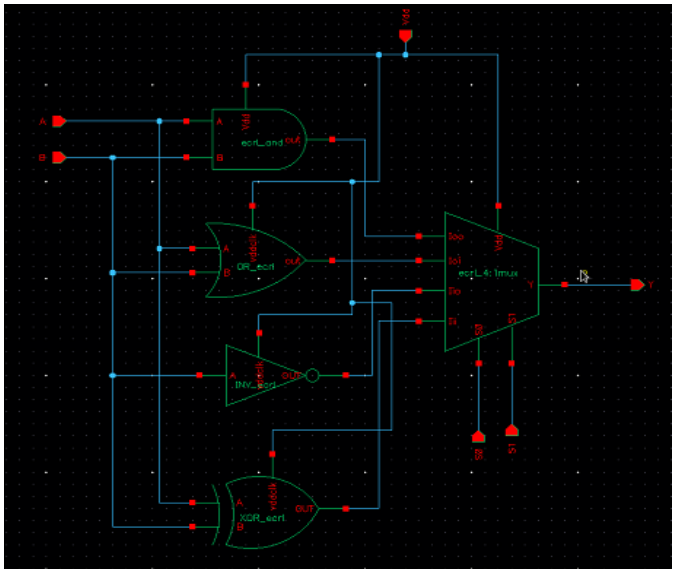

Fig 5.3. Design of Logical Block

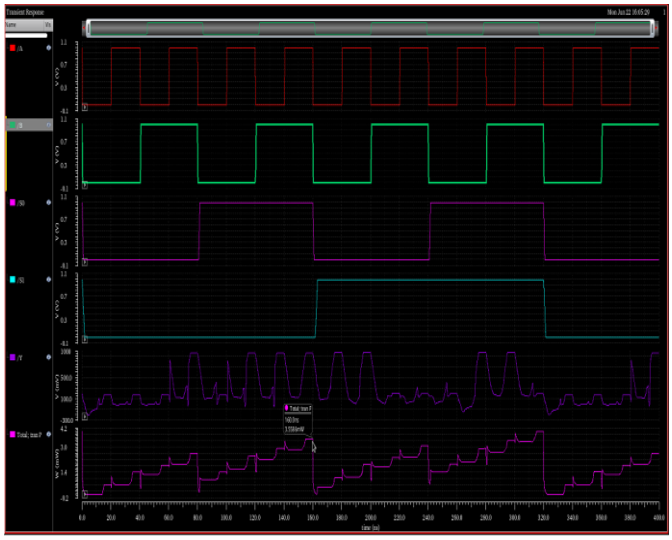

Fig 5.4. Simulation results of Logical Block

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The below figure 5.5 and fig 5.6 shows the complete schematic design of the 4 bit ALU and its simulation output.

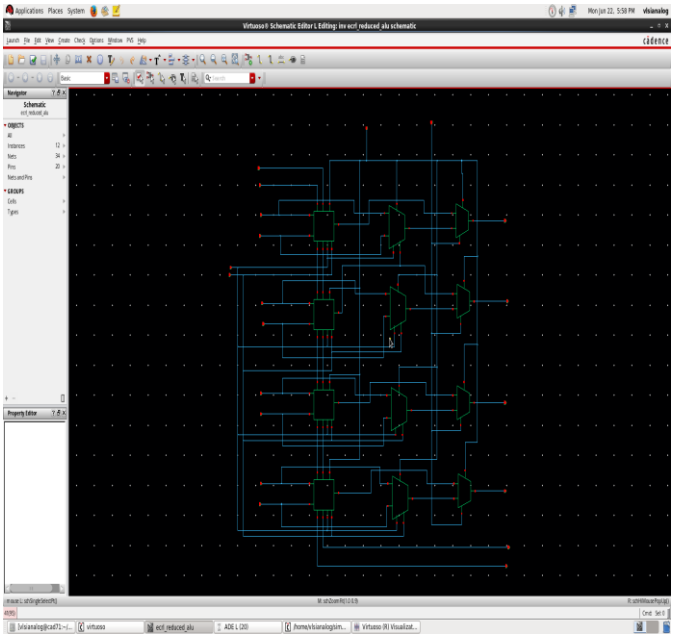

Fig 5.5 Design of complete 4 Bit ALU Block

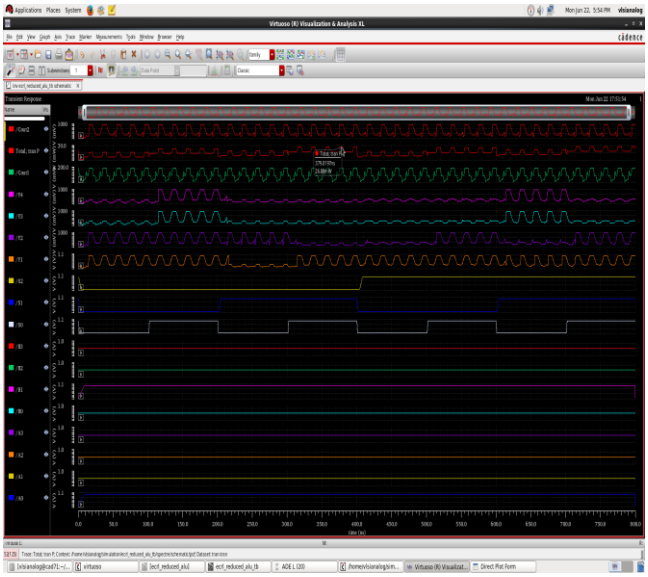

Fig 5.6 Simulation Results of 4 Bit ALU Block

Table III shows the comparison of power between the existing model[13] with the proposed model.

Table III: Power comparison of the 4-Bit ALU

	Power report of existing model (mw)[13]	Power of proposed model
AND Gate	0.693	533.939µw
OR Gate	1.493	713.62µw
XOR Gate	1.493	707.584µw
2:1 MUX	3.628	910.727µw
4:1 MUX	12.933	2.05mw
1 Bit Adder	2.076	3.3991mw
Logical Block	19.708	4.0158mw
Arithmetic Block	10.976	5.9414mw
ALU	54.028	23.93mw

Table III: Timing Analysis of 4-Bit ALU

	Delay
AND Gate	38.46E-9
NAND Gate	325.0E-12
OR Gate	38.10E-9
NOR Gate	33.10E-9
NOT Gate	28.25E-9
XOR Gate	40.26E-9
XNOR Gate	33.10E-9
2:1 MUX	17.80E-9
4:1 MUX	159.9E-9
1 Bit Adder	78.70E-9
Subtractor	80.11E-9
Comparator	79.00E-9
Logical Block	99.90E-9
Arithmetic Block	139.9E-9
ALU	403.5E-9

VIII. CONCLUSION AND FUTURE SCOPE

The design of the 4-bit ALU have been designed by using the sub blocks of full Adder, 4xl and 2xl multiplexers, and gates like exclusive-or, and, or and inverter. The ALU performs a total of eight operations, out of which four are arithmetic and remaining are logical operations. The three arithmetic operations performed are Adder, Subtractor, and Comparator and the four logical operations are AND, OR, XOR and NOT. The power is reduced 54.028mw to 23.93mw when compared with the existing ALU and the obtained delay by the design is observed to be 403.5E-9. Hence the power is reduced.

The proposed design can be tested for low on chip power density further. Though we have utilized the pulsed power source efficiently, propagation delay can further be reduced by more efficiently utilizing the pulsed power supply as VDD source. Further the performance of proposed schematic may be increased by checking noise margin and current at different nodes. Thus the FinFET based architecture can be expanded for other applications like communication and biomedical processor core. A reliable future work can be carried out in designing higher bit of ALU and other complex processing circuits using this ALU. As a final remark, we have proposed an alternative approach to the existing CMOS circuits ith smaller power, delay and faster devices. Further work can be done by implementing the other error detection and correction codes like Reed solman and Goley codes with proposed circuits to get high performance, low power and fault secure codes.

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