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Design and Implementation of 3*3 Array Multiplier using DPTL Logic

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Abstract: **A multiplier is one of the most important building blocks that is widely used in processor, embedded, VLSI applications, and in DSP applications. The three main thrust parameters of any VLSI Design lie in power, speed and area these three are the prime design constraints for portable electronics devices and signal processing applications. An array multiplier is a digital combinational circuit used for multiplying two binary numbers by employing an array of half adders and full adders. This is a fast way of multiplying two numbers. The Array architecture is a popular technique to implement the multipliers due to its compact structure. In this paper 3*3 array multiplier using DPTL have been designed. In this we are using a variety of EXOR gates with reducing power consumption and acquiring low power dissipation and minimum delay. By using double pass transistor logic (DPTL) EXOR gate to design a full adder with better results compared to CMOS technology. An array multiplier circuit is designed by using this full adder and it also responsible for reducing the power consumption. Simulation results are carried out using Mentor Graphics tool in 130nm technology.**

Keywords: Array multiplier, DPTL logic, Delay, EXOR gate, Multiplier, Mentor Graphics tools, power.

I. INTRODUCTION

Multiplier plays an important role. Multiplier circuit is based on add and shift operation. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. An array multiplier is one of the most critical functions carried out by ALU. Digital multiplication is the most extensively used operation, people who design digital signal processors sacrifice a lot of chip area in order to make the multiply as fast as possible.

CMOS (complementary metal oxide semiconductor) as a switch must be conducting to allow current flow between source and drain terminals. In CMOS logic, the input is applied to the p-type transistor either from voltage source/anode p–type. Similarly, the input is applied to the n-type transistor either from ground/cathode n-type.

In this, we are using CMOS technique. It is also known as complementary symmetry metal oxide semiconductor (CMOS, is a type of MOSFET. Fabrication process uses complementary and symmetrical pairs of p-type and n-type MOSFET for logic functions. CMOS technology is used for constructing integrated circuits.

In today's world the increasing in number of transistors on chip, power dissipation is increasing in CMOS circuits. New logics are introduced to reduce the transistors count and power dissipations in the upcoming circuits.

To overcome the problems in Complementary Pass Transistor Logic like noise margin speed degradation at reduced power supply voltage. Double pass transistor logic is the modified circuit of complementary pass transistor logic. Double pass transistor logic uses both PMOS and NMOS devices. The NMOS and PMOS transistors are arranged parallel to each other. Double pass-transistor logic attracts much attention due to its low power dissipation.

II. EXOR GATE IMPLEMENTATION USING CMOS LOGIC

In this we are designing CMOS EXOR gate with the help of PMOS and NMOS transistors. This gate is called as EXOR or exclusive OR gate because, its output is only high when one of its input is exclusively high. An EXOR gate is normally two input logic gates where, output is logical high when only one input is high. When the two inputs are equal, that is two inputs are high or two inputs are low the output will be low.

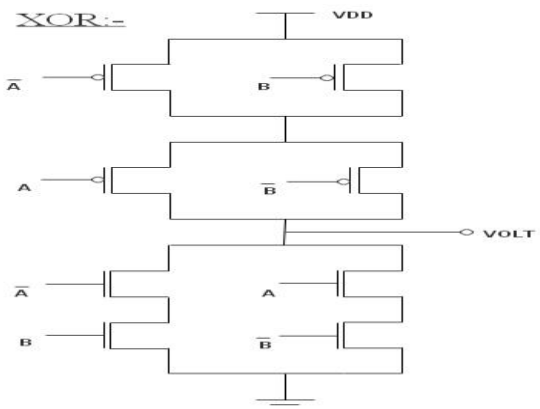

Fig 1: Schematic of two input EXOR gate

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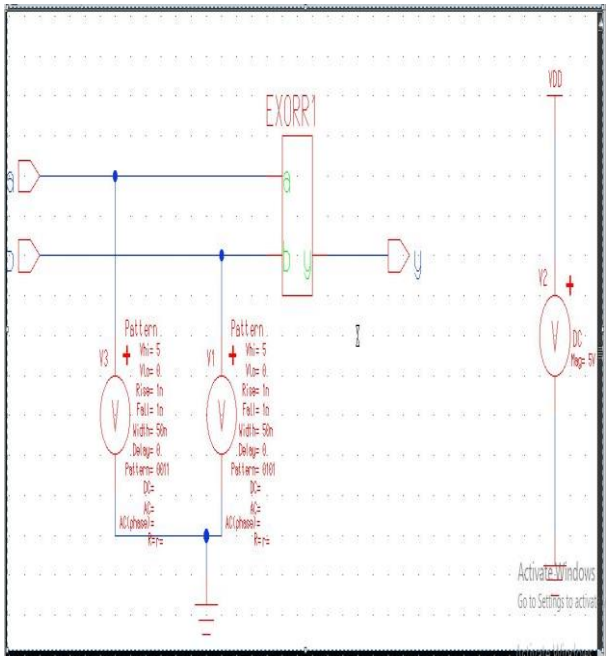

Fig 2: Simulation circuit of EXOR gate

The resultant simulation waveforms of exor gate with transistor level are obtained in mentor graphics tool.

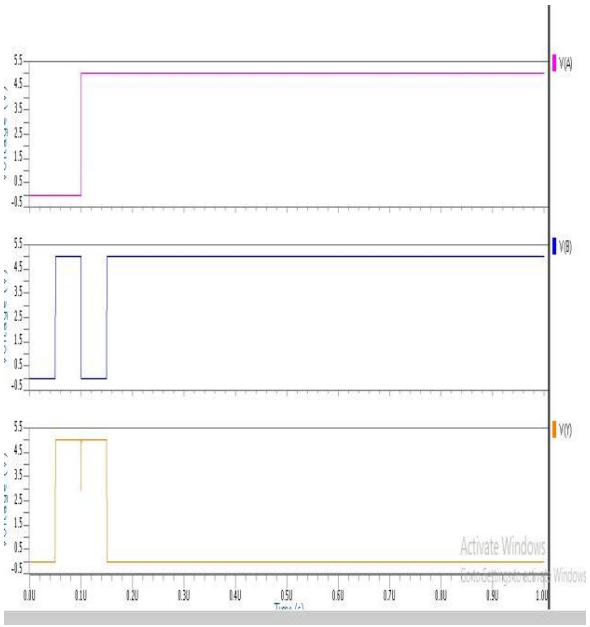

Fig 3: Simulation waveforms of EXOR gate

The existing EXOR gates are simulated using mentor graphics tool with the voltage of 5V using 130nm CMOS technology. The transient analysis of the circuit results is shown with the voltage of 5V. By using NMOS and PMOS transistors EXOR gate the power dissipation more because the greater number of transistors are used in the designing. The increase in transistor count then the power dissipation also increases.

III. PROPOSED CIRCUIT OF EXOR GATE

Double pass transistor Logic (DPTL) is modified version of Complementary Pass transistor Logic (CPL) that meets the requirement of reduced supply voltage design. PMOS transistor has been connected in parallel with NMOS to produce a full swing like full V_{DD} or full ground at the output to avoid the delay problems in existing circuit. Here we are using both PMOS and NMOS it is called double pass transistor logic (DPTL). To overcome the drawback of CPL, DPTL has been developed for low power applications and the advantage is either PMOS or CMOS can be used to implement the logic design. In this paper all the logic circuits have been implemented by DPTL.

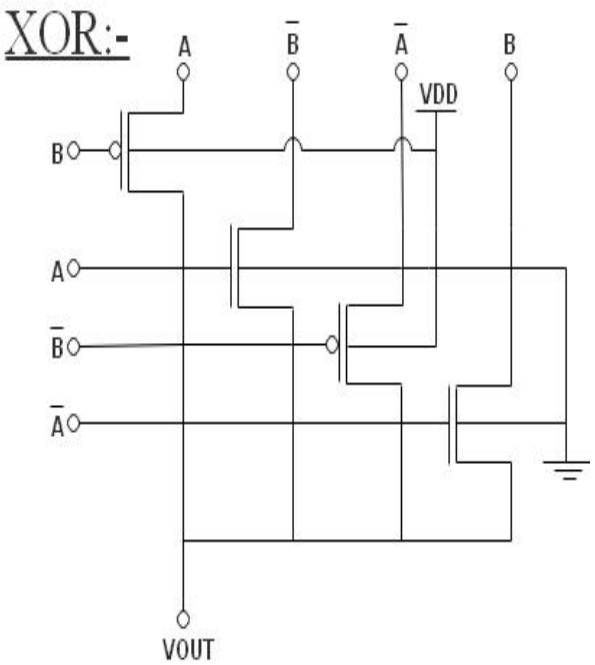

Fig 4: Structure of the double pass transistor logic (DPTL)

A Double Pass Transistor Logic (DPL) XOR gate is shown above figure.

In this double pass transistor logic XOR gate, we have four inputs and one output. Actually, we are having two inputs and also considering the complements of the inputs so total we have four inputs.Here we don't use inverters to gibe the complement inputs because if we use inverters the transistor count will inctease then power dissipation also increases.so ,we have to give the complementary inputs directly . But the operation is same as the CMOS XOR Gate.Based on the inputs the output will come in this we are using two PMOS andtwo NMOS transistors to design a double pass transistor logic XOR gate.

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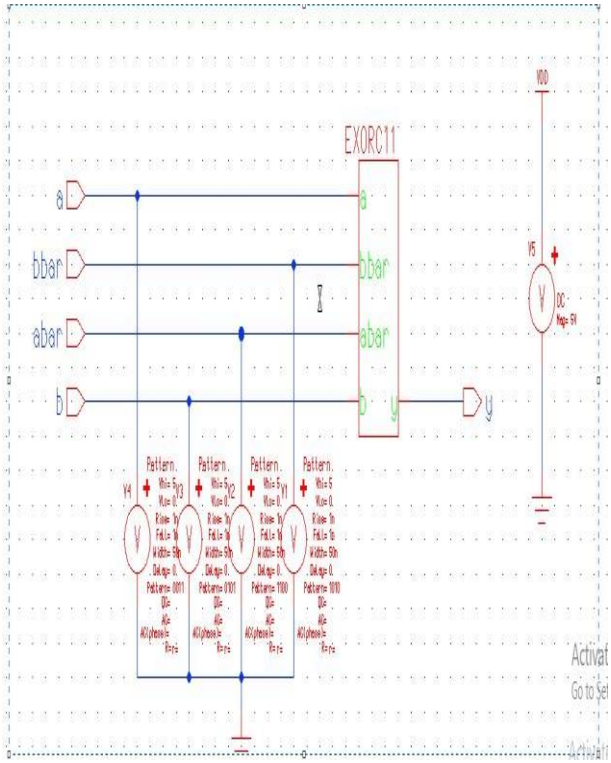

Fig 5: Simulation diagram of DPTL logic

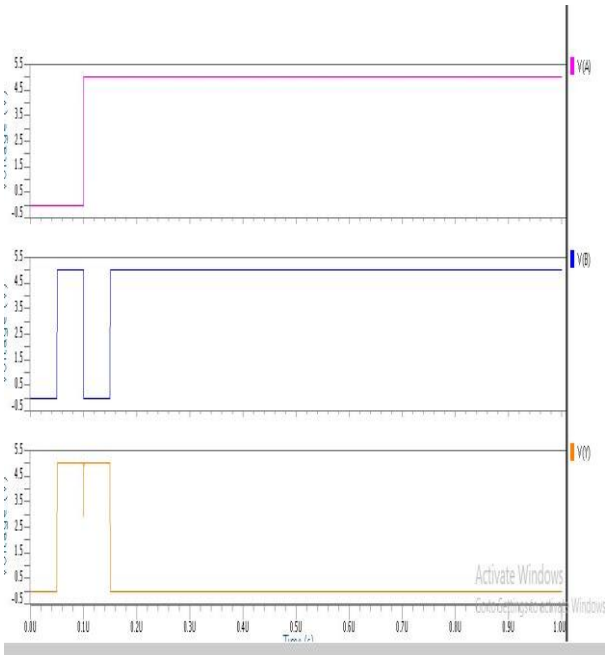

Fig 6: Simulation waveforms of DPTL Logic

IV. PROPOSED ARCHITECTURE OF ARRAY MULTIPLIER

The array multiplier is digital combinational circuit that is used for multiplication of two binary numbers by employing an array of full adders and half adders. A basic multiplier can be divided into three sections partial product generation, partial products addition and final addition. This is a fast way of multiplying two numbers since all it takes is the time for the signals to propagate through the gates that form the multiplication array.

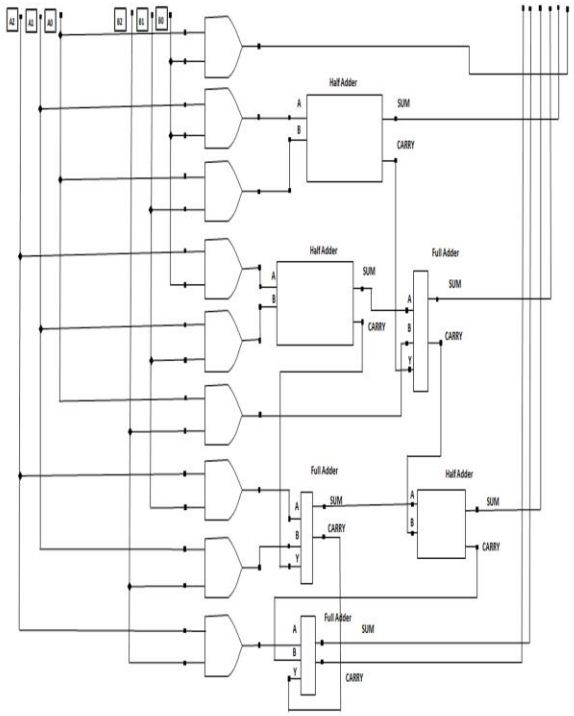

Fig 7: Architecture of 3x3 Array multiplier

In this, the proposed logic is double pass transistor logic array multiplier. The array multiplier produces partial products. The double pass transistor logic 3*3 array multiplier is designed. In the power applications average power consumption is a critical design concern.

Leakage current which is primarily determined by the fabrication technology, consists of reverse bias current in parasitic diodes formed between source and drain diffusion and the bulk region in a MOS transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage.

V. RESULTS AND DISCUSSION

In the proposed array multiplier, the full adder cells and half adder cells are implementing by using double pass transistor logic (DPTL). The full adders and half adders are designed using inverter based four transistor XOR gate to reduce the power dissipation.

This full adder cell has less power consumption as it has no direct path to ground. The elimination of a path to the ground reduces power consumption. Throughput is a measure it is defined by how many multiplications can be performed in a given amount of time for a combinational multiplier throughput is a function of latency.

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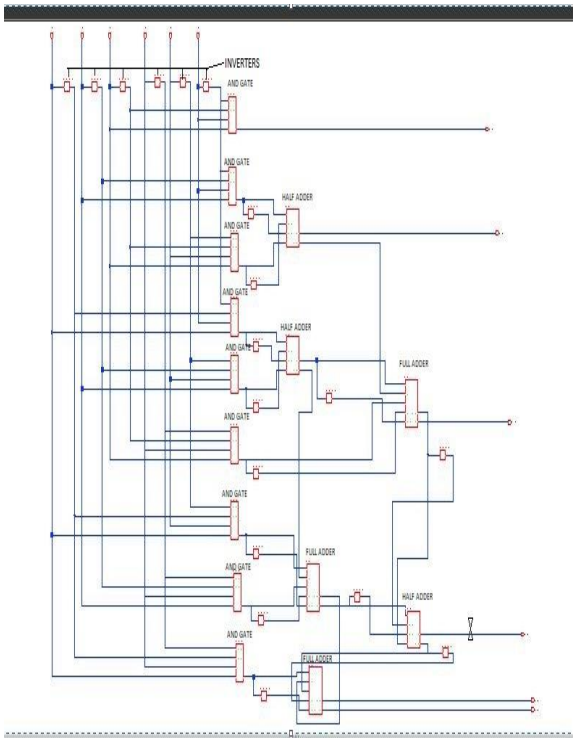


Fig 8: Schematic diagram of 3x3 array multiplier using DPTL Logic

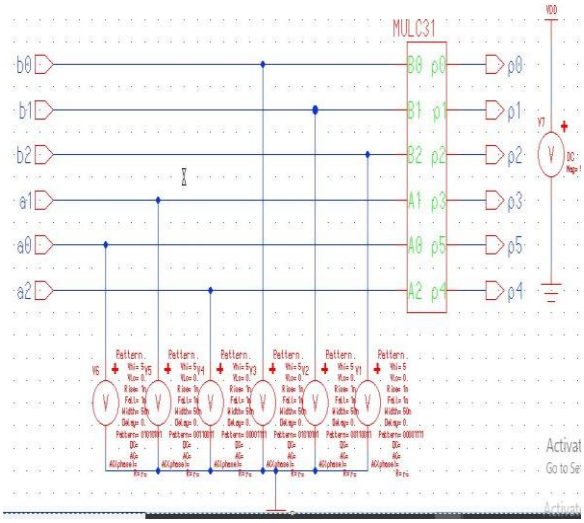
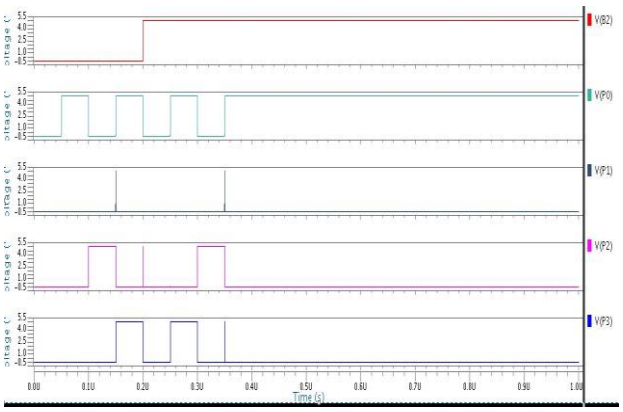


Fig 9: Simulation diagram of 3*3 Array Multiplier



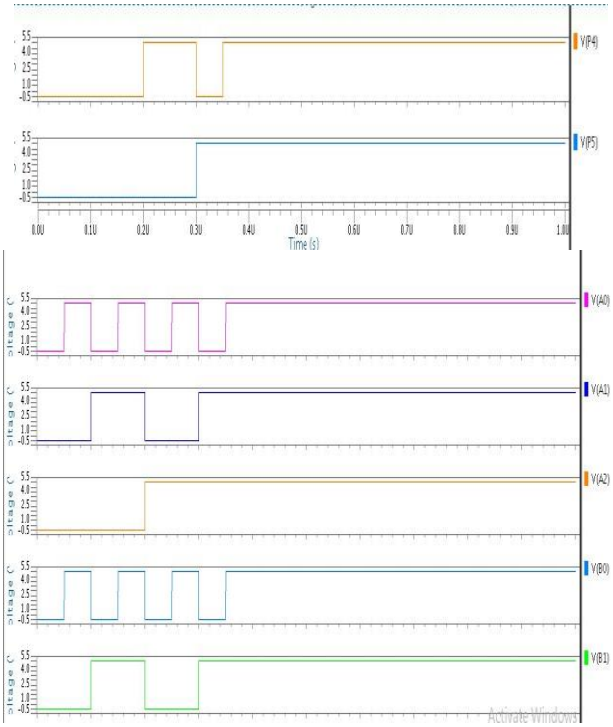


Fig 10: Simulation waveform of 3x3 multiplier using DPTL logic

Table 1: Comparative study between CMOS and DPTL systems.

LOGIC	*CMOS*	DPTL
NAND	42.3801 n watts	0.1000117n watts
NOR	152.5587 n watts	76.3802 n watts
XOR	296.499 n watts	250.727n watts
HALF ADDER	319.4589 n watts	97.6121 n watts
FULL ADDER	812.6841 n watts	521.6269 n watts
2*2 ARRAY MULTIPLIER	1120.7 n watts	500.742 n watts
3*3 ARRAY MULTIPLIER	3603.3 n watts	3231.7 n watts

It is concluded from Table 1 that alone passive or active systems are not appropriate and sustainable due to increasing energy demand trend in space heating/cooling. It forces us to adopt suitable hybrid systems according to tailor made situations.

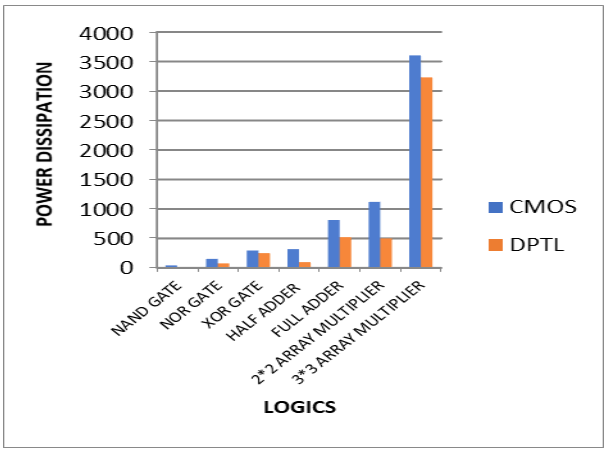


Fig 11: Power Dissipation Comparison Chart

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IV. CONCLUSION

In this paper, the proposed array multiplier is using full adder is simulated using 130nm CMOS technology. Performance parameters like power dissipation and so on are efficient in the design of array multiplier using Double Pass Transistor Logic as compared to the CMOS transistor logic. By reducing the power dissipation, the life of battery will be increased and more reliability, this is mostly preferably rather than CMOS logic. The conclusion is that, as the major application of array multiplier is the speed of the operation i.e., the performance should be high. The performance efficiency of a multiplier is increased with the design of Double pass transistors. While comparing the CMOS array multiplier with Double Pass Transistor multiplier, the power dissipation is reduced which optimizes the performance of a multiplier.

V. FUTURE SCOPE

Double pass transistor logic is a modified version of complementary pass logic, which is used to improve the circuit performance at reduced voltage level .This technique can be combined with asynchronous adiabatic logic (AAL) to obtain energy saving benefits and power benefits with improved circuit performance in full adder and multiplier designs in the digital circuits .

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