Design and Implementation of 16-Bit Carry Look Ahead Adder Using Cadence Tool

P. Suveetha Dhanaselvam[1,2], K.Hamsa Nandhini [1,3], M.Rajammal [1,4], S. Satheeswari [1,5].
[1] Velammal College of Engineering and Technology, Madurai, Tamilnadu.
[2] Associate Professor, Electronics and communication Engineering, Madurai, Tamilnadu .
[3.4.5] Final year, Department of Electronics and Communication Engineering, Madurai, Tamilnadu .

***Abstract* - Carry Look Ahead Adders are also called as fast adders as it reduces the time compared to other adders by propagating carry before the sum output, leads to great performance. In our project, a 16-Bit Carry Look Ahead Adder is implemented using cadence tool and their Transient and DC responses are analyzed. Using the logical expressions for the carry propagation (P) and carry generation (G) the carry and sum of the adder (1-Bit) is generated. Then 1 bit carry is implemented in virtuoso schematic editor and the new cellview for the carry block will be created which is given as an input for adder implementations. The transfer characteristics of the adder is analysed through the virtuoso visualization to study the characteristics of the 1 bit carry look ahead adder. Then the bit rate is extended to 4 bit. Using this 4 bit adder, 16 bit adder will be implemented using Cadence tool. In this paper, the adder is simulated in Cadence Virtuoso IC 6.1.5 and version 11.1.0.523 isr15 32 bit.**

INTRODUCTION:

Carry Generation for each bit results in delay for many adder circuits in advanced digital systems. It heavily impacts the overall performance of digital systems [1]. Various adder structures can be used to execute addition such as Carry Select Adders, Carry Increment Adders, Carry Skip Adders, etc[5]., we have chosen Carry Look Ahead Adder since this adder reduces the delay by reducing the number of gates through which a carry signal must propagate in the generation and propagation values are computed[3]. Internal carry generation is calculated in second stage. A fast method of adding numbers is called Carry Look Ahead Adders. This method does not require the carry signal to propagate stage by stage, causing a bottleneck[10]. Carry Look Ahead Adders is a major functional block in Arithmetic logical units due to its high speed operation. The Arithmetic Logic Unit has been widely used in microprocessor systems and mostly in all processing modules of Embedded Systems [3]. Therefore, it is of interest to study the functional behaviour and power consumption of Carry Look Ahead Adder. In general, every processors comprising of adders requires high speed. Therefore speeding up the adders needs the speeding up of the carry chain [3]. We are in the need of less power we go with carry look ahead adder. In arithmetic operation while improving speed of the addition it leads to the speed of all other arithmetic operation. Most cases we prefer carry look ahead adder to reducing the carry propagation delay of adders escort great performance. The Carry Look Ahead Adder is one way to speed up the carry computations. To reduce the working out time the fastest way to add two binary numbers is done by Carry Look Ahead Adders. Cadence helps to design an adder with reduction of delay & memory consumption [9]. It has many inbuilt components so that design process is so simple.

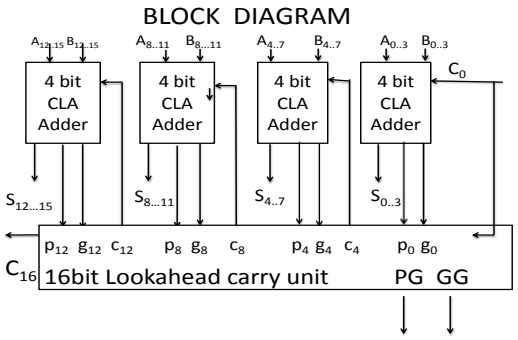

Fig1.1.Block diagram of carry look ahead adder.

To help integrate, verify, and implement complex circuits in a simpler manner .Cadence virtuoso platform is a tool which is used for designing full-custom integrated circuits and includes schematic entry, extraction and back-marginal note. Cadence reduced learning curve with a simulator- independent environment.

Virtuoso Layout suite offers increased performance and efficiency from advanced full custom polygon editing (L) through more bendable schematic-driven and constraint assisted full custom layout (XL), to full custom layout automation (GXL).The virtuoso platform is reversed by the largest number of process design kit(PDKs) available from the world's leading foundries for process node everywhere. It can stimulate circuits from 0.6µm to advanced 7nm process nodes. Cadence enables many innovations in electronic design globally and chairs an essential role in the formation of today's integrated circuits and electronics. Customers use cadence software, hardware, IP, and services to design and verify advanced semiconductor, consumer electronic, networking and tele-communications equipment, and computer systems.

Cadence virtuoso allows user to execute commands faster using user-programmable combine keys and object-sensitive pop-up menus in an advanced manner, which demonstrate appropriate operations. It helps the designers to design in easy way .The speed simulation by using schematic block to create verilog real models.It also easily develops low-power models for analog and custom digital components through a

simplifier user interface. The cadence virtuoso schematic editor offers abundant capabilities to smooth the progress and make it fast and to design easily. Definite components libraries allow faster design at both the gate and transistor levels.Refined wire-routing capabilities and supports in connecting devices.

PROPOSED METHOD

Carry look ahead adders efforts by forming propagate and generate signals(P and G) based on whether a carry is propagated through less significant bit position (with any one input is '1') ,a carry is created in that bit position (both inputs are '1'),or if a carry is killed in that bit position (both the inputs are '0') [2].

CARRY LOOK AHEAD ADDER LOGIC DIAGRAM

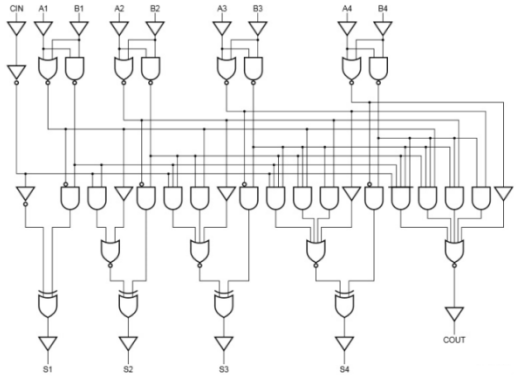

Fig1.2.Logic diagram of carry look ahead adder.

Mostly P is merely the sum output of a half –adder and the carry output of the same adder is G. After P and G are engendered the carries for each bit position are produced[2]. In carry look ahead adder the carry propagator is propagated to next bit which make this as fast adder. The design and implementation of 16-bit carry look ahead adder using cadence tool has many steps. First a 4-Bit adder is designed which is elongated to 16-bit adder.

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TRUTH TABLE

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Expressions for 4-bit:

Carry Generation(G)=AB

Carry propagation(P)=XOR(A,B)

Carry(C):

C0=G0+P0 CIN

C1=G1+P1 C0

C2=G2+P2 C1

C3=G3+P3 C2

SUM(S):

S0=XOR(A0,B0,C0)

S1=XOR(A1,B1,C1)

S2=XOR(A2,B2,C2)

S3=XOR(A3,B3,C3)

CMOS Implementation

The procedures for implementing the CMOS circuit for the expressions are as follows,
In the virtuoso schematic window,

1.Select Tool in the Library Manager.
Tool ⟶Library manager.
2.In the library manger select
File ⟶ New ⟶Library
Fill the name and click ok.
3.An Technology file for new library window appears in that choose "Attach to an existing technology library".
4.Then select
File ⟶New ⟶Cell view.
Choose the **cell** as adder and **view** as schematic.
After clicking ok an empty schematic window appears.
5. By clicking "**Add Instance**" or "i" button the components are added to the window.
6. The basics components are selected from "**AnalogLib**".
7.The pins are attached by clicking "P" and to wire the components "W" are used.
8. After making all connections Save the window.
9. Correct the error if any.
By doing the above procedure the circuit looks like Fig 1.3.

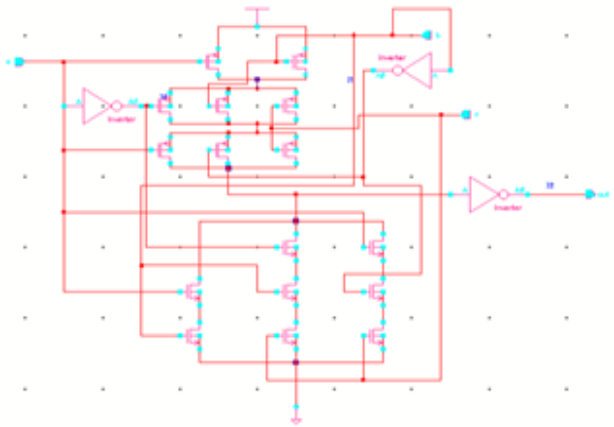

Fig1.3.CMOS Implementation of 1_bit carry.

For generating the symbol:
1. Click creates ⟶cell view⟶from cell view.
Select the inverter name as carry and click ok.

2.An "symbol generation option" window appears which contains the components names.

Check the components and click ok.

3. Now the symbol will be generated.
4. To test the working of the carry, select

File ⟶new ⟶ell view

And the cell name as carry_test.

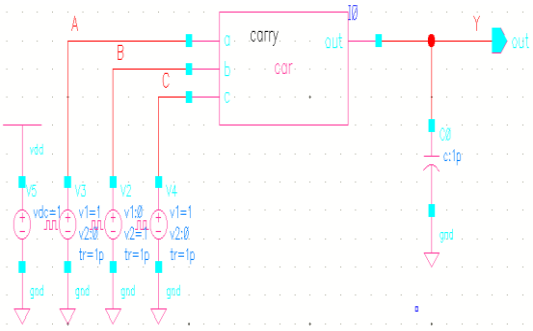

Fig1.4.Symbol generation for carry

5. An Empty window appears in which the carry symbol is placed using the "i" button.
6. The VDC and Vpulse are given.
7. To name the wire click **"L".**
8. Click on the save icon.
9. After this the window looks like Fig.1.2.
10. Now click Launch ⟶ADE L
11. Now an "**Analog design environment**" window appears .In that click variable ⟶

Copy from cellview provides the value for vbias.

12. Now click Output ⟶To be plotted ⟶

Select on schematic.

13. Select the name of the wire to add them.
14. Click Analyse ⟶hoose and select the value for trans and start the simulation. The result will obtain ad shown in Fig.3.3.
15. Do the same for the Dc response.The output will obtain as in Fig.3.2.1.

Adder circuit is implemented by giving 1 bit carry as input to the circuit by following the same procedure as above.

The CMOS implementation of the 1st bit sum was implemented in Fig1.5 and1.6.

CMOS Implementations for S0:

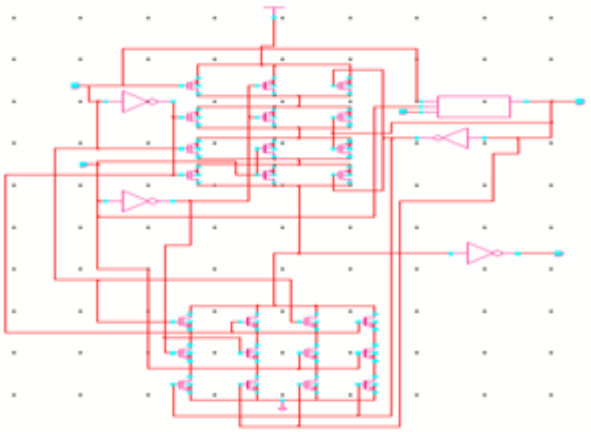

Fig1.5. CMOS Implementation for S0

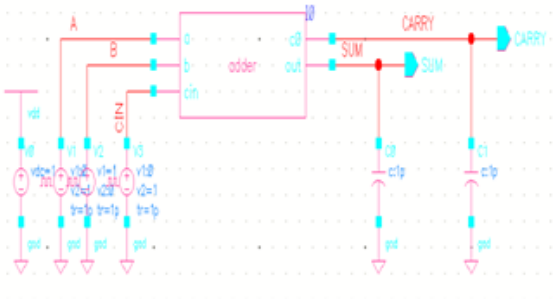

Fig1.6. Symbol Generation of S0

Using the 4-bit adder the 16 bit carry look ahead adder was implemented (Fig 2.1&2.2) and the trans ,Dc response was noted.

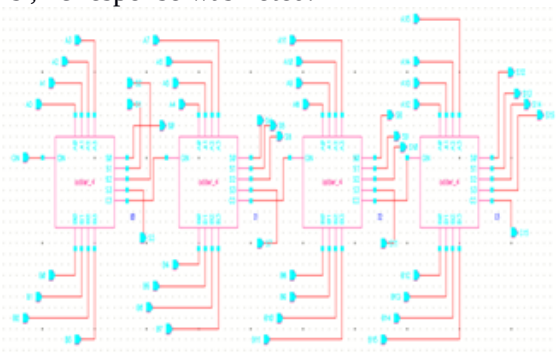

Fig2.1.Implementing 16-bit adder in cadence

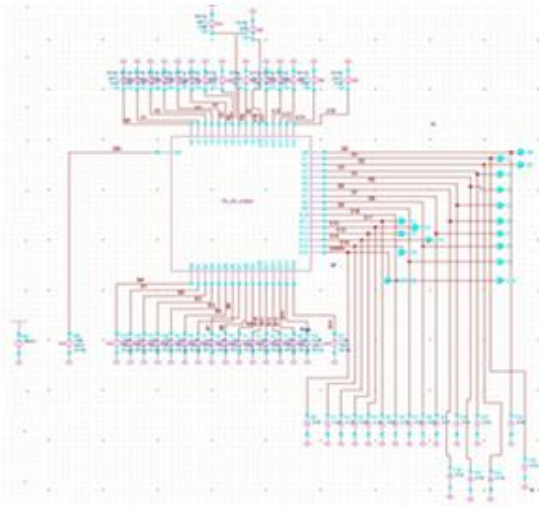

Fig2.2.Symbol generation of 16_bit carry look ahead adder.

RESULT AND DISCUSSIONS

To study the characteristics of carry look ahead adder, the Transient and DC responses are analyzed. The transient response and DC response for the 4-bit adder is shown in Fig.3.2&3.3. Properties for carry look ahead adder and CPU type frequency is given in the form of tabular column. The transient response and DC response for the 16-bit adder is shown in Fig.3.4&3.5.

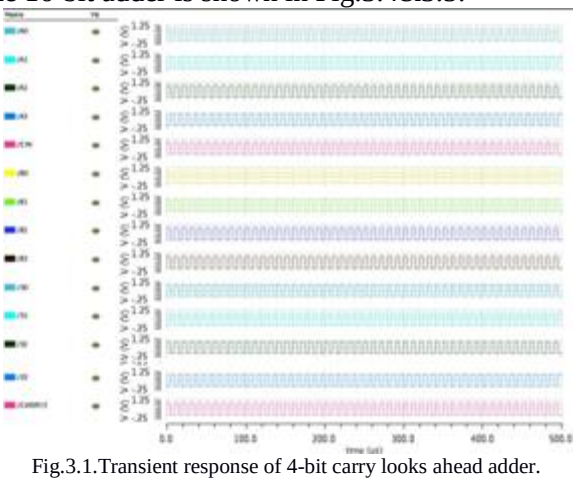

Fig.3.1.Transient response of 4-bit carry looks ahead adder.

The transient response of the 16-bit carry look ahead adder is shown in the Fig.3.3.

The important parametes of the transient response were given below. It will determine how the circuit will act under Non-well performed signals. It could be a giant peak load, a peak change in the input etc ... If original circuit starts oscillating and gets uneven under such conditions, then it is not a good circuit.

PARAMETER	VALUE
Start Time	0s
Stop Time	500us
Step Time	500ns
Max step	5µs
Total time required for trans analysis	418.85s
Peak resident memory used	349Mbytes
Number of accepted trans steps	76635

CPU Type: Intel(R) Core(TM) i7-3770 CPU @3.40GHz

Processor	PhysicalId	CoreId	Frequency
0	0	0	3401.0
1	0	1	3401.0
2	0	2	3401.0
3	0	3	3401.0
4	0	0	3401.0
5	0	1	3401.0
6	0	2	3401.0
7	0	3	3401.0

The DC response of the 4-bit and 16-bit adder was shown in the Fig .3.1.

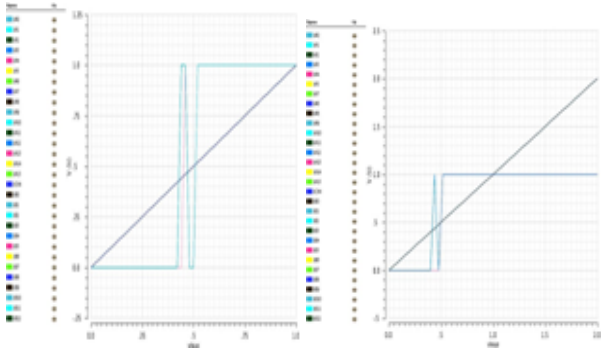

Fig.3.2. Dc response of 16-bit adder and 4-bit adder.

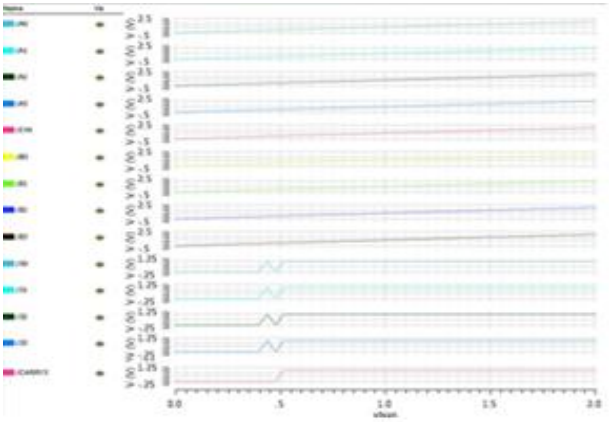

Fig.3.3. Dc response of 4-bit adder.

If it is not possible to use DC analysis to find a DC operating point because of junction problems, then on most simulators transient analysis can be used instead. Even on those simulators that utilize a pseudo-transient analysis in their DC analysis it is still meaningful to try using transient analysis. In the pseudo transient analysis the simulators do not use the capacitors and inductors. Instead they generally install capacitors of range 1F from every node to ground, or across every nonlinear component. The process would be faster only if all capacitors are linear and the equivalent range of the schematic diagram. However, the 1 F capacitors may induce a circuit to fluctuate that would not generally move front and back. In this case, transient analysis is able to find the equilibrium point, where the pseudo-transient is not.

DC Analysis 'DC' : vbias =(0 →2)

PARAMETER	VALUE
Relative total	1e-03
Absolute total(V)	1 uV
Absolute total(I)	1 pA
Temperture(temp)	27c
Tnom	27c
Gmindc	1 ps

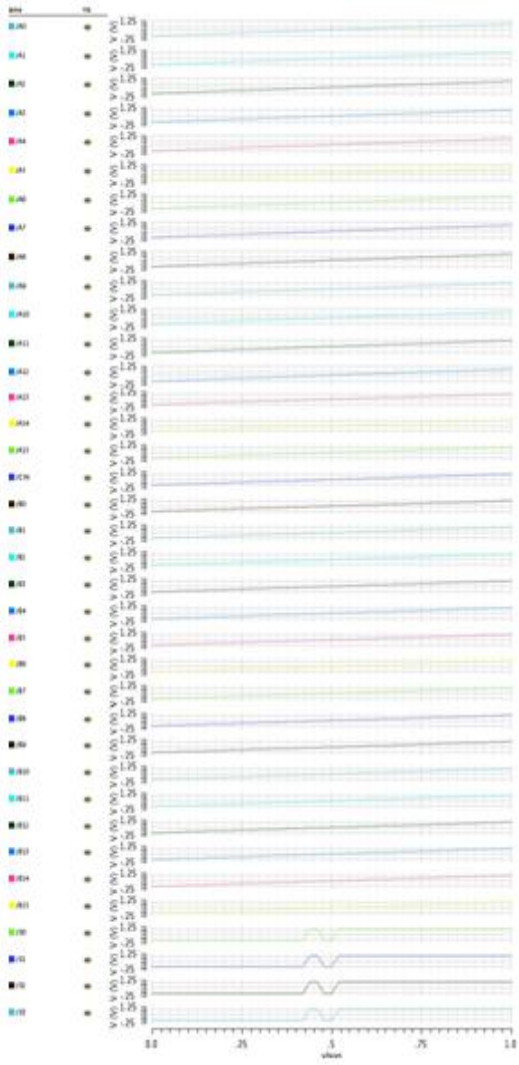

Fig.3.4.Dc response of 16-bit adder.

PARAMETER	VALUE
Start Time	0 s
Stop Time	500 us
Step Time	500 ns
Max step	5 us
Total time required for trans analysis	189.355 s
Peak resident memory used	63.5 Mbytes
Relative total	100e-06
Total time required for DC analysis	7.8868 s
Number of accepted trans steps	34195
Gmin	1 ps
Absolute total (V)	1 uV
Absolute total(I)	1 pA

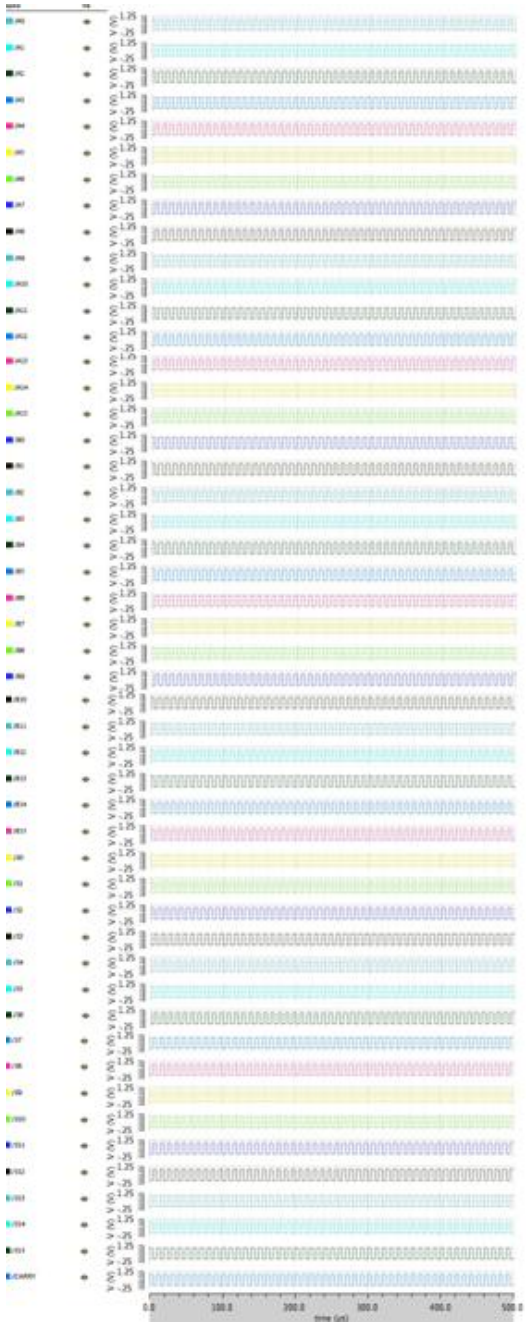

Fig.3.5.Transient response of 16-bit carry looks ahead adder

CONCLUSIONS

The 16-Bit Carry Look Ahead Adder designed using cadence tool which has less delay and less power consumption and memory consumption is very low.Though compared with other different logic design approaches carry look ahead adder employed the great importance to reducing carry propagation delay of the adder. While comparing with Adiabatic logic adder implemented in 180nm CMOS technology but in Cadence adder is implemented in 7 nm technology .The Time required for transient responses CPU =418.85 s elapsed=419.306 s,Peak resident memory=349 Mbytes. Total time required for dc analysis CPU=7.8868s elapsed=7.89968s and Peak Resident Memory=63.5 Mbytes.

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