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Design and Hardware Implementation of L-Type Resonant Step Down DC-DC Converter using Zero Current Switching Technique

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Abstract- **This paper presents the study, analysis, design implementation and simulation of L-type zero current switching (ZCS) resonant buck converter and also practically implemented in hardware. Due to the incorporation of LC based resonant circuit in conventional buck converter the switching losses drastically reduced in high power application. A mathematical calculation were done and implemented the 5W(5V/1A) rated DC-DC resonant ZCS buck converter and simulated using Pspice-Orcad capture software and hardware implemented having IC555 Timer and IRS2110 gate driver circuit for the MOSFET IRFP250.**

Keywords: Hard switching, Soft switching, Zero current Switching (ZCS)

1. INTRODUCTION

Generally DC-DC converters are having electronic devices such as SCR, MOSFET ,IGBT that are used to change DC electrical power efficiently from one voltage level to another. The use of one or more switches for the purpose of power conversion can be regarded as a SMPS. A few applications of DC-DC converters are where 5V DC on a personal computer motherboard must be stepped down to 3V, 2V or less. In all of these applications, we want to change the DC energy from one voltage level to another, while wasting as little as possible in the process. In other words, we want to perform the conversion with the highest possible efficiency.

2. SWITCHING LOSSES

In MOSFETs, the main switching losses are caused by the charging and discharging of the gate-to-source and gate-to-drain parasitic capacitance to turn on and off the device respectively. Figure 2.1 shows the physical representation of these capacitors. The MOSFET parasitic capacitances are given in terms of the device data sheet parameters, and as follows. C_{iss},C_{oss},C_{rss}

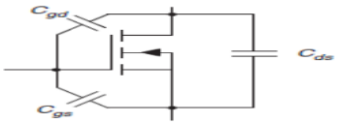

Fig 2.1: MOSFET with junction capacitance

$C_{gd}=C_{rss}$

$C_{gs}=C_{iss}- C_{rss}$

$C_{ds}=C_{oss}- C_{rss}$

where C_{rss} = small-signal reverse transfer capacitance.

C_{iss} = small-signal input capacitance with the drain and source terminals are shorted.

C_{oss} = small-signal output capacitance with the gate and source terminals are shorted.

A converter basically consists of an array of on–off electronic switches that use power semiconductor devices. If the switches are considered ideal or lossless (zero conduction
drop, zero leakage current, and instantaneous turn-on and turn-off times), the instantaneous and average power will balance at input and output of the converter. Switching mode operation makes the converter nonlinear, thus generating source and load harmonics and also EMI problems.
In Hard-Switching Topologies shown in fig2.2 a real semiconductor switch, the switch voltage or switch current do not go to zero instantaneously at the instant of turn-on or turn-off. The large overlap between the voltage and current waves during switching creates a large switching loss, thus reducing the efficiency of the converters. As the switching frequency increases the losses are increased drastically in high power applications. Turning on and turning off the power electronic switches with switching losses is known as “hard switching”.

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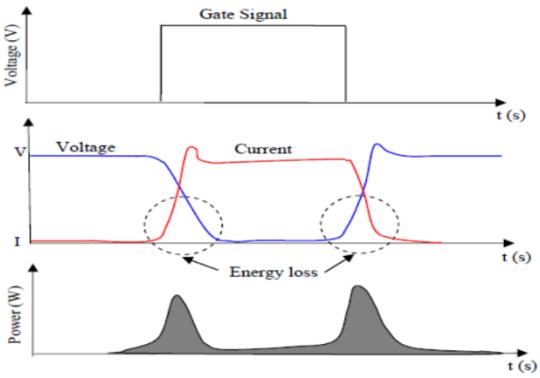

Fig2.2: Loss of power during hard-switching

In Soft-Switching Topologies, The main idea in soft switching is to prevent or minimize the switching overlap so that the switching loss is minimal. Soft switching techniques force the voltage or current to be zero during the time of transition; therefore there is no overlap between voltage and current and (ideally) no switching loss. Hence, the problem of switching losses and EMI due to hard switching converter operation is overcome by using soft switching. There are two types of soft switching which are zero-voltage switching (ZVS) and zero-current switching (ZCS). There are many ZVS and ZCS techniques have been published. The selection of switching technique is important when dealing with high power converter.

Figure2.3 shows the switching transient of the switch in a soft-switched circuit and it shows the switching losses are decreased with high amount.

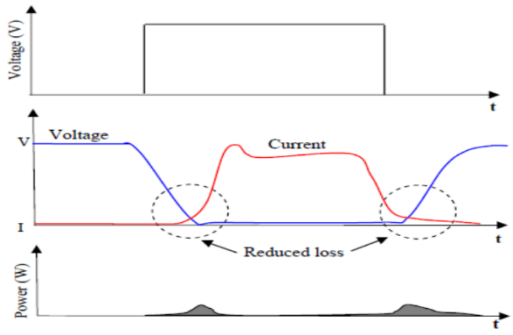

Fig2.3: Loss of power during soft-switching

3. L-TYPE ZCS RESONANT CONVERTER MODES OPERATION AND WAVEFORMS

An L-type ZCS resonant converter is shown above figure.3.1 The switching device S in the figure can be GTO, Thyristor, BJT, power MOSFET or IGBT. At low kilohertz range; GTO, thyristor or IGBT is used whereas for megahertz range; power MOSFETs are preferred. Inductor L and capacitance C near the dc source V_s from the resonant circuit whereas L_1, C_1 near the load constitute a filter circuit. Direction of currents and polarities of voltages as marked in figure are treated as positive.

The circuit of figure is initially in the steady state with constant load current I_0. Filter inductor L_1 is relatively large to assume that current i_0 in L_1 is almost constant at I_0. Initially switch S is open; resonant circuit parameters have $i_L = 0$ in L and $V_c = 0$ across C and the load current i_0 freewheels through the diode D.

For the sake of convenience working of this converter is divided into five modes as under. For all these modes, time t is taken as zero at the beginning of each mode.

Mode-1 ($0 \leq t \leq t_1$):

At t=0, switch S is turned on. As I_0 is freewheeling through diode D, voltage across ideal diode $v_D = 0$ and also $v_C = 0$, fig.3.1(mode-1). it implies that source voltage V_s gets applied across L and the switch current i_L begins to flow through V_s, switch S, L and diode D. Therefore, $V_s = L\, d_i/d_t$. It gives $i_L = \frac{V_s}{L} t$. It shows that inductor or switch current i_L rises linearly from its zero initial value. The diode current i_D is given by

$$i_D = I_0 - i_L = I_0 - \frac{V_s}{L} t$$

$$\text{At } t = t_1,$$

$$i_L = \frac{V_s}{L} . t_1 = I_0.$$

This gives $t_1 = \frac{I_0 \cdot L}{V_s}$

Also, at $t = t_1, i_D = I_0 - I_0 = 0$. Soon after $t_1, as\ i_D$ tends to reverse, diode D gets turned off. As a result of this, short circuit across C is removed.

Mode 2 ($0 \leq t \leq t_2$):

Switch S remains on. As D turns off at t= 0, current I_0 flows through V_s, L, L_1 and R. In fig.3.1(mode-1) and (mode-2), constant current through L_1 and R is represented by current source I_0. Also a current i_C begins to build up through resonant circuit consisting of V_s, L and C in series. Inductor current i_L is, therefore, given by

$$i_L = I_0 + i_C = I_0 + I_m \sin \omega_0 t$$

Where $I_m = V_S \sqrt{\frac{C}{L}} = \frac{V_s}{Z_0}$ and $\omega_0 = \frac{1}{\sqrt{LC}}$. Here $Z_0 = \sqrt{\frac{L}{C}}$ is the characteristic impedence of resonant circuit.

The capacitor current is $i_C = I_m \sin \omega_0 t$ and capacitor voltage V_c is given by

$$v_c(t) = V_s(1 - \cos \omega_0 t)$$

The peak value of current i_L is $I_p = I_0 + I_m$ and it occurs at $t = \frac{\pi}{2\omega_0} = \frac{\pi}{2}\sqrt{LC}$. At this instant, $v_c = V_s \left[1 - \cos \frac{\pi}{2}\right] = V_s\ and\ i_c = I_m$.

When $t = t_2 = \frac{\pi}{\omega_0} = \pi\sqrt{LC}$, capacitor voltage reaches peak value $V_{cp} = V_s[1 - \cos \pi] = 2V_s\ and\ i_c = 0$.

Also, at $t = t_2, i_L = I_0, i.e,$ switch current drops from peak value $(I_0 + I_m)$ to I_0.

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Mode 3 ($0 \leq t \leq t_3$):

Switch S remains on. At t= 0, capacitor voltage is $2V_s$. As i_c tends to reverse at t = 0, capacitor begins to discharge and force a current

$i_c = V_s\sqrt{\frac{C}{L}}\ \sin\omega_0 t$ opposite to i_L, fig.3.1.(mode-3) so that inductor or device current i_L is given by

$$i_L = I_0 - i_c = I_0 - I_m \sin\omega_0 t$$

And capacitor voltage $v_c = 2V_s \cos\omega_0 t$. Current i_L falls to zero

when t= t_3,

$$\text{i.e., } i_L = 0 = I_0 - I_m \sin\omega_0 t_3$$

Or $t_3 = \sqrt{LC}\sin^{-1} I_0/I_m$

At t= t_3, $v_c =$

$2V_s \cos\omega_0 t_3 = 2V_s\left[\frac{\sqrt{{I_m}^2-{I_0}^2}}{I_m}\right] = V_{c3}$ During this mode, $i_c = I_m \sin\omega_o t$ and as i_L falls to zero at t_3, switching device S gets turned off. Note that current i_c in this mode flows opposite to its positive direction, it is therefore shown negative in fig3.1(mode-3) At t= t_3, the value of $i_c = -I_0$.

Mode 4 ($0 \leq t \leq t_4$):

As switch S is turned off at t= 0, capacitor begins to supply the load current I_0 as shown in fig3.1.(mode-4). Capacitor voltage at any time t is given by

$$v_c = V_{c3} - \frac{1}{C}\int i_c.d_t$$

As magnitude of capacitor current $i_c = i_0$ is constant,

$$v_c = V_{c3} - \frac{I_0}{C}t$$

This mode comes to an end when v_c falls to zero at t= t_4.

or $V_{c3} - \frac{I_0}{C}t_4 = 0$

or $t_4 = \frac{C.V_{C3}}{I_0}$

At t=0, $v_T = V_s - V_{c3}$ and at t= t_4, $v_T = V_s - 0 = V_s$ as shown in fig3.1(mode-4).As I_o is constant, capacitor discharges linearly from V_{c3} to zero and v_T varies linearly from ($V_s - V_{c3}$) to V_s as shown in fig.3.1

Mode 5 ($0 \leq t \leq t_5$):

At the end of mode 4 or in the beginning of mode 5, capacitor voltage v_c is zero as shown in fig.3.1 waveforms. As v_c tends to reverse at t=0, diode D_m gets forward biased and starts conducting, fig.b.(mode-5). The load current I_o flows through diode D_m so that $I_{D_m} = I_o$ during this mode.

This mode comes to an end when switch S_1 is again turned on at t=t_5. The cycle is now repeated as before. Here $t_5 = T - (t_1 + t_2 + t_3 + t_4)$.

The waveforms for switch or inductor current i_L, capacitor voltage v_c, diode current I_{D_m}, capacitor current i_c and voltage across switch S_1 as v_T are shown in fig.3.1 waveforms. It is seen that at turn-on at t=0 ($0 \leq t \leq t_1$), switch current i_L=0, therefore switching loss $v_T i_L = 0$. Similarly, at turn-off at t_3($0 \leq t \leq t_3$), i_L=0 and therefore $v_T i_L = 0$. It shows that the switching loss during turn-on and turn-off processes is almost zero. The peak resonant current $I_m = \frac{V_S}{Z_0}$ must be more than the load current I_o, otherwise switch current i_L will not fall to zero and switch S_1 will not get turned off.

The load voltage v_0 can be regulated by varying the period t_5. It is obvious that longer the period t_5, lower is the load voltage.

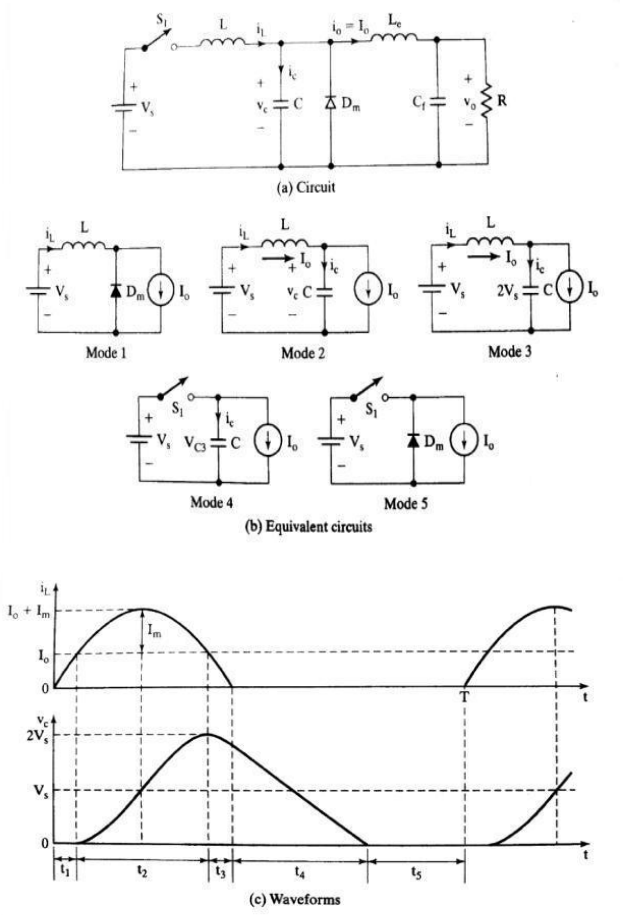

Figure 3.1: L - Type ZCS Resonant Converter circuit , modes of Operation and waveforms

4. DESIGN OF CONVERTER

Design example: To verify the operation and performance of the proposed converter, a 5W (5V*1A) experimental prototype circuit was built for battery charging application. A design procedure for 5-W converter is presented. The specifications are as follows:

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V_{in} = 12 V

V_{out} = 5 V

I_{out} = 1 A

The selection of the resonant inductor and capacitor is determined by the need to satisfy the relation

$$\frac{V_{in}}{Z_C} > I_{out}$$

Where, $Z_c = \sqrt{L_r/C_r}$

So keeping these things in mind value chosen are:

$C_r = C_d = 0.2$ micro farad

$L_r = L_1 = 20$ micro Henry

According to the relation given modes of operation, as the transistor turn on, causing current to ramp at

$d_i/d_t = \frac{12}{20} * 10\text{^}6 = 0.6 * 10^6$ A/s

So the diode current will be zero in micro seconds after the transistor turn on, then the circuit enters into mode 2.

$Z_c = \sqrt{L_r/C_r} = \sqrt{20/0.2} = 10\ \Omega$

$(it\ is\ also\ called\ characterstic\ impedence)$

According to relation given in modes of operation,

$I_{out} = V_{in}/Z_c = 12/10 = 1.2\ A$

This show

$V_{in}/Z_c > I_{out}$. So the resonant condition gets fulfilled.

However if the load increases above 1.2 A, this LC combination will no longer support soft switching.

$W_r = 1/\sqrt{LC} = 500000$ rad/sec

$f_r = W_r/2\pi = 79.577$ kHz

From the relation

$W_r t_{off} = 56.4426$

$I_L(t)$ will be zero at 180.0001 (in degree) and 359.999 (in degree).corresponding time can be calculated as

$t_{off1} = 180.0001 * \frac{\pi}{180} * 500000 = 6.28\ \mu s$

$t_{off2} = 359.99 * \pi/180 * 500000 = 12.6\ \mu s$

So MOSFET gate signal should be held high until (µs).And it should be turn off before t_{off2} is reached. The gate signal of 10.6 µs will work nice in the case.

The second integral is the area of a triangle. The triangle peak value is given by

$V_d(t_{off2}) = 12(1 - \cos(303.6)) = 5.36V$

The time until V_d reaches zero is:

$t = V_d(t_{off2})/(I_{out}/C_d) = 5.36 \div (\frac{1}{0.2\times10^{-6}}) = 1.072\ \mu s$

ΔArea= $(0.2*5.36^2)/(2*1) = 2.87*10^{-6}$ Vs

From (i)

$$\left[\int_0^{t_{off2}} V_{in}(1 - \cos(W_r t))dt\right]$$

$= 12[10.6 + 0.0923] * 10^{-6}$

$= 1.47*10^{-4}\ Vs$

So the average output voltage is

$< V_d >= (1.47 * 10^{-4} + 2.87 * 10^{-6})/T$

Since the desired output is 5V then:

$5 = (1.47 * 10^{-4} + 2.87 * 10^{-6})/T$

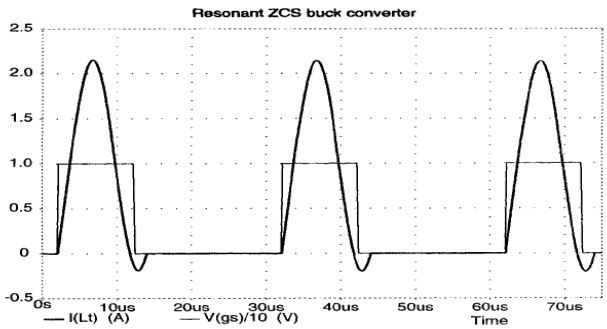
$T = 29.97\ \mu s \cong 30\mu s$

So from above we get f ≅ 33.33 kHz in ideal condition. But in practical case we have to take care the drop across the diode also over the period of time which is around 1.5 V during turn on time of diode.

6T=(147+2.87)-1.5(T-33.53)

[33.53 is the off time of diode]

Which gives T ≅ 30.79 µs and frequency = 32.478 kHz By taking other no ideality in MOSFET, inductor, capacitor practical switching frequency is coming around 36.6 kHz.



The proposed ZCS buck converter for USB power adapter 5V, 1A is presented. The converter features were listed in Table1

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Input voltage	12V
Output voltage	5V
Output current	1A
Switching frequency	33.33 kHz
Duty cycle	0.333 or 33.33%
Resonant inductor	20uH
Resonant capacitor	0.2 uF
Output filter induct	2.0mH
Filter capacitor	20uF
Load resistor	5 ohms

5. SIMULATION AND HARDWARE RESULTS

The above Proposed and designed converter is Simulated using PSpice-Orcad Capture Software and observed the results i.e. Current through the resonant inductor and voltage across resonant capacitor and MOSFET gate triggered pulses and output voltage

5.1 Pspice circuit diagram

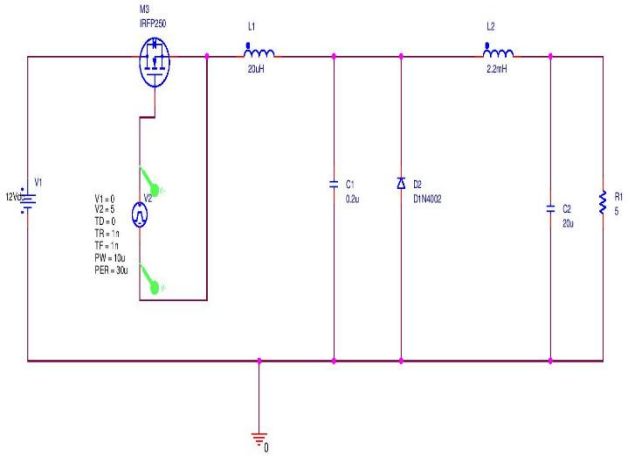

Fig5.1: Pspice model of ZCS buck converter

Simulated Results

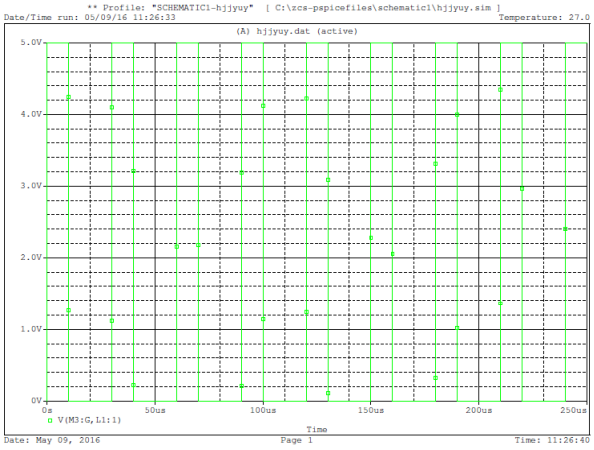

Fig5.2: Pulses to the MOSFET

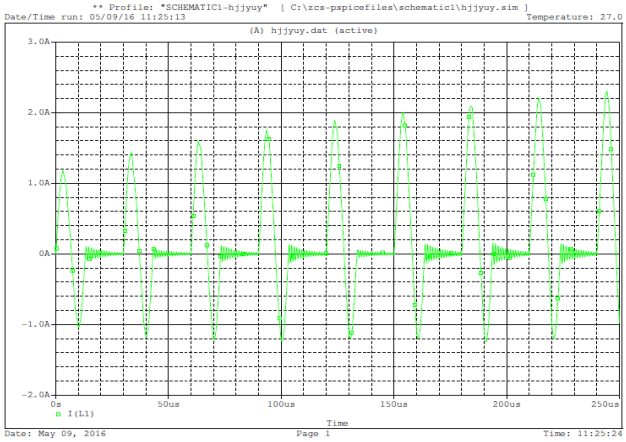

Fig5.3: Current through the resonant inductor

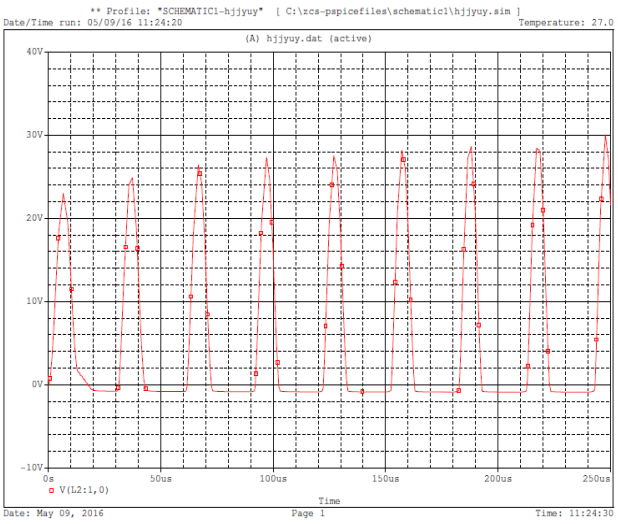

Fig5.4: Voltage across the resonant capacitor

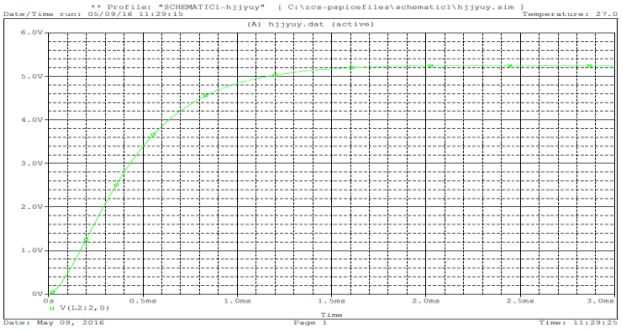

Fig5.5: Voltage across the output terminal

6. EXPERIMENTAL RESULTS

5W (5V/1.0A) prototype of the ZCS converter, as shown in Fig.5.1 is built to verify the theory. And the result is compared with simulation. The specifications of the experimental prototype is as follows: Input voltage = 12V, Output voltage = 5V, output current = 1.0Amps

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Circuit parameters of the proposed converter are as follows.

1) Switch: MOSFET IRFP250.
2) Diode: IN4001.
3) Resonant capacitor: 0.2 uF.
4) Filter capacitor: 20uF.
5) Resonant inductor: 20uH.
6) Output filter inductor: 2.0mH.
7) Load resistor 5 ohms

In experimental setup we can generate triggering pulses to drive the MOSFET by using 555 timer. Here we generated 7.76 V as a gate pulse from the timer. This pulse input is not enough to drive the Mosfet IRFP250. Hence we have to amplify the signal beyond 10 volts. Because the minimum voltage required to drive the MOSFET is to be 10 volts. To amplify this signal we are using MOSFET driver IRS2110.Now we have the pulse with the amplitude of 15.6 volts. This voltage is enough to drive our MOSFET IRFP250.

After applying this gate pulse we observe the corresponding waveforms comparing with the simulation results.

IC555 Timer

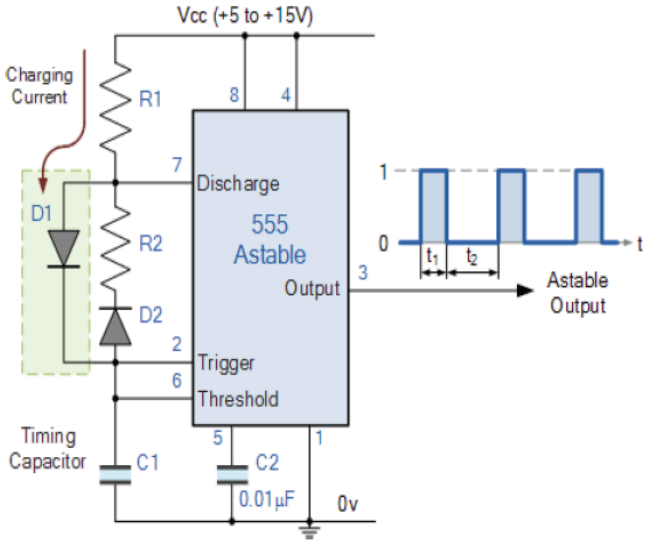

Fig6.1: Pin configuration of 555 Timer

The R_1 and R_2 resistors of 555 Timer are calculated as below

$$T_{on} = 0.693 R_1 C_1$$

$$R_1 = \frac{T_{on}}{0.693 C_1}$$

The On period T_{on}=10 micro seconds and C_1=1 nano farads

Then the value R_1=14.4K ohm

$$Toff = 0.693 R_2 C_1$$

$$R_2 = \frac{Toff}{0.693 C_1}$$

The On period Toff=20 micro seconds and C_1=1 nano farads

Then the value R_2=28.9K ohm

The resultant 555 timer configuration is given below

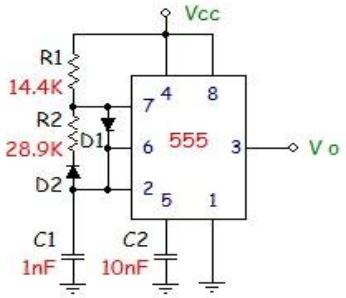

Fig6.2: circuit configuration of 555 Timer

IRS2110 Gate Driver Circuit

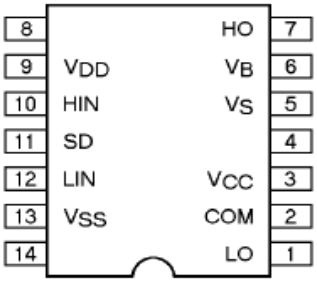

Fig6.3: Pin configuration of IRS2110

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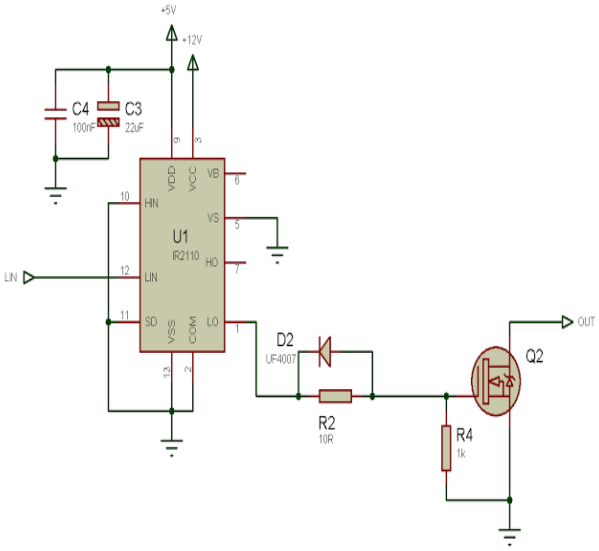

Fig6.4: IRS2110 as a low side MOSFET driver

5.3.3 Experimental Setup and Results

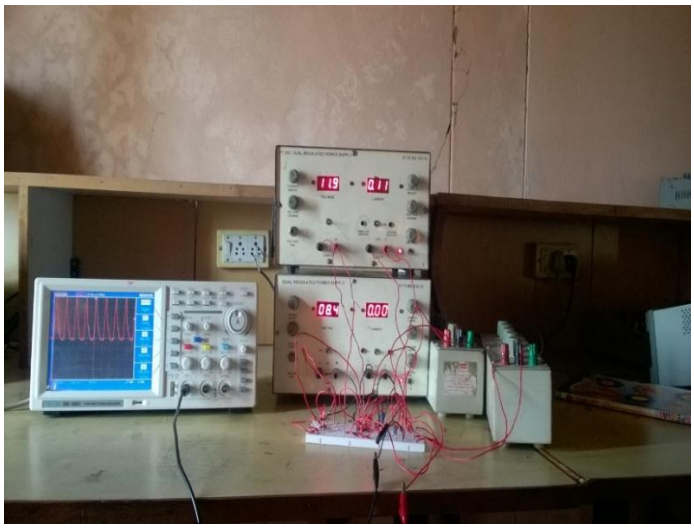

Fig6.5: Hardware circuit of L-type ZCS resonant buck converter

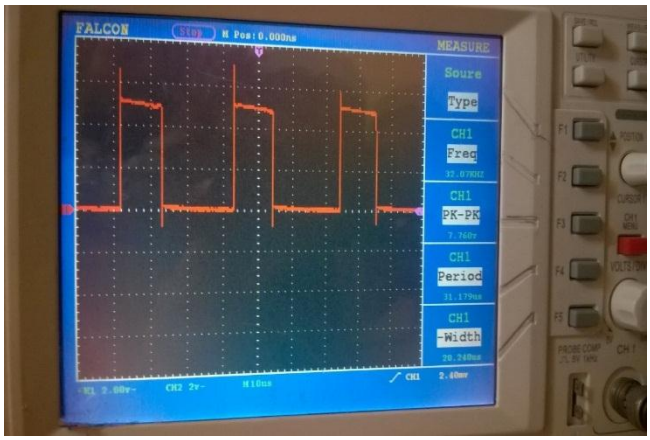

Fig6.6: Pulses from the 555 Timer

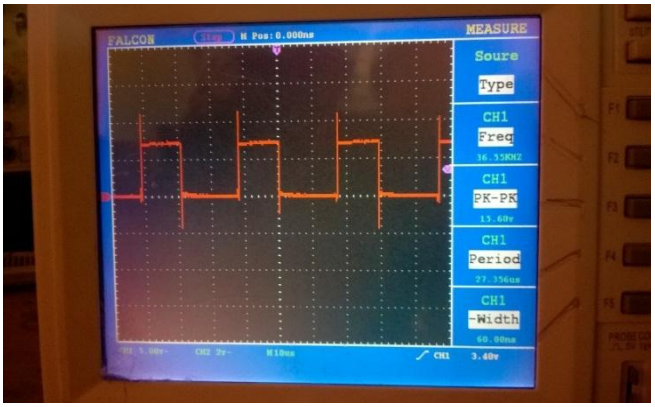

Fig6.7: Pulses from the IRS2110

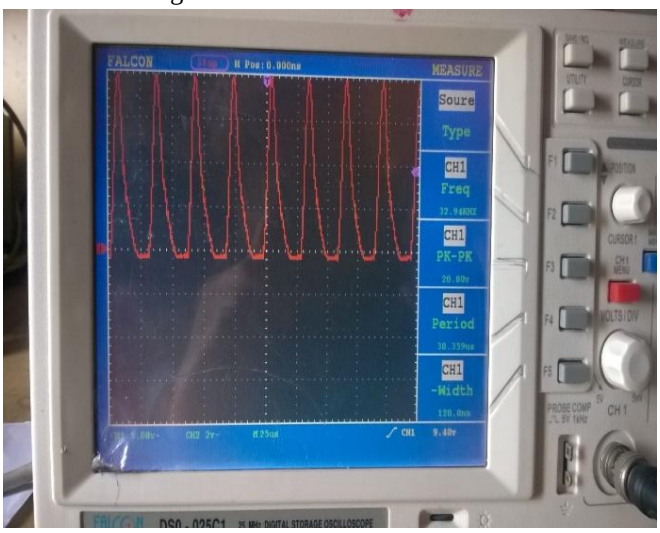

Fig6.8: Voltage across resonant capacitor

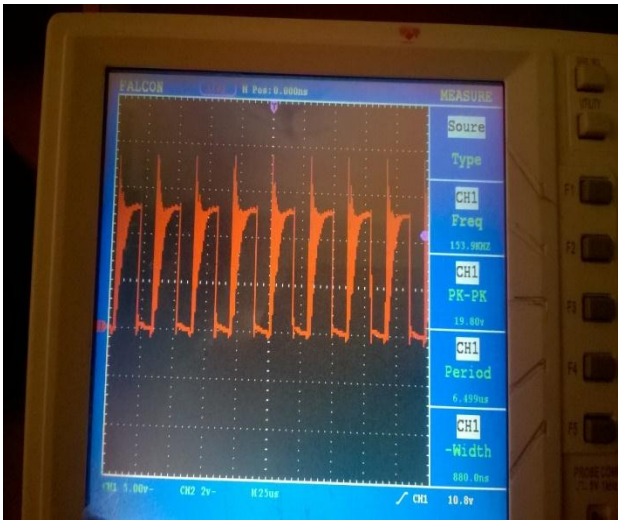

Fig6.9: Voltage across MOSFET IRFP250

7. CONCLUSION

In this paper we analyse, design and implemented the ZCS based 5W(5V/1A) resonant DC-DC buck converter. The various modes of operation of L-type ZCS resonant converter and time analysis of the resonant capacitor voltage and resonant inductor current waveforms analyzed. The ZCS resonant convetrter is simulated using

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Pspice-Orcad capture software and also implemented the experimental(hardware) proto type. In hardware implementation the required pulses are generated by IC555 Timer and amplified by IRS2110 i.e used for switching the MOSFET IRFP250. The simulated results resonant capacitor voltage, resonant inductor current and output voltage executed successfully are compared with the hardware results and also compared with the theoretical waveforms. At final we concluded that in high power applications the switching losses are reduced drastically due to incorporation of LC based resonant circuit in conventional buck converter and improved the performance and efficiency of the converter.

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