Design and Hardware Implementation of L-Type Resonant Step Down DC-DC Converter using Zero Current Switching Technique

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Abstract- This paper presents the study, analysis, design implementation and simulation of L-type zero current switching (ZCS) resonant buck converter and also practically implemented in hardware. Due to the incorporation of LC based resonant circuit in conventional buck converter the switching losses drastically reduced in high power application. A mathematical calculation were done and implemented the 5W(5V/1A) rated DC-DC resonant ZCS buck converter and simulated using Pspice-Orcad capture software and hardware implemented having IC555 Timer and IRS2110 gate driver circuit for the MOSFET IRFP250.

Keywords: Hard switching, Soft switching, Zero current Switching (ZCS)

1. INTRODUCTION

Generally DC-DC converters are having electronic devices such as SCR, MOSFET ,IGBT that are used to change DC electrical power efficiently from one voltage level to another. The use of one or more switches for the purpose of power conversion can be regarded as a SMPS. A few applications of DC-DC converters are where 5V DC on a personal computer motherboard must be stepped down to 3V, 2V or less. In all of these applications, we want to change the DC energy from one voltage level to another, while wasting as little as possible in the process. In other words, we want to perform the conversion with the highest possible efficiency.

2. SWITCHING LOSSES

In MOSFETs, the main switching losses are caused by the charging and discharging of the gate-to-source and gate-to-drain parasitic capacitance to turn on and off the device respectively. Figure 2.1 shows the physical representation of these capacitors. The MOSFET parasitic capacitances are given in terms of the device data sheet parameters, and as follows. Ciss,Coss,Crss

\[ C_{gd} = C_{iss} \]
\[ C_{gs} = C_{iss} - C_{rss} \]
\[ C_{ds} = C_{oss} - C_{rss} \]

where \( C_{iss} \) = small-signal reverse transfer capacitance.
\( C_{oss} \) = small-signal output capacitance with the gate and source terminals are shorted.
\( C_{rss} \) = small-signal input capacitance with the drain and source terminals are shorted.

A converter basically consists of an array of on-off electronic switches that use power semiconductor devices. If the switches are considered ideal or lossless (zero conduction drop, zero leakage current, and instantaneous turn-on and turn-off times), the instantaneous and average power will balance at input and output of the converter. Switching mode operation makes the converter nonlinear, thus generating source and load harmonics and also EMI problems.

In Hard-Switching Topologies shown in fig2.2 a real semiconductor switch, the switch voltage or switch current do not go to zero instantaneously at the instant of turn-on or turn-off. The large overlap between the voltage and current waves during switching creates a large switching loss, thus reducing the efficiency of the converters. As the switching frequency increases the losses are increased drastically in high power applications. Turning on and turning off the power electronic switches with switching losses is known as “hard switching”.

Fig 2.1: MOSFET with junction capacitance
In Soft-Switching Topologies, the main idea in soft switching is to prevent or minimize the switching overlap so that the switching loss is minimal. Soft switching techniques force the voltage or current to be zero during the time of transition; therefore there is no overlap between voltage and current and (ideally) no switching loss. Hence, the problem of switching losses and EMI due to hard switching converter operation is overcome by using soft switching. There are two types of soft switching which are zero-voltage switching (ZVS) and zero-current switching (ZCS). There are many ZVS and ZCS techniques have been published. The selection of switching technique is important when dealing with high power converter.

Figure 2.3 shows the switching transient of the switch in a soft-switched circuit and it shows the switching losses are decreased with high amount.

3. L-TYPE ZCS RESONANT CONVERTER MODES

OPERATION AND WAVEFORMS

An L-type ZCS resonant converter is shown above figure 2.1. The switching device S in the figure can be GTO, Thyristor, BJT, power MOSFET or IGBT. At low kilohertz range; GTO, thyristor or IGBT is used whereas for megahertz range; power MOSFETs are preferred. Inductor L and capacitance C near the dc source V_s from the resonant circuit whereas L_1, C_1 near the load constitute a filter circuit. Direction of currents and polarities of voltages as marked in figure are treated as positive.

The circuit of figure is initially in the steady state with constant load current I_0. Filter inductor L_1 is relatively large to assume that current i_s in L_1 is almost constant at I_0. Initially switch S is open; resonant circuit parameters have i_s = 0 in L and V_C = 0 across C and the load current i_o freewheels through the diode D.

For the sake of convenience working of this converter is divided into five modes as under. For all these modes, time t is taken as zero at the beginning of each mode.

Mode-1 (0 ≤ t ≤ t_1):

At t=0, switch S is turned on. As I_0 is freewheeling through diode D, voltage across ideal diode V_D = 0 and also V_c = 0, fig.3.1 (mode-1). It implies that source voltage V_s gets applied across L when the switch current i_s begins to flow through V_s, switch S, L and diode D. Therefore, V_s = L_1 d_i_s / d_t. It gives i_s = V_s / L_1 t. It shows that inductor or switch current i_s rises linearly from its zero initial value.

The diode current i_d is given by

$$i_d = i_o - i_l = i_0 - \frac{V_S}{L} t$$

At t = t_1,

$$i_l = \frac{V_s}{L} t_1 = i_0.$$  

This gives

$$t_1 = \frac{i_0 - L}{V_s}.$$  

Also, at t = t_1, i_d = i_0 - i_o = 0. Soon after t_1, as i_d tends to reverse, diode D gets turned off. As a result of this, short circuit across C is removed.

Mode 2 (0 ≤ t ≤ t_2):

Switch S remains on. As D turns off at t=0, current I_0 flows through V_s, L_1 and R. In fig.3.1 (mode-1) and (mode-2), constant current through L_1 and R is represented by current source I_o. Also a current i_c begins to build up through resonant circuit consisting of V_s, L and C in series. Inductor current i_s is, therefore, given by

$$i_s = i_0 + i_c = i_0 + i_m \sin \omega_0 t$$

Where

$$I_m = V_S \sqrt{\frac{L}{C}} = \frac{V_s}{Z_0}$$

and

$$\omega_0 = \frac{1}{\sqrt{LC}}.$$  

Here Z_0 = \sqrt{L/C} is the characteristic impedance of resonant circuit.

The capacitor current is

$$i_c = I_m \sin \omega_0 t$$  

and capacitor voltage V_c is given by

$$V_c(t) = V_s(1 - \cos \omega_0 t).$$

The peak value of current i_c is I_p = I_0 + I_m and it occurs at

$$t = \frac{\pi}{2 \omega_0}.$$  

At this instant, V_c =

$$V_s \left[ 1 - \cos \frac{\pi}{2} \right] = V_s \ \text{and} \ i_c = I_m.$$  

When

$$t = \frac{\pi}{\omega_0},$$

the capacitor voltage reaches peak value V_cp = V_s(1 - \cos m). Also, at

$$t = t_2, \ i_L = I_o, \ i.e., \ \text{switch current drops from peak value (I_0 + I_m) to I_o.}$$
Mode 3 (0≤t≤t₃):

Switch S remains on. At t=0, capacitor voltage is 2Vₛ. As i_c tends to reverse at t = 0, capacitor begins to discharge and force a current

\[ i_c = Vₛ \frac{C}{L} \sin \omega_0 t \]

opposite to i_L, fig.3.1.(mode-3) so that inductor or device current i_L is given by

\[ i_L = I₀ - i_c = I₀ - Iₘ \sin \omega_0 t \]

And capacitor voltage \( v_c = 2Vₛ \cos \omega_0 t \). Current \( i_L \) falls to zero when \( t = t₃ \).

\[ i_c = Iₘ \sin \omega_0 t \]

\[ v_c = \frac{1}{C} \int i_c \, dt \]

Or

\[ t₃ = \sqrt{\frac{C}{L}} \sin^{-1} \left( \frac{I₀ - Iₘ \sin \omega_0 t₃}{Iₘ} \right) \]

During this mode, \( i_c = Iₘ \sin \omega_0 t \) and as \( i_L \) falls to zero at \( t₃ \), switching device S gets turned off. Note that current \( i_c \) in this mode flows opposite to its positive direction, it is therefore shown negative in fig.3.1.(mode-3) At \( t = t₃ \), the value of \( i_c = -I₀ \).

Mode 4 (0≤t≤t₄):

As switch S is turned off at \( t = 0 \), capacitor begins to supply the load current \( I₀ \) as shown in fig.3.1.(mode-4). Capacitor voltage at any time \( t \) is given by

\[ v_c = Vₛ - \frac{1}{C} \int i_c \, dt \]

As magnitude of capacitor current \( i_c = i₀ \) is constant,

\[ v_c = Vₘ - \frac{i₀}{C} \int \]

This mode comes to an end when \( v_c \) falls to zero at \( t = t₄ \). or

\[ Vₘ - \frac{i₀}{C} \leq 0 \]

\[ t₄ = \frac{CVₘ}{i₀} \]

At \( t₀ \), \( V_T = Vₛ - Vₘ \) and at \( t = t₄ \), \( V_T = Vₛ - Vₘ = 0 \) as shown in fig.3.1.(mode-4). As \( I₀ \) is constant, capacitor discharges linearly from \( Vₘ \) to \( Vₛ \) and \( V_T \) varies linearly from \( Vₛ - Vₘ \) to \( Vₛ \) as shown in fig.3.1.

Mode 5 (0≤t≤t₅):

At the end of mode 4 or in the beginning of mode 5, capacitor voltage \( v_c \) is zero as shown in fig.3.1 waveforms. As \( v_T \) tends to reverse at \( t=0 \), diode \( Dₘ \) gets forward biased and starts conducting, fig. b.(mode-5). The load current \( I₀ \) flows through diode \( Dₘ \) so that \( Iᵢₘ = I₀ \) during this mode.

This mode comes to an end when switch \( S₁ \) is again turned on at \( t = t₅ \). The cycle is now repeated as before. Here \( t₅ = T - (t₁ + t₂ + t₃ + t₄) \).

The waveforms for switch or inductor current \( iₘ \), capacitor voltage \( v_c \), diode current \( iₚₘ \), capacitor current \( i_c \) and voltage across switch \( S₁ \) as \( V_T \) are shown in fig.3.1 waveforms. It is seen that at turn-on at \( t=0 \) (0≤t≤t₁), switch current \( i_c = 0 \), therefore switching loss \( V_Ti_c = 0 \). Similarly, at turn-off at \( t₃ \), \( i_c = 0 \) and therefore \( V_Ti_c = 0 \). It shows that the switching loss during turn-on and turn-off processes is almost zero. The peak resonant current \( Iₘ \) must be more than the load current \( I₀ \), otherwise switch current \( iₘ \) will not fall to zero and switch \( S₁ \) will not get turned off.

The load voltage \( Vₘ \) can be regulated by varying the period \( t₅ \). It is obvious that longer the period \( t₅ \), lower is the load voltage.

**4. DESIGN OF CONVERTER**

*Design example:* To verify the operation and performance of the proposed converter, a 5W (5V*1A) experimental prototype circuit was built for battery charging application. A design procedure for 5-W converter is presented. The specifications are as follows:
\[ V_{in} = 12 \text{ V} \]
\[ V_{out} = 5 \text{ V} \]
\[ I_{out} = 1 \text{ A} \]

The selection of the resonant inductor and capacitor is determined by the need to satisfy the relation
\[ \frac{V_{in}}{Z_c} > I_{out} \]

Where, \( Z_c = \sqrt{L_r/C_r} \)

So keeping these things in mind value chosen are:
\[ C_r = C_d = 0.2 \text{ micro farad} \]
\[ L_r = L_1 = 20 \text{ micro Henry} \]

According to the relation given modes of operation, as the transistor turn on, causing current to ramp at
\[ \frac{d_i}{dt} = \frac{12}{20} \times 10^6 = 0.6 \times 10^6 \text{ A/s} \]

So the diode current will be zero in micro seconds after the transistor turn on, then the circuit enters into mode 2.
\[ Z_c = \sqrt{L_r/C_r} = \sqrt{20/0.2} = 10 \Omega \]

(it is also called characteristic impedance)

According to relation given in modes of operation,
\[ I_{out} = \frac{V_{in}}{Z_c} = 12/10 = 1.2 \text{ A} \]

This show
\[ \frac{V_{in}}{Z_c} > I_{out}. \] So the resonant condition gets fulfilled.

However if the load increases above 1.2 A, this LC combination will no longer support soft switching.
\[ W_r = \frac{1}{\sqrt{LC}} = 500000 \text{ rad/sec} \]
\[ f_r = \frac{W_r}{2\pi} = 79.577 \text{ kHz} \]

So MOSFET gate signal should be held high until (\( \mu s \)). And it should be turn off before \( t_{off2} \) is reached. The gate signal of 10.6 \( \mu s \) will work nice in the case.

The second integral is the area of a triangle. The triangle peak value is given by
\[ V_d(t_{off2}) = 12(1 - \cos(303.6)) = 5.36V \]

The time until \( V_d \) reaches zero is:
\[ t = \frac{V_d(t_{off2})}{(I_{out}/C_d)} = 5.36 + \left( \frac{1}{0.2 \times 10^6} \right) = 1.072 \mu s \]

\[ \Delta \text{Area} = (0.2 \times 5.36^2)/(2 \times 1) = 2.87 \times 10^{-6} \text{ Vs} \]

From (i)
\[ \int_{0}^{\Delta t} V_{in}(1 - \cos(W_r t))dt \]
\[ = 12[10.6 + 0.0923] \times 10^{-6} \]
\[ = 1.47 \times 10^{-4} \text{ V}s \]

So the average output voltage is
\[ < V_d > = (1.47 \times 10^{-4} + 2.87 \times 10^{-6})/T \]

Since the desired output is 5V then:
\[ 5 = (1.47 \times 10^{-4} + 2.87 \times 10^{-6})/T \]
\[ T = 29.97 \mu s \approx 30 \mu s \]

So from above we get \( f \approx 33.33 \text{ kHz} \) in ideal condition. But in practical case we have to take care the drop across the diode also over the period of time which is around 1.5 V during turn on time of diode.

\[ 6T=(147+2.87)-1.5(T-33.53) \]

[33.53 is the off time of diode]

Which gives \( T \approx 30.79 \mu s \) and frequency \( = 32.478 \text{ kHz} \) By taking other no ideality in MOSFET, inductor, capacitor practical switching frequency is coming around 36.6 kHz.
The above Proposed and designed converter is Simulated using PSpice-Orcad Capture Software and observed the results i.e. Current through the resonant inductor and voltage across resonant capacitor and MOSFET gate triggered pulses and output voltage

5.1 Pspice circuit diagram

![Pspice circuit diagram](Fig5.1)  
**Fig5.1:** Pspice model of ZCS buck converter

Simulated Results

![Simulated Results](Fig5.2)  
**Fig5.2:** Pulses to the MOSFET

![Simulated Results](Fig5.3)  
**Fig5.3:** Current through the resonant inductor

![Simulated Results](Fig5.4)  
**Fig5.4:** Voltage across the resonant capacitor

![Simulated Results](Fig5.5)  
**Fig5.5:** Voltage across the output terminal

6. EXPERIMENTAL RESULTS  
5W (5V/1.0A) prototype of the ZCS converter, as shown in Fig.5.1 is built to verify the theory. And the result is compared with simulation. The specifications of the experimental prototype is as follows: Input voltage = 12V, Output voltage = 5V, output current = 1.0Amps
Circuit parameters of the proposed converter are as follows.

1) Switch: MOSFET IRFP250.
2) Diode: IN4001.
3) Resonant capacitor: 0.2 uF.
4) Filter capacitor: 20uF.
5) Resonant inductor: 20uH.
6) Output filter inductor: 2.0mH.
7) Load resistor 5 ohms

In experimental setup we can generate triggering pulses to drive the MOSFET by using 555 timer. Here we generated 7.76 V as a gate pulse from the timer. This pulse input is not enough to drive the Mosfet IRFP250. Hence we have to amplify the signal beyond 10 volts. Because the minimum voltage required to drive the MOSFET is to be 10 volts. To amplify this signal we are using MOSFET driver IRS2110. Now we have the pulse with the amplitude of 15.6 volts. This voltage is enough to drive our MOSFET IRFP250.

After applying this gate pulse we observe the corresponding waveforms comparing with the simulation results.

The R₁ and R₂ resistors of 555 Timer are calculated as below

\[ T_{on} = 0.693RC \]

\[ R_1 = \frac{T_{on}}{0.693C_1} \]

The On period \( T_{on} = 10 \) micro seconds and \( C_1 = 1 \) nano farads

Then the value \( R_1 = 14.4K \) ohm

\[ T_{off} = 0.693RC_1 \]

\[ R_2 = \frac{T_{off}}{0.693C_1} \]

The On period \( T_{off} = 20 \) micro seconds and \( C_1 = 1 \) nano farads

Then the value \( R_2 = 28.9K \) ohm

The resultant 555 timer configuration is given below

![Fig6.2: Circuit configuration of 555 Timer](image)

**IRS2110 Gate Driver Circuit**

![Fig6.3: Pin configuration of IRS2110](image)
5.3.3 Experimental Setup and Results

In this paper, we analyse, design and implemented the ZCS based 5W(5V/1A) resonant DC-DC buck converter. The various modes of operation of L-type ZCS resonant converter and time analysis of the resonant capacitor voltage and resonant inductor current waveforms analyzed. The ZCS resonant converter is simulated using the IRS2110 as a low side MOSFET driver.
Pspice-Orcad capture software and also implemented the experimental(hardware) prototype. In hardware implementation the required pulses are generated by IC555 Timer and amplified by IRS2110 i.e used for switching the MOSFET IRFP250. The simulated results resonant capacitor voltage, resonant inductor current and output voltage executed successfully are compared with the hardware results and also compared with the theoretical waveforms. At final we concluded that in high power applications the switching losses are reduced drastically due to incorporation of LC based resonant circuit in conventional buck converter and improved the performance and efficiency of the converter.

REFERENCES