Design And Evaluation Of High Speed Low Power Area Efficient PI-MBEC Carry Select Adder

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Abstract: **Computation speeds have increased dramatically during the past three decades resulting from the development of various technologies. The execution speed of an arithmetic operation is a function of two factors. The first is the circuit technology and the second is the used algorithm. Algorithm goals include the adder structures and the Data format. In this paper, a 16-bit conditional Possible Input Modified Binary to Excess One Converter (PI-MBEC) carry select adder is used to reduce the area in an efficient gate-level modification by reducing the most significant bit function in Binary to Excess One Converter (BEC) structure. Based on this modification 16-bit PI-BEC Carry Select Adder architecture has been developed and compared with the existing 16-bit BEC Carry Select Adder architecture. This work analyses the behavior and estimates the performance of the proposed design with the existing 16-bit BEC Carry Select Adder design in terms of area (Gate count), delay and power. The implemented design in this work has been coded using very high speed hardware description language. From the results, it is clear that the proposed design has reduced area and power to a great extent when compared with the BEC Carry Select Adder. The PI-MBEC adder architecture is therefore low area, low power and high speed approaches for VLSI hardware implementation.**

Keywords: **Binary to Excess One Converter, Carry Select Adder, Xilinx, Low power, Delay, Area efficient, Possible input.**

1. Introduction:

High-speed computation (addition and multiplication) has always been a fundamental requirement of high-performance processors and systems. In digital adders, the speed of addition is limited by the slack time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Ramkumar B and Harish M Kittur, (2010) used Binary to Excess One Convertor (BEC) instead of RCA with Cin=1 in the SQRT CSLA to achieve low power and area consumption. The basic objective of this paper is to use Possible Input Modified Binary to Excess One Converter (PI-MBEC) instead of BEC in the Carry Select Adder to achieve lower delay, area and power consumption. The main advantage of PI-MBEC is used to reduce the number of logic gates in the most significant bit function and reduce the critical path delay by the possible inputs than the BEC architecture.

This paper is structured as follows:

Section 2 provides the background literature relevant to PI-MBEC carry select adder. Section 3 describes the delay and area evaluation methodology of the basic components of the design in detail. Section 4 is devoted to a study of the BEC CSLA. Section 5 introduces the high speed new energy and area saving strategy and explains the basic principles that drive the mechanism in the Proposed design PI-MBEC CSLA. Section 6 presents delay, area and power comparision of the Proposed design PI-MBEC and the BEC CSLA design. Finally from the comparision the proposed architecture requires low power, delay and area than BEC CSLA. Section 7 provides a hardware implementation details and a summary of the results obtained through testing and provides a detailed analysis of the results.

2. Possible Input Modified Binary to Excess One Converter (PI-MBEC) carry select adder

The main idea of this design is to use PI-MBEC instead of the BEC in order to reduce the delay, area and power consumption of the BEC CSLA by the possible inputs. Basic function of the CSLA using the 4-bit PI-MBEC and function table of 4-bit PI-MBEC are Shown in figure2 and table2.

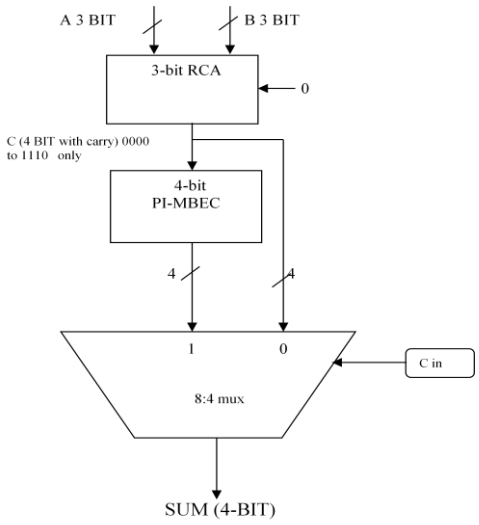

Figure 1 illustrates the logic architecture of the 4bit PI-MBEC group.

The inputs (A and B) of 3-bit RCA with Cin=0 are varies from 000 to 111. If the two inputs A and B are 111(maximum value) the output C(4 BIT with carry) of 3-bit RCA with Cin=0 is 1110. So the Possible Input(C) of 4-bit PI-MBEC is varies from 0000 to 1110 only. One input of the 8:4 mux is the 3-bit RCA with Cin=0 output (C) and another input of mux is the 4-bit PI-MBEC output (X).According to the control signal (Cin) the mux is used to select either the 3-bit RCA with Cin=0 output (C) or the 4-bit PI-MBEC output (X).

Table 1 Function table of 4 bit PI-MBEC

Possible input (C) of PI-MBEC	Excess-1 output (X) of PI-MBEC
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111

*(1111) input is not possible.

Possible input reduces the MSB function using OR gate in the PI-MBEC instead of using XOR gate in the BEC.

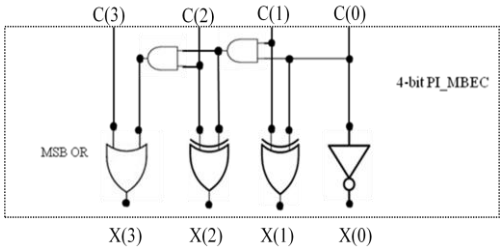

Figure 2 4 bit PI-MBEC

The Boolean expressions of the 4-bit PI-MBEC is listed below
X(0) = NOT C(0)

X(1) = C(0) XOR C(1)

X(2) = C(2) XOR (C(0) AND C(1))

X(3) = C(3) **OR** (C(0) AND C(1) AND C(2))

3. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC BLOCKS

3.1. XOR GATE

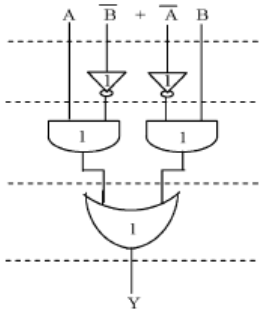

Figure 3 Structure of XOR Gate

Table 2 Delay and Area count of the Basic Blocks of CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Figure 3. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. Then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

4. STRUCTURE OF BEC CARRY SELECT ADDER.

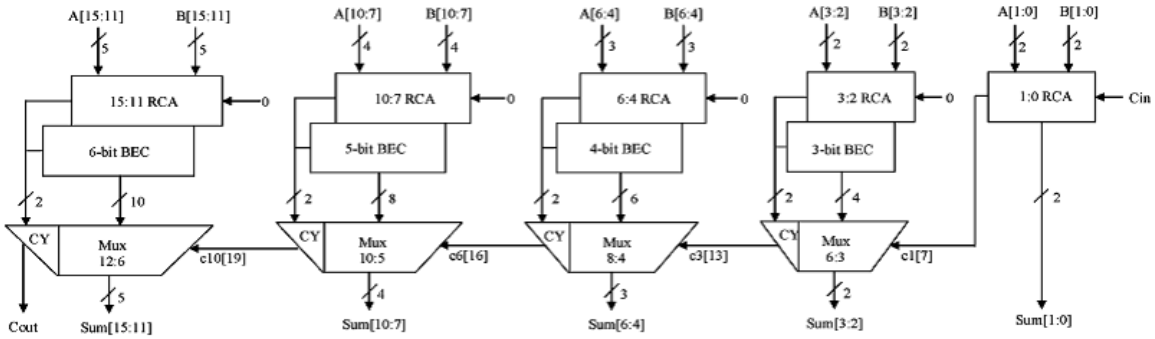

Figure 4 16 BIT BEC CSLA

4.1 DELAY AND AREA EVALUATION METHODOLOGY OF 16-BIT BEC CSLA

The structure split into five groups. The delay and area estimation of each group are shown in Figure 5 –10. The steps leading to the evaluation are given here.

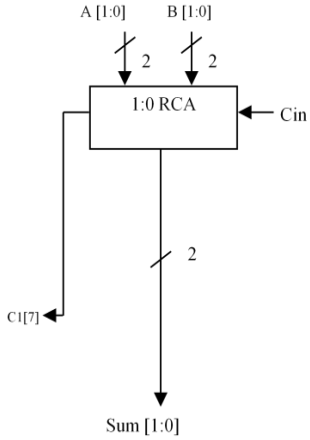

Figure 5 Structure of Group 1 – 16 BIT BEC CSLA

Maximum delay=8
*Gate count= RCA 2BIT Cin=1 → 2FA=2*13=26*

1) The group2 has one 2-b RCA which has 1 FA and 1 HA for Cin=0. Instead of another 2-bit RCA with Cin=1 a 3-bit BEC is used which adds one to the output from 2-bit RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t)=7] of 6:3 mux is earlier than the s3[t=9] and c3[t=10] and later than the s2[t=4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

2) The area count of group2 is determined as follows:

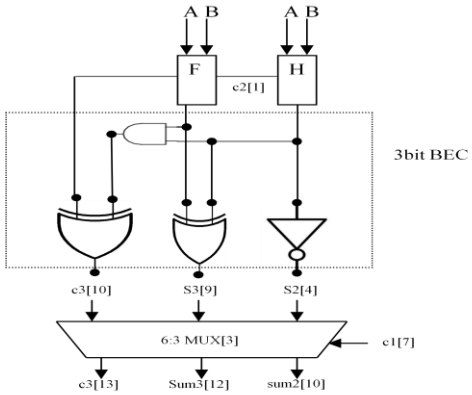

Figure 6 Structure of Group 2 – 16 BIT BEC CSLA

3) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

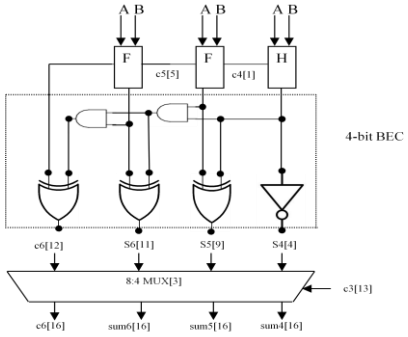

Figure 7 Structure of Group 3 – 16 BIT BEC CSLA

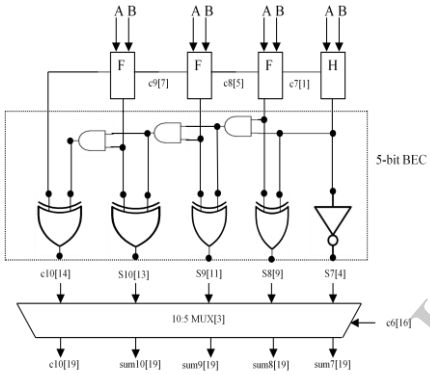

Figure 8 Structure of Group 4 – 16 BIT BEC CSLA

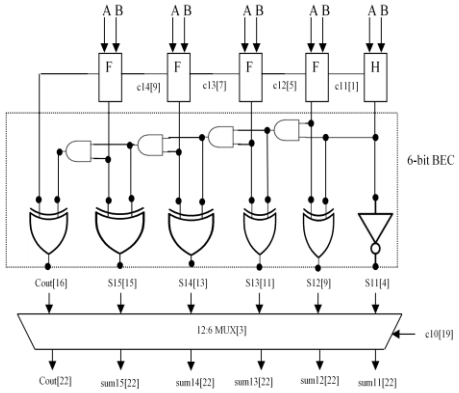

Figure 9 Structure of Group 5 – 16 BIT BEC CSLA

Maximum delay=22
RCA_5BIT Cin=0→1HA+4FA
*6_BIT BEC Gate count=1NOT+5XOR+4AND=1+(5*5)+4=30*

*Gatecount=1HA+4FA+6_BITBEC+6(2:1MUX)=6+(4*13)+30+(6*4)*

=6+52+30+24=112

4)Similarly, the estimated maximum delay and area of the all groups of the BEC CSLA are evaluated and listed in Table 3.

Table 3 Delay and Area of BEC CSLA Group

Group	Delay	Area (Gate Count)
Group1	8	26
Group2	13	43
Group3	16	66
Group4	19	89
Group5	22	112
TOTAL	78	336

5. PROPOSED PI-MBEC CARRY SELECT ADDER

The basic idea of the proposed work is using n-bit PI-MBEC CSLA to improve the speed of addition. The detailed structure and function of PI-MBEC is discussed in section 5.1. This logic can be implemented with any type of adder to further improve the speed. The proposed 16 bit PI-MBEC carry select adder is compared in with the conventional fast 16 bit BEC carry select adder. This work has realized the improved performance of the CSLA with PI-MBEC logic through custom design and layout .The proposed CSLA using PI-MBEC has reduced area, delay and power consumption of BEC CSLA. The basic idea of the proposed architecture is that which replaces the BEC by PI-MBEC.

5.1 STRUCTURE OF PI-MBEC CSLA

As stated above the main idea of this work is to use PI-MBEC instead of the BEC in order to achieve the high performance of the regular CSLA. To replace the 3-bit BEC, a 3-bit PI-MBEC is required. A structure of a 16-bit PI-MBEC carry select adder is shown in Figure 10.

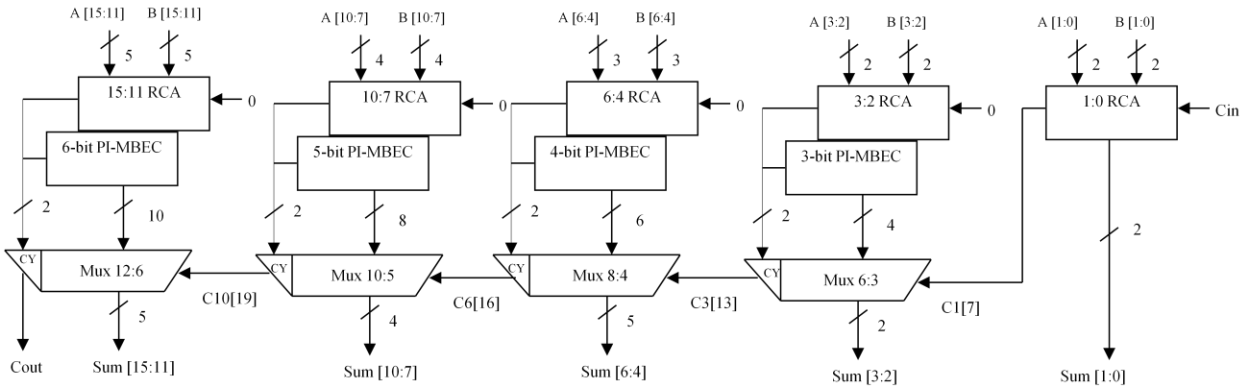

Figure 10 Proposed 16 BIT PI-MBEC CSLA

5.2 DELAY AND AREA EVALUATION METHODOLOGY OF 16-BIT PI-MBEC CSLA

Once again Split the structure into five groups. The delay and area estimation of each group are shown in Figure11–16. The steps leading to the evaluation are given here.

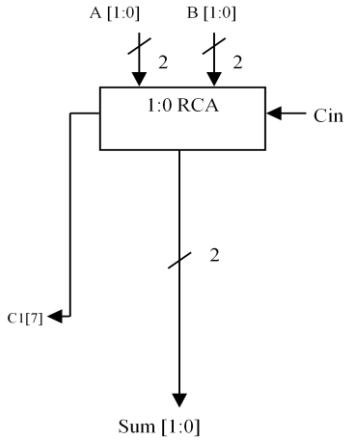

Figure 11 Structure of Group 1 – 16 BIT PI-MBEC CSLA

Maximum delay=8
*Gate count= RCA 2BIT Cin=1 → 2FA=2*13=26*

1) The group2 has one 2-bit RCA which has 1 FA and 1 HA for Cin=0. Instead of 3-b BEC, a 3-bit PI-MBEC is used which adds one to the output from 2-bit RCA with Cin=0. Based on the consideration of delay values of Table I, the arrival time of selection input c1[time(t)=7] of 6:3 mux is earlier than the s3[t=9] and c3[t=8] and later than the s2[t=4]. Thus, the sum3 and final c3 (output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.
2) The area count of group2 is determined as follows:

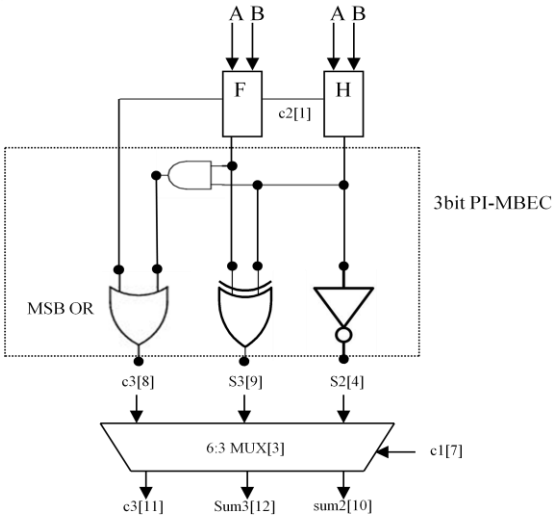

Figure 12 Structure of Group 2–16BIT PI-MBEC CSLA

3) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the PI-MBEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

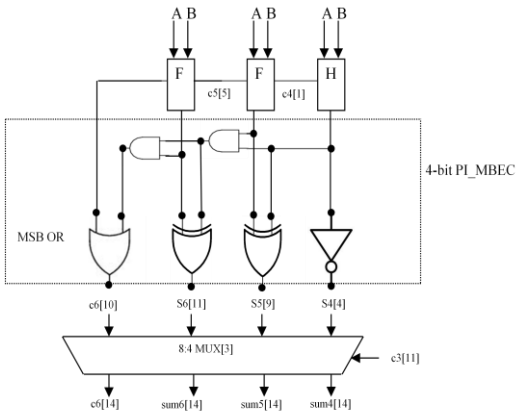

Figure 13 Structure of Group 3 – 16 BIT PI-MBEC CSLA

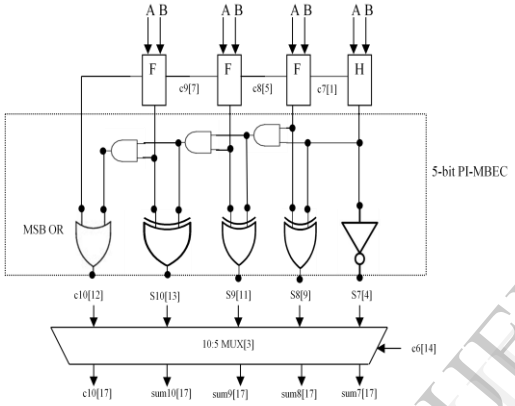

Figure 14 Structure of Group 4 –16 BIT PI-MBEC CSLA

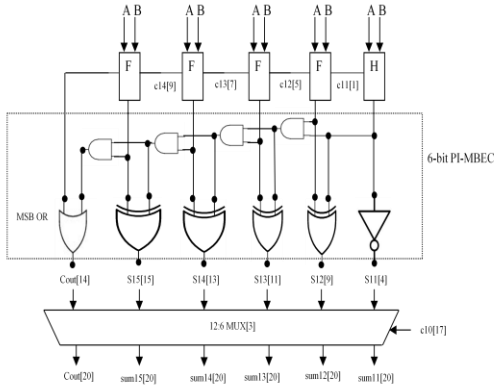

Figure 15 Structure of Group 5 –16 BIT PI-MBEC CSLA

Maximum delay=20
RCA_5BIT Cin=0→1HA+4FA
*6_ BIT PI-MBEC Gate count=1NOT+4XOR+4AND+10R=1+(4*5) +4+1=26*
*Gatecount=1HA+4FA+6_bit PI-MBEC +6(2:1MUX)=6+(4*13)+26+(6*4) =6+52+26+24=108*

4)Similarly, the estimated maximum delay and area of the all groups of the PI-MBEC CSLA are evaluated and listed in Table4 .

Table 4 Delay and Area of PI-MBEC CSLA Group

Group	**Delay**	**Area (Gate Count)**
Group1	8	26
Group2	12	39
Group3	14	62
Group4	17	85
Group5	20	108
TOTAL	71	320

6.SIMULATION AND ANALYSIS OF RESULTS

6.1 GROUP ANALYSIS

Simulation of 16-bit BEC CSLA and PI-MBEC CSLA has been done using Xilinx 13.2 tool. The designs of each type are as described in section 4 and 5. The analysis of results of the 16-bit BEC CSLA and PI-MBEC CSLA are shown in Figures 16 and17. Xilinx 13.2 navigator is used for synthesizing the code. The code is written using VHDL language. Table 3 and 4 illustrate delay and gate count of 16 Bit BEC CSLA and the proposed 16 Bit PI-MBEC CSLA.

From the Table 3 and 4, it is clear that the proposed16-bit PI-MBEC CSLA saves (336-320) 16 gate areas than the 16-bit BEC CSLA, with (71-78) 7 decreases in gate delays and (20-22) 2 decreases in gate maximum delays.To further evaluate the performance, the design has resorted to ASIC implementation and simulation.

The results depicted in Figure 16 shows that the proposed PI-MBEC CSLA has lesser gate count when compared to BEC CSLA.

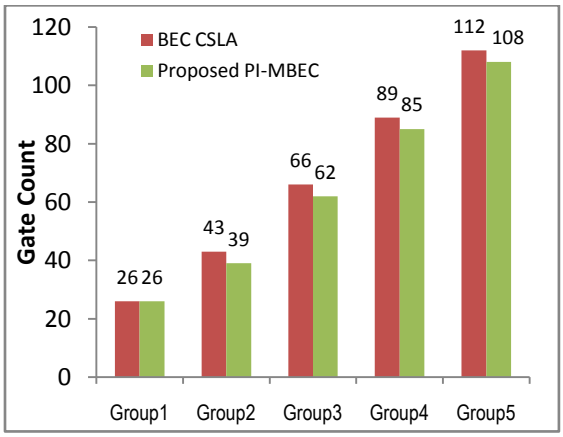

Figure16 Comparison of Gate Count

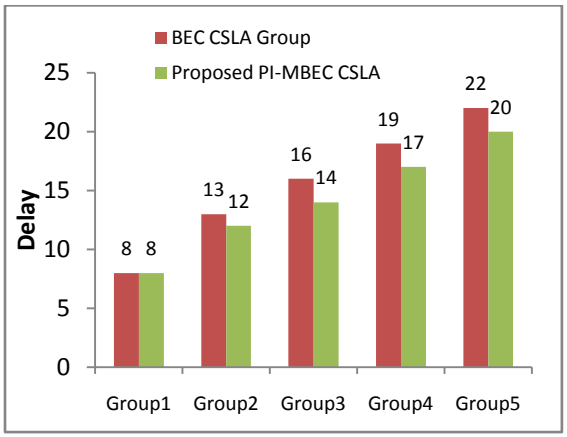

Figure 17 Comparison of Delay

Figure 17 compares the adder circuits for delay comparison. When compared to BEC CSLA with proposed PI-MBEC CSLA, the proposed circuit occupies less delay than BEC CSLA.

6.2 STAGE ANALYSIS

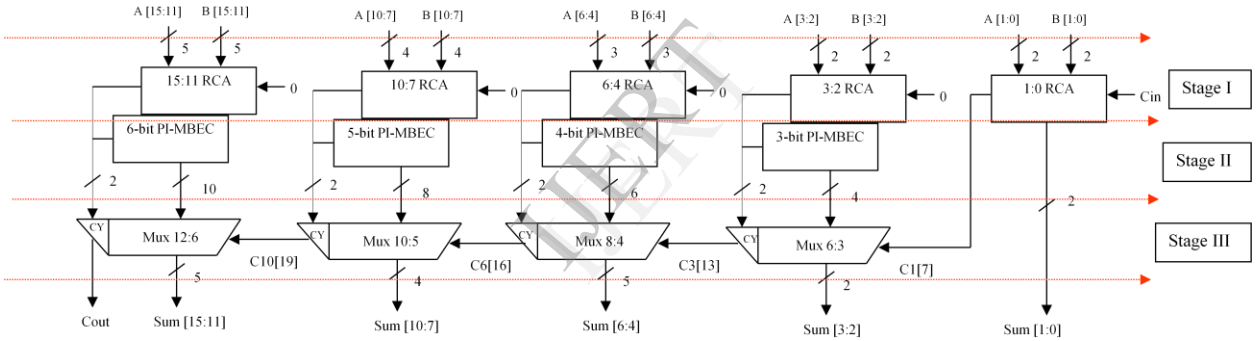

Figure 18 16 bit PI-MBEC CSLA

Table 5 Stage Analysis of SQRT and BEC CSLA

STAGE II					
16 Bit BEC CSLA			16 Bit PI-MBEC CSLA		
Block	Component	Gate Count	Block	Component	Gate Count
3_BIT BEC	1NOT, 1AND, 2 XOR	12	3_BIT PI-MBEC	1NOT, 1AND,1XOR,1OR	8
4_BIT BEC	1NOT,2AND, 3XOR	18	4_BIT PI-MBEC	1NOT,2AND,2XOR, 1OR	14
5_BIT BEC	1NOT,3AND, 4XOR	24	5_BIT PI-MBEC	1NOT,3AND,3XOR, 1OR	20
6_BIT BEC	1NOT,4AND, 5XOR	30	6_BIT PI-MBEC	1NOT,4AND,4XOR, 1OR	26
Total Gate Count		**84**	**Total Gate Count**		**68**

Gate Count in stage I and stage III are equal. But in stage II total 84 Gate count in BEC CSLA blocks was replaced by 68 Gate count in PI-MBEC that the PI-MBEC CSLA saves (84-68) 16 gate areas than the

BECCSLA.

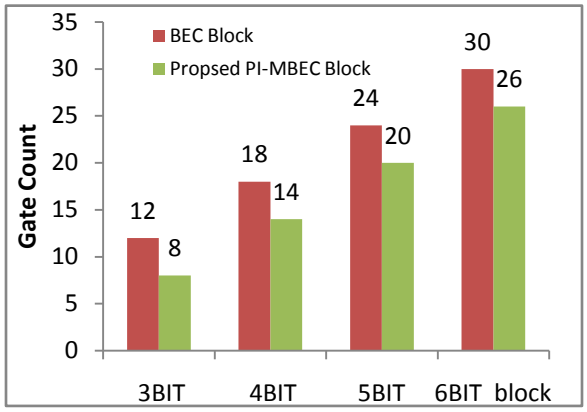

Figure 19 Comparison of Stage II

6.3 POWER ANALYSIS

The simulation files of two CSLA designs are imported to Xpower analyzer, and the performance of proposed PI-MBEC CSLA is analyzed and compared against the BEC CSLA designs.

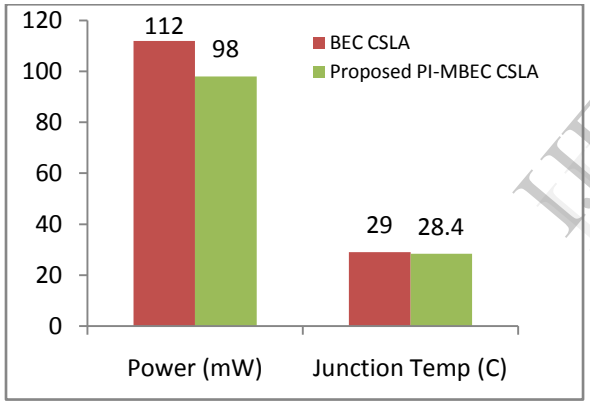

Figure 20 Comparison of Power and Junction Temperature

7. FPGA IMPLEMENTATION

Create user constraints file (UCF) file by configure the input and output pins of FPGA (SPARTAN 3E), then generate the programming file (BIT) and configure in the target device (Spartan 3E). The two adders are designed using VHDL language in Xilinx ISE Navigator 13.2. And all the simulations are performed using Xilinx ISim simulator. The performance of proposed PI-MBEC CSLA is analyzed and compared against the BEC CSLA design. The number of gates used in the design indicates the area of design. The power consumption is measured in terms of total power and dynamic power. The speed of the adder is estimated by the delay involved in the design. It can be seen from Table 3 and 4 that area, delay and power consumption of PI-MBEC is less than BEC CSLA. As the number of gates used in the design of PI-MBEC are fewer than the BEC CSLA. The reduced number of gates and delay of the PI-MBEC offers a great advantage in the reduction of area, total power consumption and increase in speed of computation.

CONCLUSIONS

A simple approach is proposed in this work to reduce number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared result with 16-bit BEC CSLA shows that the 16-bit PI-MBEC CSLA is significantly reduced by delay (9.09%), area (4.76%) and power (12.5%) respectively. The power-delay product and also the area delay product of the proposed PI-MBEC design which indicates the success of the method for high performance system. The proposed PI-MBEC CSLA architecture is therefore, low area, low power, and high speed efficient for VLSI hardware implementation.

The results thus far have been very encouraging and further investigations would help in fine tuning the PI-MBEC adder to bring maximum benefit. It would be very worthwhile investigating the use of area efficient PI-MBEC CSLA in place of BEC CSLA. In order to accurately measure energy consumption of the new system, VLSI implementations need to built and tested. This requires a detailed knowledge of the circuitry involved and synchronization of the CSLA designs. This analysis will be crucial in determining the commercial viability of the new system. An important factor that needs to be investigated is how a variable process time will affect implementation complexity of the algorithm.

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