Design and Delay Analysis of Various 256-Bit Adders using Verilog

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***Abstract* – In this paper, several adders are being examined and compared in terms of delay of throughput. The objective of this paper is to design different architecture of adders and to observe the reliable output. Existing adder's performance will widely vary with respect to their area requirements and speed of execution. The proposed adder's architecture named Ripple carry adder, Carry look ahead adder, Carry skip adder, Carry save adder, Carry select adder, decomposes into blocks of carry generator, carry propagator and multiplexer. As Addition is the most important operation in data processing hence its speed has a significant impact on digital circuits. We have demonstrated the efficiency of the proposed architectures along with the design method in 256 bit operands.**

Keywords – Throughput, RTL schematic, Technological schematic, Simulation, Ripple carry adder, Operands, RCA (Ripple Carry Adder), CLA (Carry Look Ahead adder), CSkA (Carry Skip Adder), CSA (Carry Save Adder), CSlA (Carry Select Adder), ALU (Arithmetic Logic unit)

I. INTRODUCTION

Adders are called a digital circuit because they perform addition of numbers. It is a circuit that sums up the amplitude of 3 inputs that gives 2 outputs called sum and carry.They are being used in many processor architectures, ALU and computational units. Each adder creates a carry value which needs to be propagated via the circuit adders. Even though for many number of representations, adders can be constructed in the form of binary- coded decimal or excess-3, the most common adders operate on binary numbers.

RLA is a digital adder circuit, where in the carry out of every full adder will be the carry in of the next most significant full adder. It is so called because each carry bit receives rippled into the following next stage. CLA or fast adder is a type of digital circuit. It calculates one or more carry bits earlier than the sum, which reduces the wait or delay time. CSA is a form of virtual adder used in computer microarchitecture to locate the sum of 3 extra n-bit numbers in binary. CSlA is a way to enforce an adder, which may be a logic detail that finds out the sum of numbers. CSkA is a type of adder implementation that improves on delay of RCA when compared to other adders.

II. EXPRESSION OF ADDER

Sum = A^B^Cin
Carry = (A&B)|(B&Cin)|(Cin&A)
Carry generator = A&B
Carry propagator = A^B

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth Table

III. METHODOLOGY

A. Ripple Carry Adder

Basically, a full adder plays the addition operation on three inputs and produces the two outputs. Initially, it performs the addition on two inputs such as A and B along with the third input carry as C-IN. The two outputs produced are designated as S and C-OUT, where S is sum and C-OUT as carry-out. Full adder is designed with such a logic that it is capable of taking eight inputs at a time in order to create a byte-wide adder and the output carry is cascaded from one adder to another.

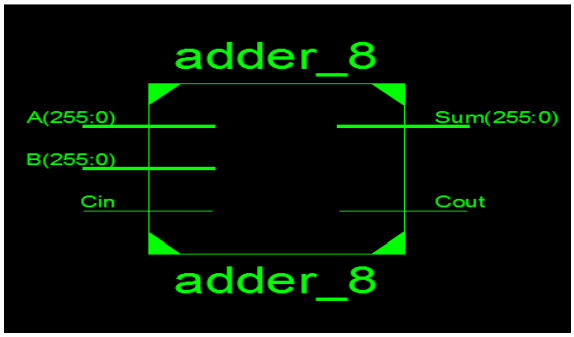

Figure 1: RTL View of RCA

Logical Expression for SUM:
= A' B' C-IN + A' B C-IN' + A B' C-IN' + A B C-IN
= C-IN (A' B' + A B) + C-IN' (A' B + A B')

= C-IN XOR (A XOR B)
Logical Expression for C-OUT:
= A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN
= A B + B C-IN + A C-IN

By making use of the truth table, we can implement the full adder logic. Sum expression is an XOR operation between the inputs A, B and C-IN whereas Carry-out expression is an AND&OR operation between the inputs A,B and C-IN.

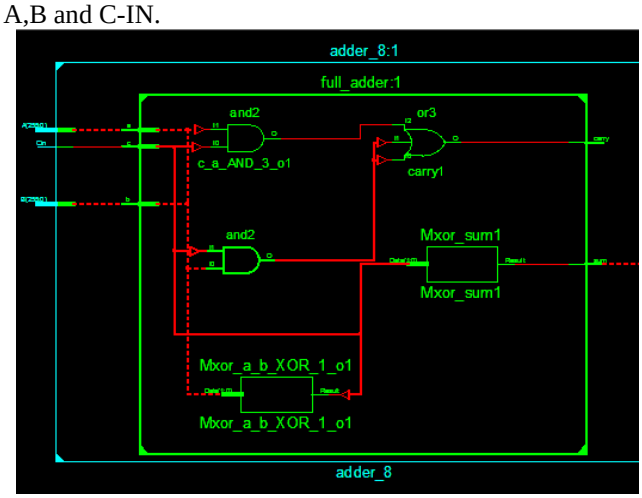

Figure 2: Technological View of RCA

B. Carry Look Ahead adder

A carry-look ahead adder (CLA) is also known as a fast adder which is basically used in digital logic. It is known as a fast adder because it increases the speed by reducing the time required to interpret the carry bits Working of the CLA follows like this, initially it calculates the carry bits before sum, so it is helpful in reducing the propagation delay to find the result of the larger bits of the adder.(P. Balasubramanian, 2016)

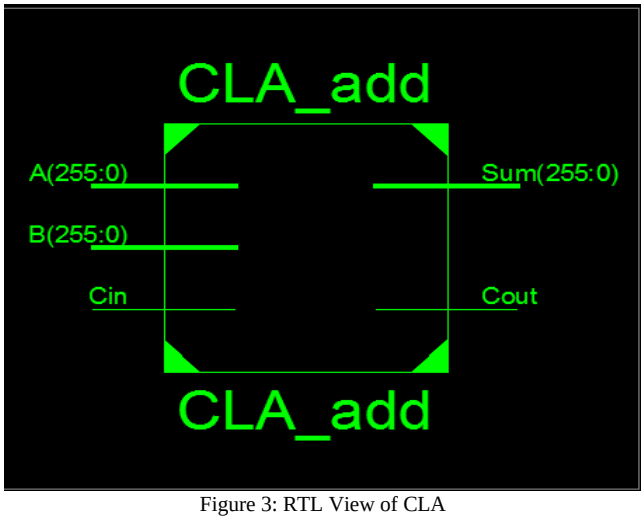

Figure 3: RTL View of CLA

The carry look ahead requires the additional hardware to improve its speed but it is not dependent on the number of bits. Basically this adder makes use of propagating and generating carries. Fast adder mainly depends on two things i.e. Calculating for each digit position whether it is going to propagate the carry, now the word digit can be replaced by the word bit since it makes use of the concepts generating and propagating carries. Secondly, by combining all these calculated values to deduce quickly to know whether the group is going to propagate the carry which comes in from the right.

G (A, B) =A & B
P (A, B) =A+B

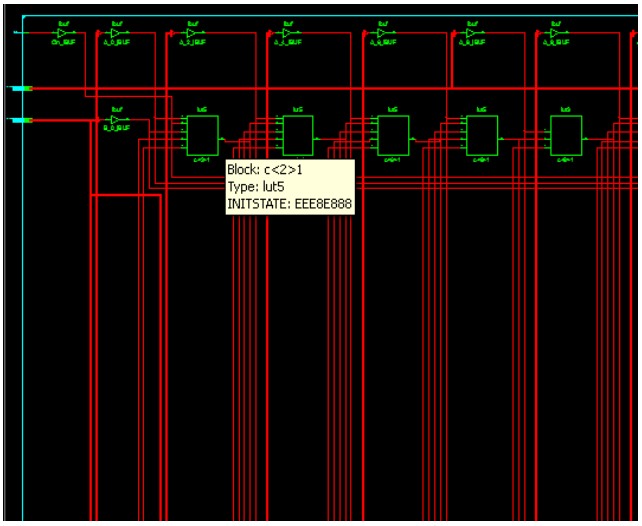

Figure 4: Technological View of CLA

C. Carry Skip adder

Carry Skip adder is often called as Carry by-pass adder. In this the implementation of the adder enhances the delay of RCA with less effort when compared with other adders. In the worst case, the improvement in delay is achieved by making use of several carry by-pass adders to form a block-carry-skip-adder. Unlike the other adders such as RCA, CLA etc. the performance of this carry skip adder can be enhanced with only a few combinations of input bits. The critical path in this adder begins at the first full adder. In order to reduce this critical path, block-carry-skip adders are used where the skip adders are chained.

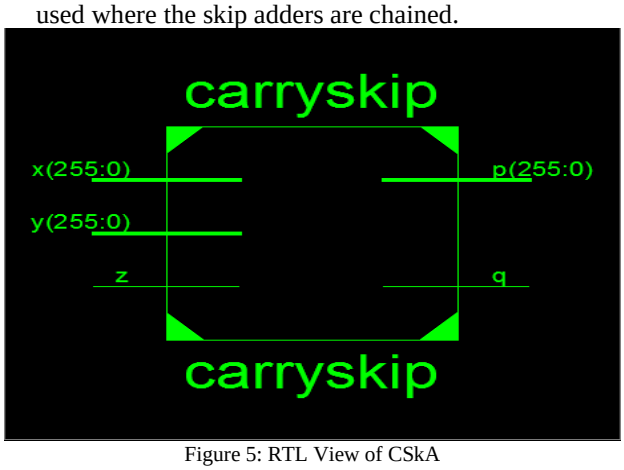

Figure 5: RTL View of CSkA

Block-carry-skip adders are basically composed of many number of carry-skip adders. Mainly there are two kinds of this adder i.e. Fixed size block-carry-bypassadders and Variable size block-carry-bypass adders. The critical path in this fixed size adders consists of the ripple path and the first block consists of the skip element. The performance of this adder can be still increased by making use of the variable

size block-carry-skip adders i.e. the preliminary blocks of this adder are made smaller to notice the carry generated quickly to propagate in addition and the middle blocks are not made small later the most significant blocks are made small so that the carry inputs arriving late is processed quickly.(Shweta Thakur, Aug 2018)

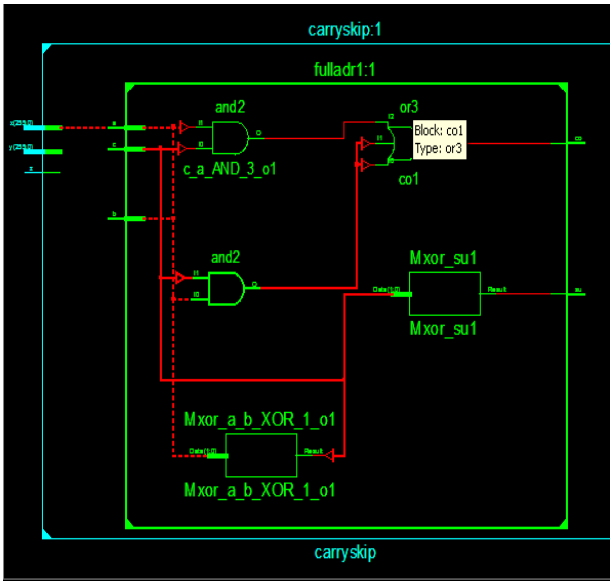

Figure 6: Technological View of CSkA

D. *Carry Save adder*

In Ripple Carry Adder (RCA), propagation of carry from one stage to the other stage takes longer time. Due to this reasonRCA will introduce an overall delay in the circuit. In order to avoid this problem, carry save adder came into an existent. It also had sort out the delay problem up to certain extent. Due to which the propagation of carry in carry save adder can be avoided. In this adder partial sum and partial carry is generated and also get stored. The partial carry which is stored cannot be propagated to the successivebits of higher order. The generated partial carry and partial sum in last step will be get added by using any of the carry propagation adder.(Ashvin Chudasama, 2016)

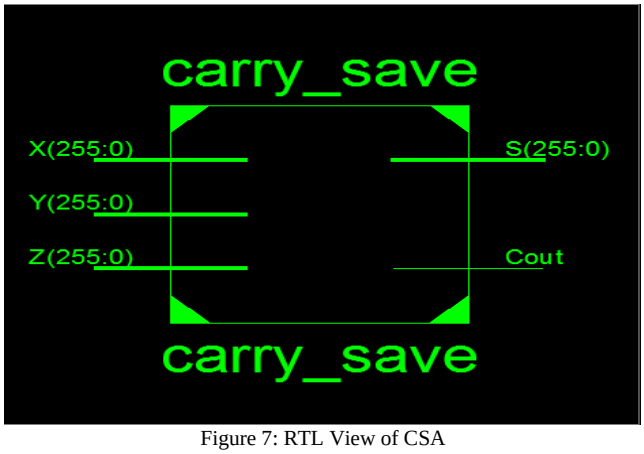

Figure 7: RTL View of CSA

In order to avoid waiting for ripple,carry look ahead adder adds up the group generate signals and group propagate signals. Carry Look Ahead adder provides higher delay for the higher order bits when compared to other adders due to the existence of large number ofgates. In digital adders, speed of the addition is defined by timeneeded to propagate the carry acrossthe adder. In case of primary adder for eachbit position the sum is generated sequentially only after the previous bit position has been summed.

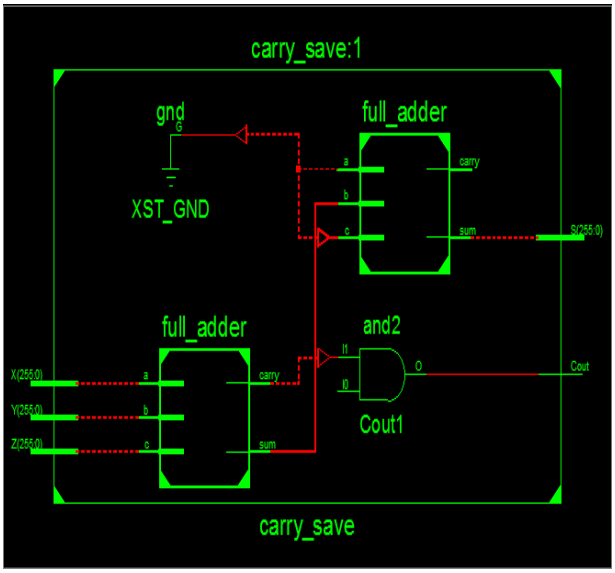

Figure 8: Technological View of CSA

E. *Carry Select adder*

The carry-select adder comprises two ripple carry adders and a multiplexer. Addition of two n-bit numbers with a carry-select adder is computed with two adders, therefore we use two ripple carry adders. In order to perform the calculation twice, one time by assuming the carry-in being zero and the other time assuming it will be one. After both the results are calculated, the correct sum, and the correct carry-out, is selected by the multiplexer once when the correct carry-in is known. Therefore the wide variety of bits in every carry select block can be uniform, or variable.(Bala Sindhuri Kandulaa, 2016)

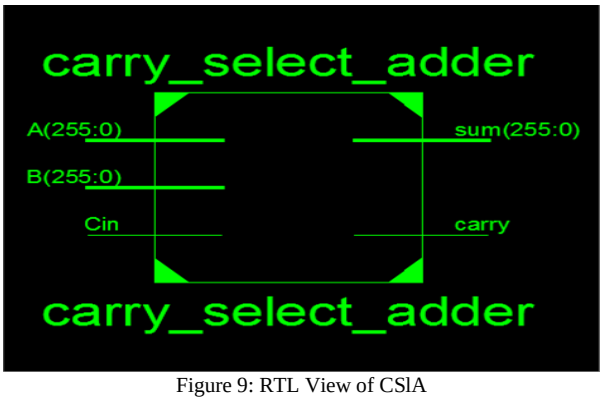

Figure 9: RTL View of CSlA

Figure 9 is the RTL (register transfer level) view of the carry select adder. It has 3 inputs A, B and Cin with the sum and carry as output. Since we are working on 256 bit the inputs to A, B are 255:0 which is equal to 256 bit.
After working with the Xilinx tool the simulation output was 5.31 secs which is the CPU execution time.

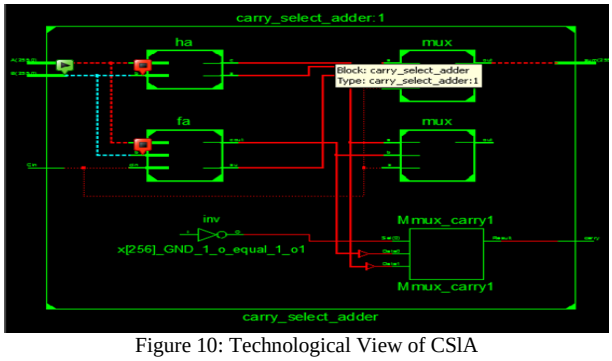

Figure 10: Technological View of CSlA

IV. SIMULATION RESULT

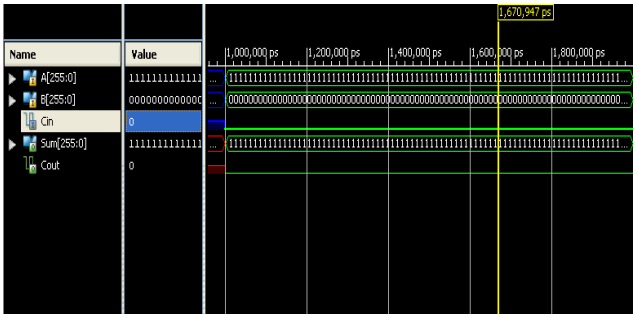

Figure 11: RLA

Timing Report:
Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.41 secs

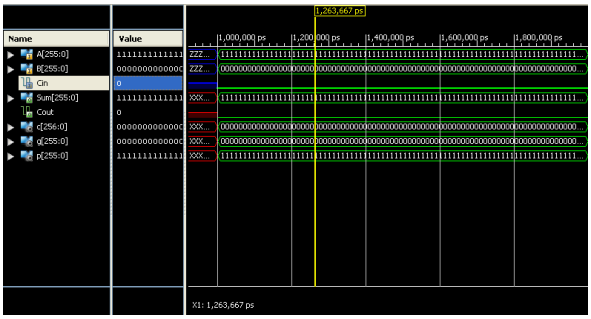

Figure 12: CLA

Timing Report:
Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 5.06 secs

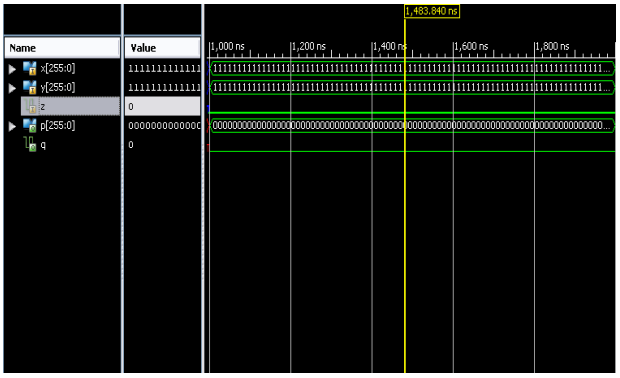

Figure 13: CSkA

Timing Report:
Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.39secs

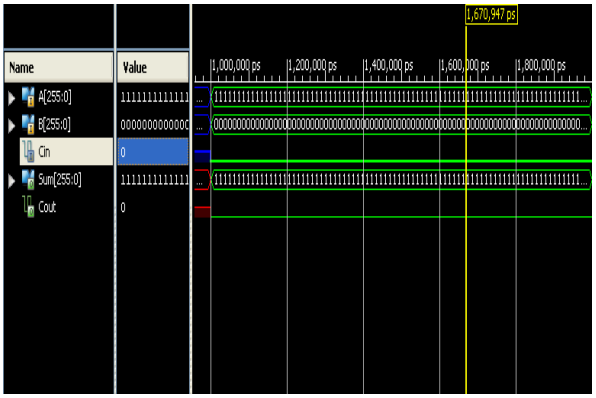

Figure 14: CSA

Timing Report:
Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.28 secs

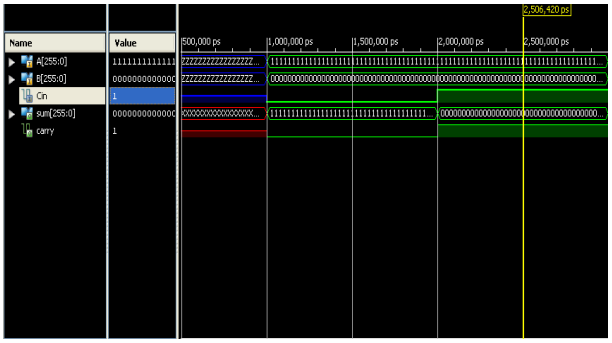

Figure 15: CSlA

Timing Report:
Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.31 secs

V. CONCLUSION

SL.NO	TYPES OF ADDERS	REAL TIME EXECUTION(IN SECS)	CPU TIME EXECUTION(IN SECS)
1	RCA	6.00	5.41
2	CLA	5.00	5.06
3	CSkA	6.00	5.39
4	CSA	6.00	5.28
5	CSlA	6.00	5.31

Table 2: Comparison Table

An extensive performance of all types of adders has been examined. Their performance was analyzed in terms of gate level and delay throughput. From this analysis, 256 bits' ripple carry adder is just a series of full adder connected serially where carry propagator from first full adder to last one. Delay is maximum on this case. Carry look ahead adder is one which is calculated beforehand and of course delay is much lesser when compared to others. In carry save and carry select adder, the delay is minimum as compared to carry skip and full adder. Therefore, carry skip is faster than full adder. Hence it can be concluded by stating that full adder has the maximum delay when compared to other

adders (carry look ahead adder, carry skip adder, carry save adder, carry select adder)(Kunjan D. Shinde)

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