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Design And Comparison Of Flip-Flops Using CMOS Technology

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Abstract

This project develops a methodology for selecting and optimizing flip-flops for high-performance and low-energy systems. The transistor sizes are optimized for minimal delay under constrained energy consumption and a novel analysis and comparison strategy is proposed, which suitably accounts for all the previously mentioned aspects to achieve fair and meaningful results. In this one main approach has been suggested to reduce clock dissipation in Dual Edge Triggered flip-flops (DET). In this part, Low power, energy efficient CMOS Flip-flops using dual edge triggering is proposed. Four DET Topologies are compared using DSCH3.1 and Microwind3.1 CAD tool in 65 and 120nm technology. Among these four topologies it is observed that the DET-TGLM has the best power, delay and PDP compared to remaining. The DET-TGLM reduces the large amount of capacitance at every clock transition. It is observed that DET-SPL produces the minimal power-delay product among the four technologies. Hence the use of SPL Flip-Flop in critical timing paths, the performance characteristics of a circuit can be significantly improved. Therefore the proposed DET Topology is a better solution for reducing clock related power consumption and also minimizing the overall power consumption of the circuit.

In the second part the effect of PVT (Process, Voltage, and Temperature) variations on the performance of proposed flip-flops is investigated.

Key Words— *CMOS, Flip-flops , Delay, DET topologies, clocking, clock dissipation, Master-Slave, Low-power, High- performance, Energy consumption, power delay product (PDP).*

1. Introduction

Flip-Flops (FFs) are the basic building blocks of data path structures. Indeed, they allow for the storage of data processed by combinational circuits and the synchronization of operations at a given clock frequency. Because of their multistage structure, high clock switching activity, and increasing portion of clock period occupied by their timing latency, the speed and energy of FFs significantly affect the overall performance of a data path. Optimal FF design strategies are usually based on automated algorithms embedded directly into simulators. These algorithms are powerful methods to optimize constraints such as speed, energy consumption, or energy-delay products, even for complicated FFs consisting of several internal nodes. Moreover, they also allow to account for the joint optimization of FFs and clock networks, for instance, through a proper clock slope setting. Of course, the resulting design strategies will depend on the specific FF topology and on the design constraint to be optimized.

The appropriate choice of flip-flop (FF) topologies is of Fundamental importance in the design of VLSI integrated Circuits and in particular, of both high-speed and low-energy Microprocessors. Indeed, FFs affect the clock frequency, since their delay occupies a significant fraction of the clock Cycle, especially in fast micro-architectures with low logic depth. Moreover, together with the circuits devoted to the clock generation and distribution,FFs are part of the clock network, which is responsible for 30%–50% of the whole chip energy budget.Latches and flip-flops are basic sequential elements commonly used to store logic values and are always associated with the use of clocks and clocking networks.

In low-energy, constant throughput system, the supply voltage is often scaled down to minimize the energy consumption. The design of the clocking subsystem-register elements and clock distribution network-has to be resistant to noise and timing failures for robust circuit operation. Noise robust designs are usually fully static or pseudo-static. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. In addition, from a timing perspective, flip-flop latency consumes a large portion of the cycle time while the operating frequency increases.

Accordingly, flip-flop choice and design has a profound effect both in reducing the power dissipation and in providing more slack time for easier time budgeting in high-performance systems.

In this paper, large number of DET topologies having less power dissipation, delay and energy in a 65nm and 120nm CMOS technology are proposed. The organization of the paper is as follows. In section 2 DET topologies are proposed. In section 3 result analysis is presented. Finally, conclusions are presented in Section 4.

2. *Dual edge-triggered (DET) flip-flops:*

Dual edge-triggered (DET) flip-flops provide an effective technique for reducing the power consumption of a large design by reducing the power consumed in the clock distribution network. An ideal dual edge-triggered flip-flop allows the same data throughput as a single edge-triggered (SET) flip-flop while operating at half the clock frequency and sampling data on both edges of the clock

The four DET topologies are as follows:

- Transmission Gate Latch-Mux [3] (DET-TGLM);
- Symmetric Pulse Generator FF [4] (DET-SPGFF);
- Static Pulsed Latch [5] (DET-SPL);
- Conditional Discharge FF [6] (DET-CDFF).

2.1. Transmission Gate Latch-Mux (DET-TGLM):

In DET-TGLM, the data transfer between latches is made unidirectional. The unidirectional **nature** of this transfer improves the IDDQ **testability, as** well **as** the performance and also reduces the large amount of capacitance at every clock transition.

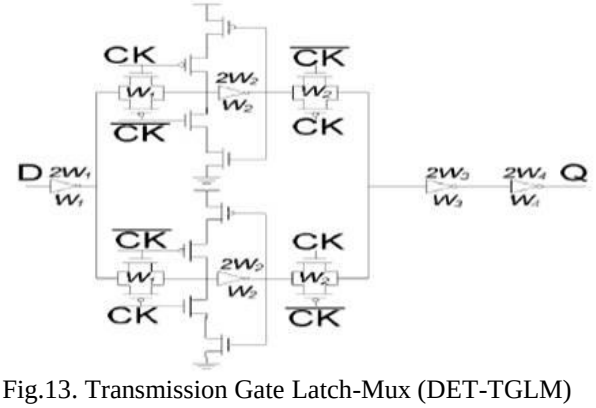


Fig.13. Transmission Gate Latch-Mux (DET-TGLM)

2.2. Symmetric Pulse Generator FF (DET-SPGFF):

We present a new dual-edge triggered flip-flop (DETFF) that exhibits low delay and small power consumption compared to other storage elements. The new DETSE uses two symmetric pulse generator stages, each one responding to one particular transition of the clock, hence the name *Symmetric Pulse Generator Flip- Flop* (SPG-FF). Node *X* is allowed to switch to a low level only in the short time window following the rising clock edge. This time window is defined by the delay of three inverters *Inv1-Inv3* (Fig.14), this feature makes the set-up time of the storage element negative and the short transparency window makes clock uncertainty absorption possible.

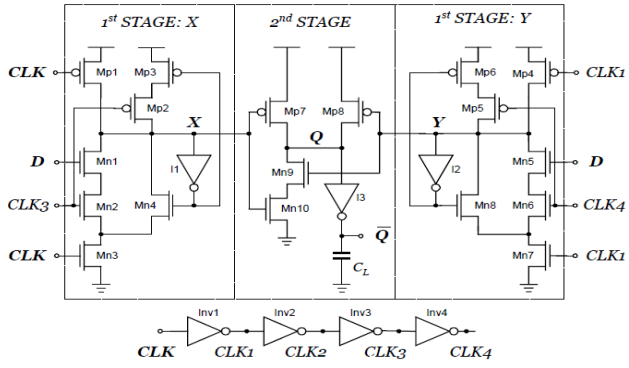


Fig.14. Symmetric Pulse Generator FF (DET-SPGFF)

An advantageous property of SPG-FF is that the critical path consists of a single domino-like gate whose first stage is dynamic (*1st STAGE: X* or *1st STAGE: Y*) and second stage is the static *NAND* gate from Fig. 15. Consequently, a static output is available after two fast logic stages. Normally, the transistors are sized so that each stage has about the same gain. In this case, speed is traded for power consumption.

2.3. Static Pulsed Latch (DET-SPL):

An energy efficient ***dual edge-triggered,*** static pulsed latch is shown in Fig.15.The path from data to output of the flip- flop is identical to the single edge triggered flip flops**,** latency and throughput of static pulsed latch are same as single edge triggered flip flops**,** while the clock frequency is halved. **As** a result, the power dissipation of **DET-SPL** with a local pulse generator is 21% less than **SET**. Sharing the pulse generator is not as effective for the **DET-SPL as** for the **SET** since the transistor sizes are larger; therefore if sharing is possible the single edge-triggered has the lowest energy consumption. These comparisons reflect only the energy of the flip-flop itself and do not include power in the clock distribution network.

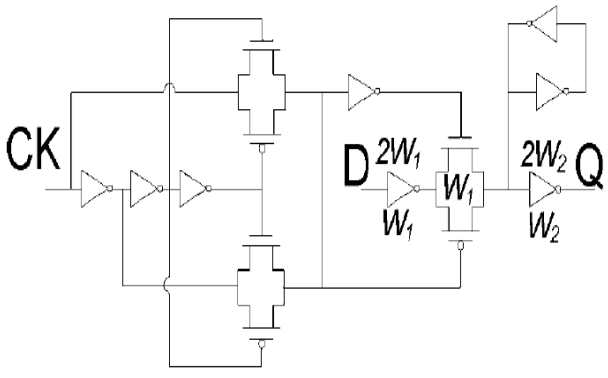


Fig.15. Static Pulsed Latch (DET-SPL)

2.4. Conditional Discharge FF (DET-CDFF):

The conditional discharging scheme is employed in the CDFF as follows: in order to reduce the redundant switch power, we employ a discharge control transistor N5 at the discharge path of the first stage.

Since node X is not charged and discharged every clock cycle, no glitches appear on the output node Q when the input D stays high, and Q will not be discharged at the beginning of each evaluation. As a result, CDFF features less switching noise generation, which is an important issue in mixed signal circuits. Moreover, node stays HIGH or precharged in most cases, which helps in simplifying the keeper structure as shown in Fig.16, and it also reduces the capacitive load at node.

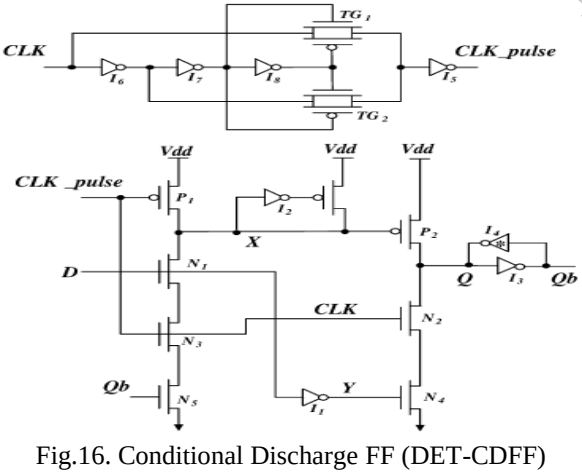


Fig.16. Conditional Discharge FF (DET-CDFF)

3. *Simulation and Implementation Results:*

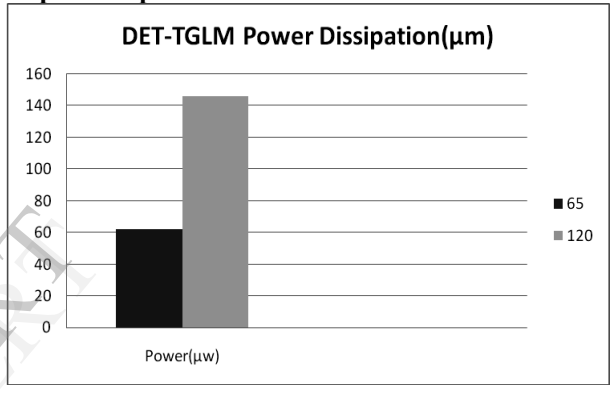
In this work, we compare and analyze four DET Topologies using 65 and 120nm technologies. The figure of merit used to compare these technologies is Power-Delay Product (PDP). The DET Topologies implemented in this work are Transmission Gate Latch-Mux, Symmetric Pulse Generator FF Static Pulsed Latch Conditional Discharge FF which are given below in the tables.

Result Analysis: DET-TGLM

Technology	65nm	120nm
Power Dissipation(µw)	61.977	146
Delay(ns)	0.050	1.138
PDP(*10-15)	3.0988 5	166.14 8
Area(µm2)	164.02	491.30

Fig: Result analysis

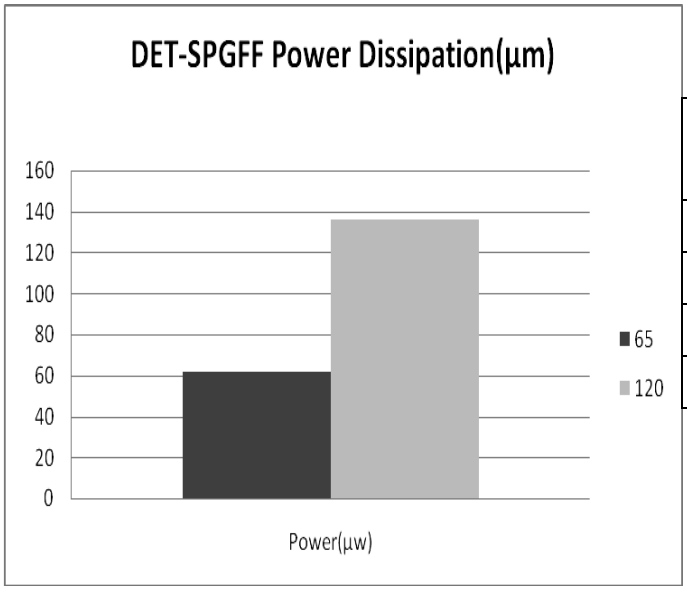
Graphical representation:



Result Analysis: DET-SPGF

Technology	65nm	120nm
Power Dissipation(µw)	61.432	136
Delay(ns)	0.077	1.777
PDP(*10-15)	4.73026	241.672
Area(µm2)	124.58	370

Graphical representation:

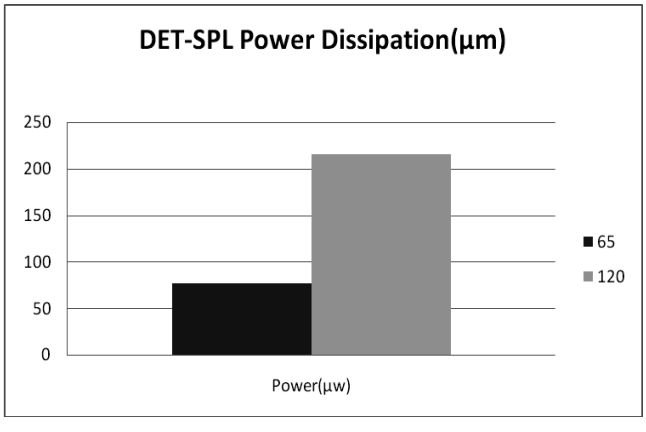


Result Analysis: DET-SPL

Technology	65nm	120nm
Power Dissipation(µw)	77.132	216
Delay(ns)	0.049	1.205
PDP(*10-15)	3.7794 6	260.28
Area(µm2)	47.80	144.59

Fig: Result analysis

Graphical representation:



Comparative Analysis of DET FF Topologies:

Technique	Power (µw)	Delay (ns)	PDP (*10-15)	Area (µm2)
DET-TGLM	61.977	0.050	3.09885	164.02
DET-SPGFF	61.432	0.077	4.73026	124.58
DET-SPL	77.132	0.049	3.77946	47.80
DET-CDFF	93.670	0.113	10.5847	77.44

Fig: DET FF Topologies in 65nm Technology

Technique	Power(µw)	Delay(ns)	PDP (*10-15)	A(µm2)
DET-TGLM	146	1.138	166.148	491.30
DET-SPGFF	136	1.777	241.672	370
DET-SPL	216	1.205	260.28	144.59
DET-CDFF	233	2.629	612.557	233.91

The DET Topologies implemented in this work are Transmission Gate Latch-Mux, Symmetric Pulse Generator FF, Static Pulsed Latch Conditional Discharge FF are successfully implemented using DSM Technology. Considering the power-delay product [PDP] as the figure of merit, we compared each of the circuits. It is observed that DET-SPL produces the minimal power-delay product among the four technologies. Hence the use of SPL Flip-Flop in critical timing paths, the performance characteristics of a circuit can be significantly improved. Therefore the proposed DET Topology is a better solution for reducing clock related power consumption and also minimizing the overall power consumption of the circuit.

4. Conclusions:

The DET Topologies implemented in this work are Transmission Gate Latch-Mux, Symmetric Pulse Generator FF, Static Pulsed Latch and Conditional Discharge FF are successfully implemented using 65

and 120 nm technology. Considering the power-delay product [PDP] as the figure of merit, we compared each of the circuits. It is observed that DET-SPL produces the minimal power-delay product among the four topologies. Hence the use of SPL Flip-Flop in critical timing paths, the performance characteristics of a circuit can be significantly improved. Therefore the proposed DET Topology is a better solution for reducing clock related power consumption and also minimizing the overall power consumption of the circuit.

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