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Design and Comparative Analysis of Low Power Dynamic Random Access Memory Array Strucyure

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***Abstract*- Memory plays an essential role in the design of electronic systems where storage of data is required. In this paper comparative analysis of different DRAM (Dynamic Random Access Memory) cell based memory array structure has been carried out in nanometer scale memories. Modern advanced processor use DRAM cells for chip and program memory. But the major drawback of DRAM is the power dissipation. The major contribution of power dissipation in DRAM is off-state leakage current. Also the improvement of power efficiency is difficult in DRAM cells. This paper investigates the power dissipation analysis in DRAM cells. Here 1T1C dram cell, 3T dram cell, 4T dram cell has been designed using TANNER EDA Tool.**

Keywords- DRAM cell; Memory Array; low power;

I.INTRODUCTION

On-chip memory has been widely used in VLSI (Very Large Scale Integration) circuits [4]. Memory plays an essential role in the design of electronic design where storage of data is required. The amount of memory required is depends on the type of application. The Semiconductor memory is classified according to the type of data storage and data access. Memory is classified into two types RAM (Read Only Memory) and RAM (Random Access memory). RAM storage is volatile it means that the information can be accessed only when the power is ON [5]. The RAM is again classified into two types: SRAM (Static Random Access Memory) and DRAM.

SRAM is static in nature and it has latch circuit to store each bit. SRAM cells are the main memory devices that are being used in the modern digital systems. It is more expensive and faster when compared to DRAM [10]. SRAM requires at least four to six transistors to store each bit of memory. Unlike DRAM data stored in SRAM need not to be refreshed periodically. So SRAM consume less power. SRAMs are mostly used in cache memories in mainframes, microprocessor. On the other hand DRAM is dynamic in nature and slower compare to SRAM [9].

DRAM requires only one capacitor to store the each bit of data, but the charge of the capacitor decreases with time. DRAM can hold more data than SRAM of same size of chip. But need to refresh the capacitor periodically dram consumes more power. The advantage of the dram is structure is simplicity [8] and it is used in high densities. DRAM is used in main memories in personal computers and in mainframes [7].

In modern day processor power dissipation plays a major role because of the miniaturization of the chip
design. So this stack technique can be used in future for reducing the power consumption. Further enhancement can also be made in the design in future to reduce the delay, because stacking of transistors increases delay and this DRAM cell can be used effectively. Since the cost and size of DRAM cells are less when compared to SRAM cells and power is the only major disadvantage of DRAM these optimized cells can be used to replace the SRAM cells for storage purpose.

In this paper, we have taken three different DRAM cells such as 1T1C,4T and 3T.Read and write operation for storing a single bit of memory have been designed in T-Spice Tanner EDA tool are made. The power consumption for the above mentioned DRAM cells and structures were compared in 250nm technology.

II. DIFFERENT DRAM CELL TYPES

DRAM is a type of volatile memory. Nowadays semiconductor memory is capable to store large data in small area. In past SRAM is more preferable as compared to DRAM because of its high speed operation, large noise margin and logic compatibility.

A. T1C DRAM Cell

The circuit diagram of a basic one transistor one capacitor cell structure used in modern DRAM devices to store a single bit of data.

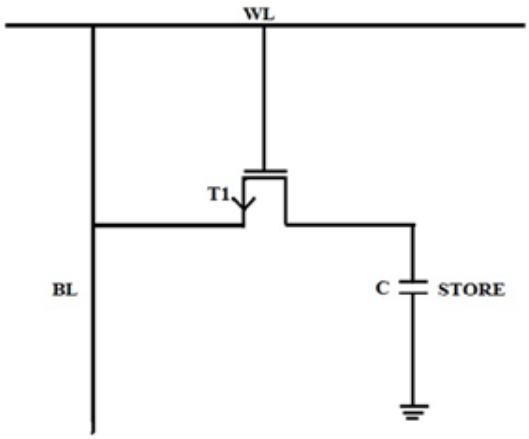

Fig. 1 1T1C DRAM Cell

In this structure, when the access transistor is turned on by applying a voltage on the gate of the access transistor [3], a voltage representing the data value is placed onto the bit line and charges the storage capacitor. The Storage capacitor then retains stored charge after the access transistor is turned off and the voltage on the voltage on the Word line is removed. However the electrical charge stored in the storage capacitor will gradually leak away with the passage away with the passage of time [11]. To ensure data integrity, the stored data value in the DRAM cell must be periodically read out and written back by the DRAM device in a process known as refresh. In the following section, the relationship between cell capacitance, leakage and the need for refresh operations.

B. Three-transistor DRAM Cell

It consists of 3 transistors and one capacitor. The information is stored in the charge form in parasitic capacitor. Transistors M1 and M3 acts as access transistors during write operation and read operations respectively. Transistor M2 is the storage transistor and is turned on or off, according to the amount of charge stored in capacitor c. Both read and write operations of 3T-DRAM cell proceeded in a two phase process [2].

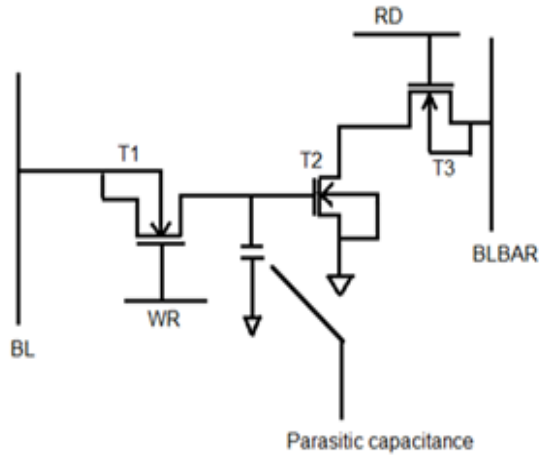

Fig. 2 Three-transistor DRAM Cell

The three transistor cell utilizes a single transistor as a storage device and one transistor for ‘read’ operation and other for ‘write’ operation. During the write operation the write signal is enabled and the data is fed into the T1 transistor. When data is to be read from the cell, read line is enabled and data is read through the bit line. 3T DRAM cell occupies less area compared to the 4T DRAM cell. The 3T1C cell structure has an interesting characteristic in that reading data from the storage cell does not require the content of the cell to be discharged onto a shared bit line. That is data reads to DRAM cells are not destructive in 3T1C cells [12].

C. Four transistor DRAM cell

The DRAM cell consists of four transistors. One transistor for write operation and other transistor for read operations [4].

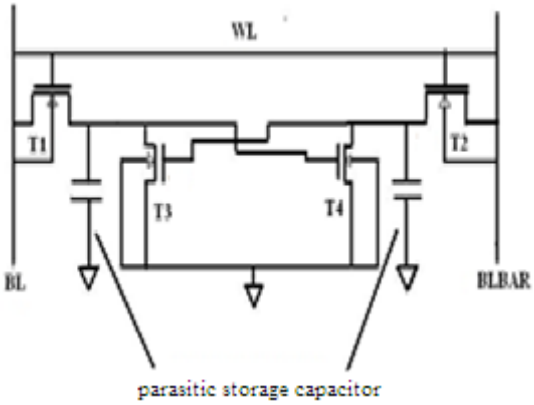

Fig. 3 Four Transistor DRAM Cell

In write operation the word line is enabled and data stored in the form of charge as a capacitance. There is no current path is provided to the storage node, hence data is lost due to leakage so the data need to be refreshed periodically. The read operation is non-destructive.

III. MEMORY ARRAY STRUCTURE DESIGNS USING DRAM CELLS

A memory array structure consists of a row decoder and column decoder to select a particular cell and to write on it [6].

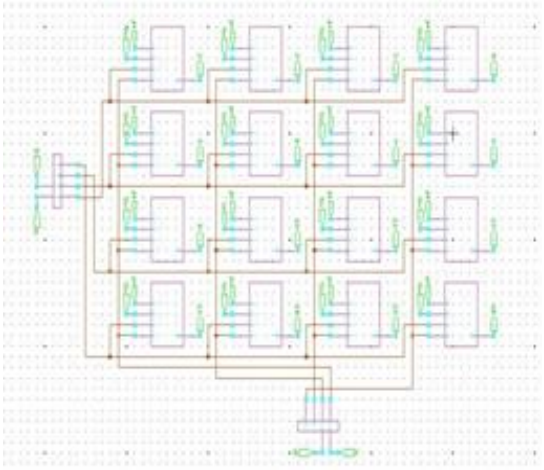

Fig. 4 Schematic of 4X4 Memory Array using 3T DRAM Cell

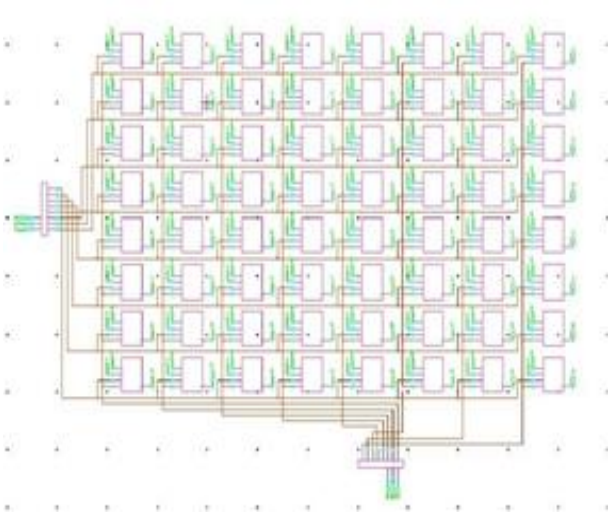

Fig. 5 Schematic of 8X8 Memory Array using 3T DRAM Cell

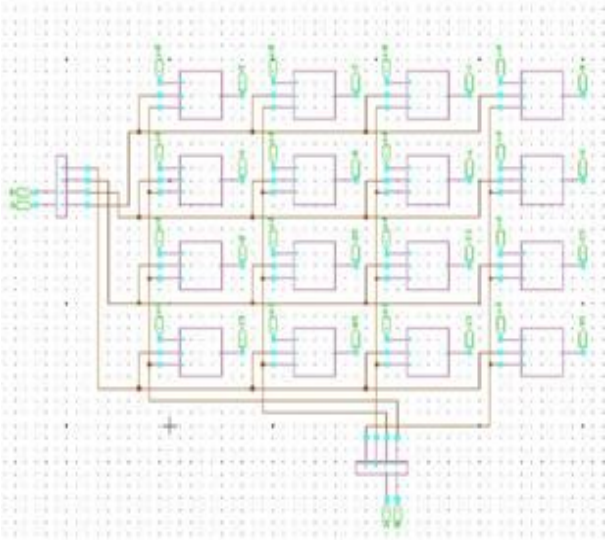

Fig. 6 Schematic of 4X4 Memory Array using 4T DRAM Cell

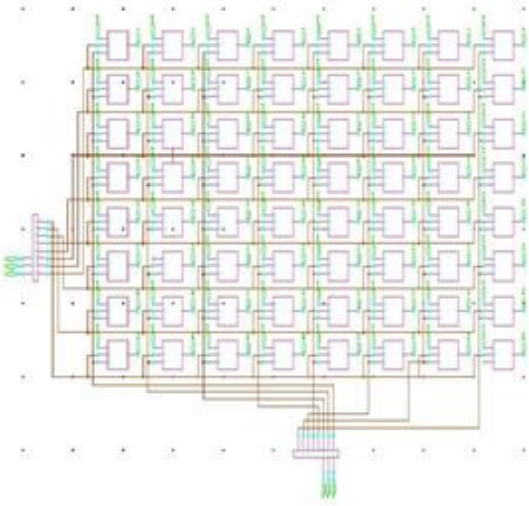

Fig. 7 Schematic of 8X8 Memory Array using 4T DRAM Cell

IV. SIMULATION RESULTS AND ANALYSIS

There are four inputs namely A, B, C, D and the output is v(2). For every supply voltages the power also changes for every input.

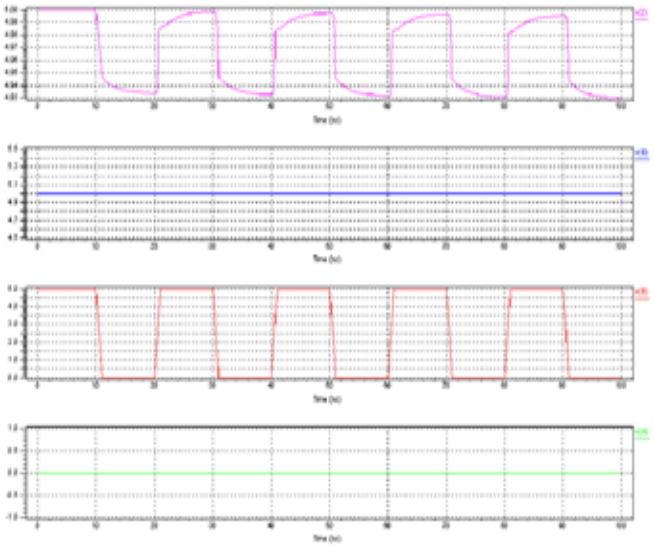

Fig. 8 Simulation Result for 4X4 Memory Array using 3T DRAM cell

There are Six inputs namely A, B, C, D, E, F and the output is v(28). For every supply voltages the power also changes for every input.

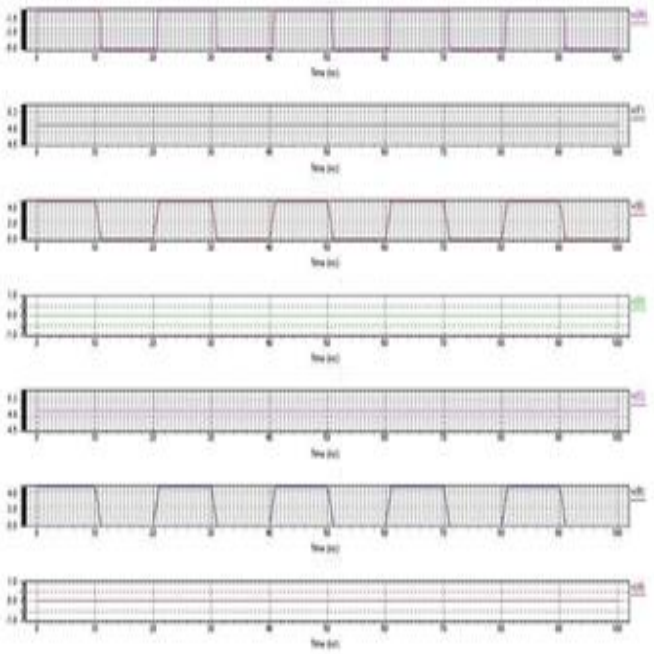

Fig. 9 Simulation Result for 8X8 Memory Array using 3T DRAM cell

There are four inputs namely A, B, C, D and the output is v (2). For every supply voltages the power also changes for every input.

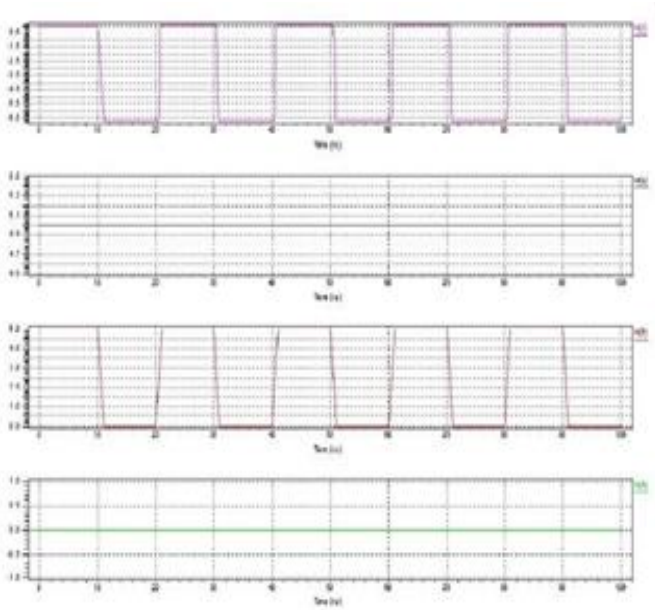

Fig. 10 Simulation Result for 4X4 Memory Array using 4T DRAM cell

There are Six inputs namely A, B, C, D, E, F and the outputs is v(28). For every supply voltages the power also changes for every input.

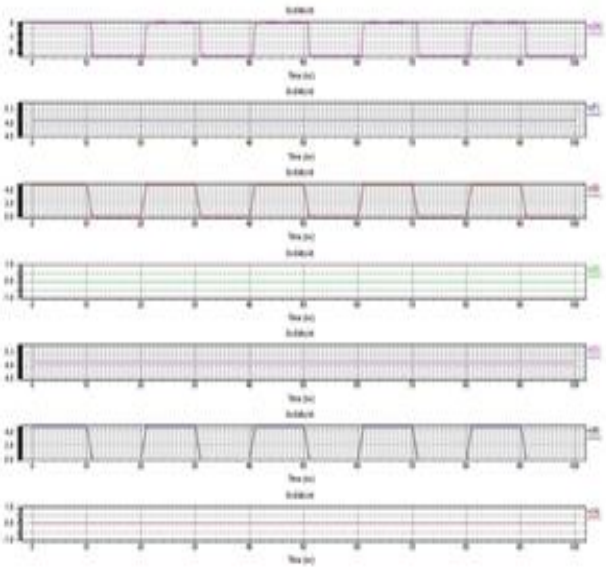

Fig. 11 Simulation Result for 8X8 Memory Array using 4T DRAM cell

The time period is given in x axis and the voltage is represented in y axis. The input value of (A) is given as (00) and (B) is given as (10) and (C) is given as (11) and (D) is given as (00) and (E) is given as (10) and (F) is given as (10) the output cell is selected.

The 3T DRAM cell is designed using TANNER EDA Tool and the power report for the design for different voltages has been tabulated.

TABLE 1.Power Result for 3T DRACells at Various Voltage Levels

Supply voltage (in volts)	**Existing 3T DRAM cell (in micro watts)**	**Proposed 3T DRAM using stack (in micro watts)**
3	0.921	0.787
3.5	1.219	0.799
4	1.573	0.821
4.5	1.78	0.839
5	1.953u	0.854

The table 1 shows the average power consumption of existing and proposed 3T DRAM cell using stack approach. The stack technique reduces the leakage power and thus the average power consumption of the 3T DRAM cell has reduced to a considerable extent.

TABLE 2.Power Result for 8X8 Memory Array Using 3T DRAM cells at various Voltage levels

Supply voltage (in volts)	**Existing 8x8 array using 3T DRAM cell (in mill watts)**	**Proposed 8x8 array using 3T DRAM (in mill watts)**
3	2.99	2.51
3.5	4.398	3.66
4	6.137	5.036
4.5	8.255	6.519
5	10.673	8.191

TABLE 3.Power Result for 4T DRAM Cells at Various Voltage Levels

Supply voltage (in volts)	Existing 4T DRAM cell (in micro watts)	Proposed 4T DRAM using stack (in micro watts)
3	1.40	0.92
3.5	1.85	1.22
4	2.39	1.57
4.5	3.02	1.98
5	3.03	1.75

The table 3 shows the average power consumption of 4T DRAM cell for the existing and proposed cell. Stack technique has been used to reduce the leakage power of the cell. Thus the overall power consumption of the cell is reduced.

TABLE 4.Power Result for 8X8 Memory Array Using 4T DRAM cells at various Voltage levels

Supply voltage (in volts)	Existing 8x8 array 4T DRAM using Cell (in milli watts)	Proposed 8x8 array using 4T DRAM (in milli watts)
3	2.18	1.74
3.5	3.236	2.36
4	4.52	3.35
4.5	6.07	4.43
5	7.40	5.43

It shows that the power consumption increases as array size increases. The average power consumption of the array structures have been reduced using the stack technique.

All the circuits have been simulated using BSIM 3V3 250nm technology on Tanner EDA tool with different voltage levels.

V. CONCLUSION

The DRAM cells have many advantage over sram cells. So it is important to analyse the power consumption of dram cells. So, we in this paper simulated 1T1C, 3T, 4T dram cells using TANNER EDA tool and made a comparative analysis of power consumption of these cells for different voltage levels. The power optimized DRAM cells is designed using three techniques sleep approach, stack approach and sleepy stack approach. In all techniques the power has been reduced considerably. But the area is increased because of the use of extra transistors but the power has been reduced. Although the power has reduced in all techniques, sleep approach shows the best result. But the drawback of this approach is that the data in the cell will be lost in ideal state. So it may not be the efficient approach. On comparing the other two approaches, the stack approach shows the best result. Thus the array structure for the 3T DRAM cell and 4T DRAM cell is designed using stack approach using TANNER EDA Tool in 250nmtechnology.

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