Design and Analysis of Low Power, High Speed 3-2 Compressor Architectures in 45-nm Technology

Bijoyendra Chowdhury
School of Electronics Engineering
KIIT University
Bhubaneshwar, India

Kanan Bala Ray
School of Eectronics Engineering
KIIT UNIVERSITY
Bhubaneshwar, India

Niladri Ghosh
School of electronics
KIIT UNIVERSITY
Bhubaneshwar, India

Sushanta K. Mandal
Department of Electronics and Communication Engineering,CUTM
Bhubaneshwar, India

***Abstract*---In this paper, various types of 3-2 compressor architectures have been designed and analysed. The required XOR and XNOR gate circuits have been constructed with pass transistor logicand mixed threshold voltage (MVT)as well as swing restoration technique adoption thatachieves low power with less number of transistor countsi.e. lower on chip area. The proposed compressor architectures are compared with the conventional CMOS configuration and 18T. The performances of the hybrid compressor architectures compared with MVT and swing restoration is found to be more efficient in the sphere of area, power as well asperformance.The simulation of the proposed designs has been performed in Cadence Virtuoso with 1 V supply.**

Keywords---Mixed threshold voltage (MVT) scheme, threshold voltage, low power, high speed, power delay product (PDP), Topology (T).

I. INTRODUCTION

The presentresearch interests ingrowing mobility and performance of small portable mobile devices, three important areas i.e. speed, area and power consumption are specially highlighted where speed has become one of themost serious issue in modern VLSI design as well as the leakage power reduction.

In respect to the multiplication algorithm, parallel multipliers are widely used to speed up the processors in respect to performance Compared to the serial multipliers [1]. There are two basic directions to improve the performance of the parallel multipliers, one is the Booth algorithm and the other is the Wallace tree compressors [2]. A basic Multiplier architecture concept can be separated into three parts, (1) partial product generation,(2) partial product accumulation stage and(3) final addition stage for getting the output.

Duringthe partial products accumulation stage in multipliers, large amount of power and delay are required as the higher order accumulation program demands higher order compressor circuit.More number of adders or compressors are involved to perform the partial product accumulation as higher order multiplications circuitsdemands more no of full adder and compressor circuits [3-4]. The numbers of adders are reduced simply by adopting different methodologies of higher order compressors in the complex multipliers. A basic 3-2 Compressor circuit is based on the concept of the counter of full adder. A higher order compressors circuit have four/five/six/seven inputs and two outputs as a basic 3-2 Compressor circuitry may be expressed as a one bit full adder circuit [5].The speed, area and power consumption of the multipliersare directly proportional to the efficiency of the compressor circuitry [6-7].

A basic 3-2 Compressor is defined as a single bit adder circuit that has three inputs as in full adder and two outputs. The proposed hybrid architectures(shown in section 4)contain the fact that both the XOR and XNOR logic are efficiently used to reduce the delay. To reduce the power consumption by using MVT and to improve the output swing by introducing swing restoration circuit are adopted in this work. The high Vt transistors are placed such a way that they are not in the critical path. Thus the time required for switching of the p-mos. and n-mos. transistors in the critical path is not extended.

II. MIXEDTHRESHOLD VOLTAGE (MVT)

In the case of mixed-Vth CMOS circuit, there can have various threshold voltages with definite process supress the transistors in the gates inside the transistors. There we take into account, two types of mixed-Vth CMOS circuit intention.For type one scheme (MVT1), there is neither any mixed Vth in pull-up nor in pull-down networks. For the other scheme (MVT2), mixed Vth is permittedeverywhereapart from the transistors connected in series as the transistors remainingin stack have the same threshold voltage is just because of the system estimation. As the threshold voltage of a transistor isdominated by

channel doping methodology, the transistors having stack, the channels remainveryintimate to each other which makes it very difficult to acquireexclusive channel doping. Hence, it is inflexible for getting separate threshold voltages for the transistors having stack. Audibly,multi-threshold-voltagescheme offers more benefits for the high thresholdaction in CMOS circuits than the gate-level dual threshold voltage (Dual Vth) concept.[8]- [9]

III. PROPOSEDDIFFERENT COMPRESSOR ARCHITECTURES (3-2)

The 3-2 compressor consists 3 inputs (x1, x2 and cin) and 2 outputs (Sum & Carry) i.e. a full adder. The input Cin is the output from the neighbouring lower significant compressor circuit. The combination of more 3-2 compressors construct higher order compressors as 3-2 is the basic building block of compressor shown in Fig.1.The Boolean expressions of a basic 3-2 compressor are as expressed below:

SUM out =A ⊕ B ⊕ Cin
CARRY out= (A ⊕ B).Cin + (A ʘ B).B

This work focuses on various types of 3-2 compressor topology.

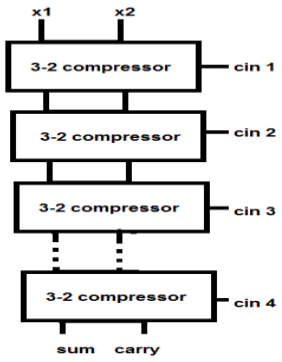


Fig: 1: Higher order compressor using 3-2 compressors.

A. Topology-1: 12T Architecture

A novel 12T 3-2 compressor has been presented here consisting 6 transistor XOR-XNOR circuitry for sum generation and pass transistor logics to form the carry shown Fig.2. Though the output of the sum delivers full output voltage swing but the output voltage of carry suffers from one threshold voltage drop i.e. VDD-Vtn as we have n-mos. pass transistors to form the carry which is non-ideal. This hybrid circuitry also suffers from static leakage power and overall power consumption but it has a strong impact on delay.

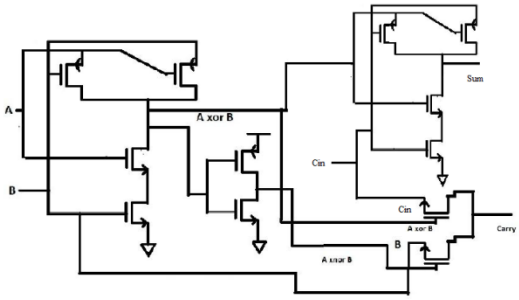


Fig: 2: Topology-1:12T Architecture

B. Topology-2: 12T Architecture with MVT

Mixed threshold voltage concept has been adopted here to reduce the overall power consumption and the leakage power shown in Fig.3. The high Vt transistors are exchanged with some low Vt transistors such a way, the previous critical path value doesn't hampered. Thus, the delay of the topology remains same as the previous topology delivers a compatible delay.

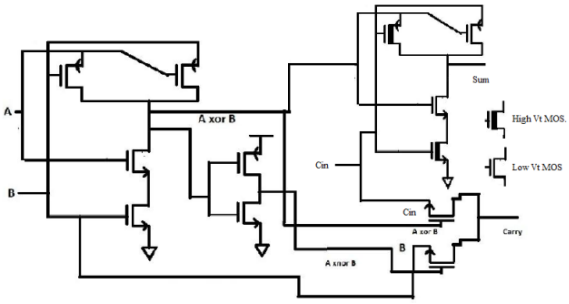


Fig: 3: Topology-212T Architecture with MVT

C. Topology-3: Swing Restoration Architecture

Though topology-1 delivers a favourable delay, there remains a very extensive problem in regard to output voltage swing in the carry output caused by the n-mos.pass transistor.
This problem can be solved by adding a swing restoration circuit instead of n-mos. pass transistors shown in Fig.4.

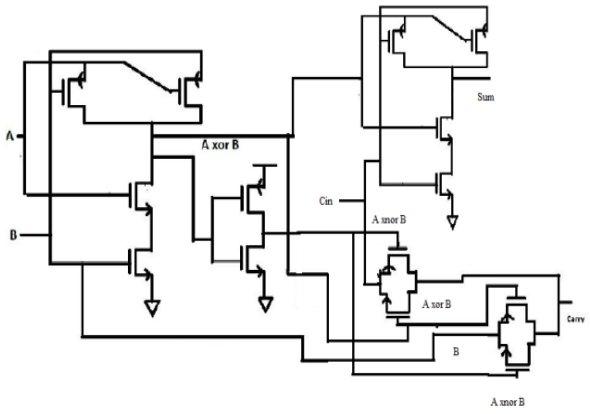


Fig: 4: Topology-3:14T Architecture

D. *Topology-4Swing Restoration Architecture with MVT scheme.*

In this new hybrid topology, delay as well as power related issues are made cleared as Topology-3 suffers from leakage power which is a big issue in deep submicron technologies by introducing MVT scheme in 14T (3-2 compressor) swing restoration topology shown in Fig.5.

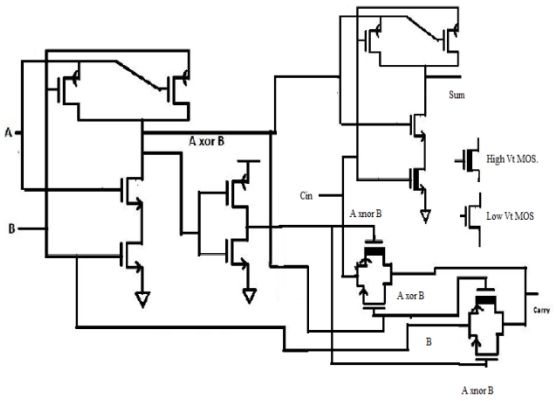


Fig: 5: Topology-414T Architecturewith MVT scheme.

IV. SIMULATION,PERFORMANCE ANALYZE AND REASUTS

The different compressor topologies have been simulated in Cadence Virtuoso platform using 45 nm Standard CMOS process technology. The circuit schematics are converted to respective layouts (shown in Fig.6, Fig.7. Fig.8 and Fig.9) with the help of Cadence LAYOUT XL window. The parasitic extraction has been performed to realize the post layout simulation. Both pre-layout and post layout simulations have been done under 1 volt power supply.
Here T1, T2, T3 and T4stand for Topology 1,Topology 2,Topology 3 and Topology4 respectively.

Table: 1 put forth on the topologies in terms of compactness and smaller on chip area.

Table: 1		
TOPOLOGY	***TRANSISTOR COUNT***	***AREA (in micron sq)***
T1	12	13.694
T2	12	13.714
T3	14	14.632
T4	14	14.739

Table: 2 Different topologies in terms of smaller delay.

Table: 2		
TOPOLOGY	*PRE-LAYOUT (In Pico Sec.)*	*POST-LATOUT (In Pico Sec).*
T1	97.53	94.21
T2	98.62	96.38
T3	97.89	94.55
T4	98.21	96.43

Table: 3 put forth on the topologies in terms of leakage power consumption.

Table: 3		
TOPOLOGY	*PRE-LAYOUT (Pico watt.)*	*POST-LATOUT (Pico watt.)*
T1	10.18	11.32
T2	6.26	7.18
T3	11.23	12.5
T4	7.44	8.6

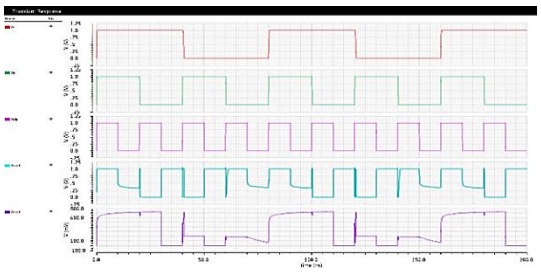
Table: 4 Average power consumption of different topologies.

Table: 4		
TOPOLOGY	*PRE-LAYOUT In Nano watt.*	*POST-LATOUT In Nano watt.*
T1	139.6	189.1
T2	116.5	138.9
T3	154.6	178.5
T4	112.6	136.04

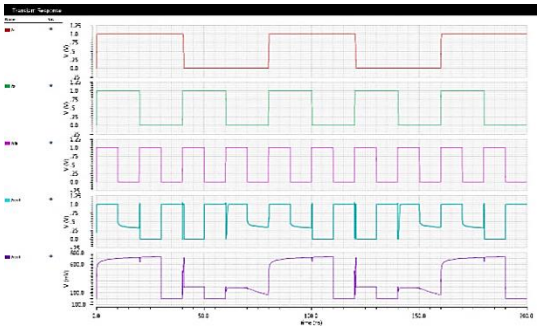
Table: 5 Power delay product of different of topologies.

Table: 5		
TOPOLOGY	*PRE-LAYOUT In (WATT-SEC)*	*POST-LATOUT In (WATT-SEC)*
T1	13.6×10^{-18}	17.8×10^{-18}
T2	11.5×10^{-18}	13.4×10^{-18}
T3	15.5×10^{-18}	16.8×10^{-18}
T4	11×10^{-18}	13.1×10^{-18}

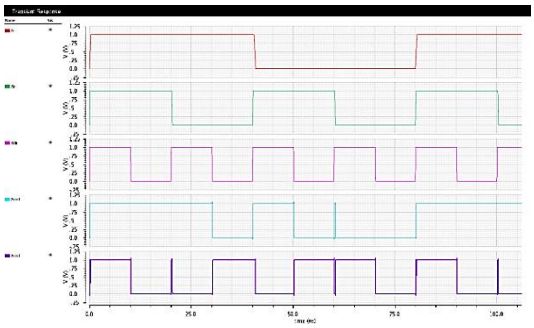
Though, all the topologies are more performance, area and power efficient than the conventional CMOS [10] and 18T [11] topologies shown in Table: 6. But there is a big issue in Topology 1 and 3regarding output voltage swing as shown in Graph 1 and Graph 3. There is also a big issue of leakage power in topology 1 and 2 shown in Graph 1 and Graph 3 because of lower threshold voltages and short channel devices. As far it is shown that Topology 4 provides significantly less leakage power as mixed threshold voltage is applied, full output swing as swing restoration circuit replaces the pass transistors,reduced dynamic power as the issues like short circuit power dissipation is reduced due to increase of threshold voltage and lesser delay as the MVT has not been used in critical path. The power-delay products of the post layout simulations are plotted against various temperaturesin Graph 6.



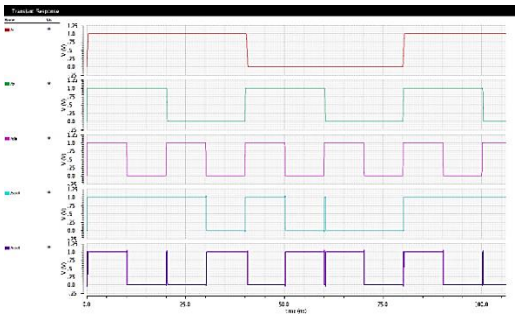
Graph 1: Output of topology 1



Graph 2: Output of topology 2



Graph 3: Output of topology 3



Graph 4: Output of topology 4

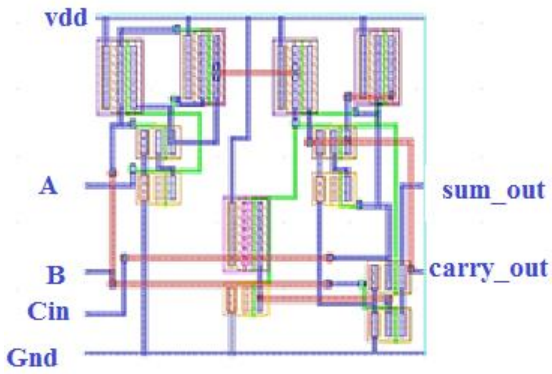


Fig: 6: layout of Topology 1

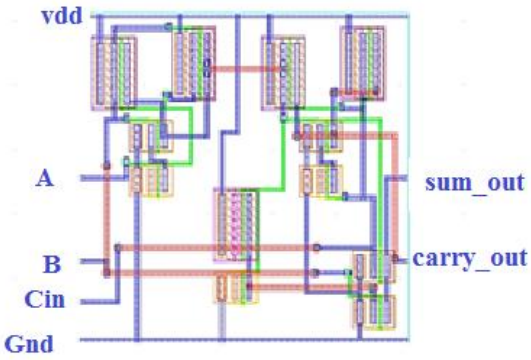


Fig: 7: layout of Topology 2

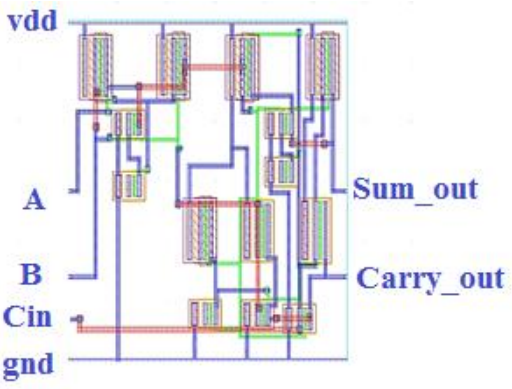


Fig: 8: layout of Topology 3

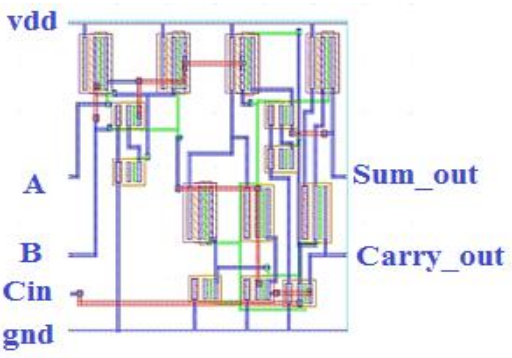
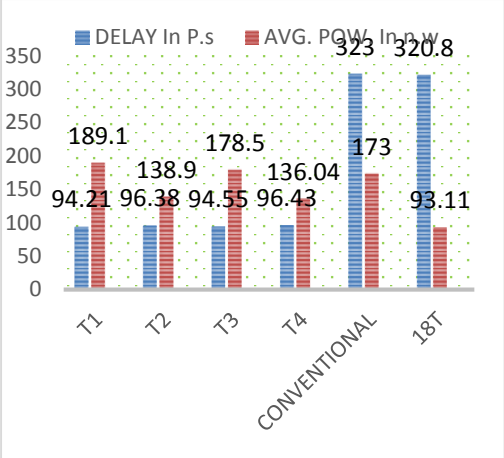


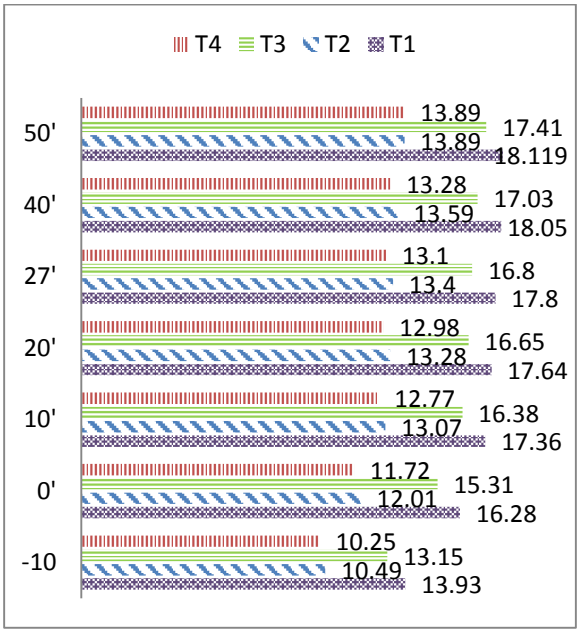
Fig: 9: layout of Topology 4

Table: 6 put forth on the topologies in terms of power and delay compared to CMOS and 18T.

Table: 6		
TOPOLOGY	*Propagation Delay (Pico Sec.)*	*Power consumption (Nano Watt.)*
Conventional [10]	323	173
18T [11]	320.8	93.11
T1	94.21	189.1
T2	96.38	138.9
T3	94.55	178.5
T4	96.43	136.04



Graph 5: Comparison of Delay and Power dissipation in various adder topologies.



Graph 6: Comparison of power-delayproduct (in Nano. Watt. Nano Sec)of different topologies product in various temperatures.

VII. CONCLUSIONS

This paper proposes 4 new topologies of 3:2 compressor which blooms with lesser on chip area, lesser power consumption and lesser delay. The simulation results claimthe effectiveness of the proposed hybrid topologies. Also the comparative study presented in Table: 6 and Graph. 5prove that the topologies can be efficient choice for low power high speed higher compressor design.

VII. ACKNOWLEDGMENT

I would like to express my gratitude to all the co-authors who gavemethe possibility to complete this work. A special thanks to my guide, Mrs.Kananbala Ray, whose encouragement, helped me to coordinate my work.

REFERENCES

[1]. S.Karthick1, S.Karthika2, S.Valarmathy"DESIGN AND ANALYSIS OF LOW POWERCOMPRESSORS" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 1, Issue 6, December 2012.
[2]. S. Veeramachanemi, K. Krishna, L. Avinash, S.R. Puppola and M.B. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2Compressors," IEEE Proc. OjVLSlD '07, pp. 324-329, 2007.
[3]. [S. F. Hsiao, M. R. Jiang, and J. and S. Yeh, "Design of high speed low-power 3-2 counter and 4-2 compressor for fast multipliers," Electron. Lett, vol. 34, no. 4, pp. 341–343, 1998.
[4]. H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR–XNOR gates," IEEE Trans. Circuits Syst. II, vol. 49, pp. 25–30, Jan. 2002.
[5]. R. Zimmermann and W.Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid- State Circuits, vol. 32, pp. 1079–1090, July 1997.
[6]. Nabihah Ahmad and RezaulHasan, "A New Design of XOR-XNOR gates for low power application", IEEE conf, ICEDSA, 2011.
[7]. Hung Tien Bui, A.K. Al-Sheraidah, and Yuke Wang, "New 4-transistor XOR and XNOR designs," in Proceedings of the Second IEEE Asia Pacific Conference on ASICs, 2000, pp.25-28.
[8]. S. Mutoh, et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS",IEEE Journal of Solid-State Circuits, Vol. 30, No. 8, pp. 847-854, 1995.
[9]. Liqiong Wei, Zhanping Chen, and Kaushik Roy, "Mixed-Vth (MVT) CMOS Circuit Design Methodology for Low Power Applications", Design Automation Conference, 36th proceedings, pp. 430-435, 1999
[10]. Raju Gupta, SatyaPrakashPandey and ShyamAkashe, "Comparative Analysis and Optimization of Active Power and Delay of 1-Bit Full Adder at 45 nm Technology" 978-1-4673-5630-5//13/$31.00 ©2013 IEEE
[11]. SubhramitaBasak, DipankarSaha, Sagar Mukherjee, SayanChatterjee and C. K. Sarkar," Design and Analysis of a Robust, High Speed, Energy Efficient 18 Transistor 1-bit Full Adder Cell, modified with the concept of MVT Scheme"2012 International Symposium on Electronic System Design.