International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 3 Issue 12, December-2014

Design and Analysis of Low Noise Amplifier for ISM Band

Mr. T. Rubesh Kumar
Assistant Professor
Prathyusha Institute of Technology And Management
Chennai, India.

Ms. S. Inbalakshmi
Assistant Professor
Prathyusha Institute of Technology And Management
Chennai, India.

Ms. C. T. Melfa Steffy
Second year M.E.
Prathyusha Institute of Technology And Management
Chennai, India.

Abstract- **In this paper we have designed and analyzed a low noise amplifier (LNA) for ISM band at 2.4 GHZ frequency. This proposed amplifier uses GaAs FET transistor which has low noise and was a high electron mobility transistor, and also provides good input and output matching. The design simulation was done using Advance Design Simulation (ADS) software. At 2.4 GHZ frequency the designed amplifier gives a noise figure (nf) of 0.21dB, input return loss (S11) of -21.49 dB and output return loss (S22) of -21.26 dB.**

Keywords: Low Noise Amplifier, Advance Design System, high electron mobility transistor, noise figure

I. INTRODUCTION

An electrical device which is used to boost the desired signal power received at the front end of the communication system, while adding little noise and distortion as possible is called low noise amplifier. Low noise amplifier is placed as a first component of the receiving system. The noise figure of all following stages in the receiving system is reduced by providing a low noise amplifier with high gain and low noise figure, thus it provides enough amplification and minimum degradation of signal-to noise ratio (SNR).

Low noise amplifier are widely used in a variety of applications such as RF communication systems, cellular telephone, two way radio, personal digital assistant (PDA), Bluetooth devices with other communication systems. Low noise amplifiers are used in many systems where low-level signals must be sensed and amplified.

In LNA design it is necessary to compromise its simultaneous requirements for high gain and low noise figure, stability, good input and output matching. The proposed low noise amplifier design is carried out with a systematic procedure and simulated by Advanced Design Systems (ADS) designed by Agilent.

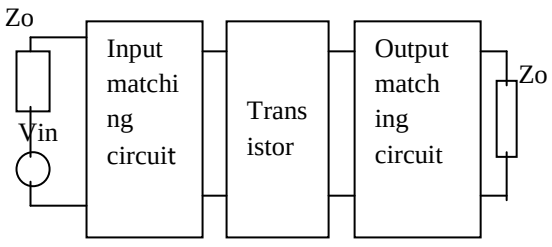

Fig1. Block Diagram of single stage LNA

A. Transistor Selection

In this paper, GaAs FET transistor has been chosen for designing the low noise amplifier. Gallium arsenide is preferred over silicon due to its superior performance at microwave frequencies. It has low noise

II. LNA DESIGN

In the designing of low noise amplifiers, the important goals are minimizing the noise figure of low noise amplifier, producing higher gain, lower power consumption and providing good input and output matching.

and was a high electron mobility transistor. Before using the transistor must be biased at appropriate operating point. So that, it can work under required values and achieve less power consumption.

B. Noise Figure

Noise can be characterized as any undesired signal that interferes with the main signal to be processed. Noise in electronic components is caused by random thermal fluctuations of electrons. Noise figure is commonly used to define extra noise generated by the circuit or system. It can also said that, the ratio between SNR at input to the SNR at output, and is expressed in decibels. It is expressed by following equation.

$$NF = 10 \log \frac{SNR_{in}}{SNRout} \text{ in dB} \quad (1)$$

Where,

NF= Noise figure

SNR_{in}= Signal to Noise ratio at the input of the circuit or system

SNR_{out}= Signal to Noise ratio of the circuit or system at output

C. Gain

The gain of the device is its ability to amplify the amplitude or power of the input signal. It is defined as the ratio of output to input signal and is often expressed in decibel. The general transducer gain (G_T) of a two port network having S21 & S12 values, is

G_T= Power delivered to load / Power available from source

In terms of s-parameters, transducer gain (G_T) is given by,

$$G_T = [(1- | \Gamma s | 2) /(|1-S11 \Gamma s| 2)] [|S21| 2] [(1- |\Gamma_L| 2) / (| 1-S22 \Gamma_L | 2) \quad (2)$$

If S12=0, then Γ_{IN} = S11 and Γ_{OUT} = S22 and transducer gain becomes the unilateral gain.

Overall gain (in dB) of the transistor

$$G_{TU} (dB) = G_S (dB) + G_O (dB) + G_L (dB) \quad (3)$$

D. Input and Output Return Loss

Input return loss indicates the mismatch between the input impedance of an amplifier and the characteristic impedance of the transmission line at its input by acting as a measure of the amount of power reflected back when an input signal is injected into the input of the amplifier through the transmission line.

Input Return Loss = -20 log |S11| (4)

Output Return Loss = -20 log |S22| (5)

E. Stabilizing Techniques

By introducing some resistive feedback at input side and resistive loading at output side, the designer can stabilize the amplifiers. Disadvantage to this technique is that it fails for designing low noise amplifier because the resistive terminations introduce some extra noise to the amplifier. In such cases the stabilization is done by providing inductors in emitter or source side, as the inductors are noiseless devices.

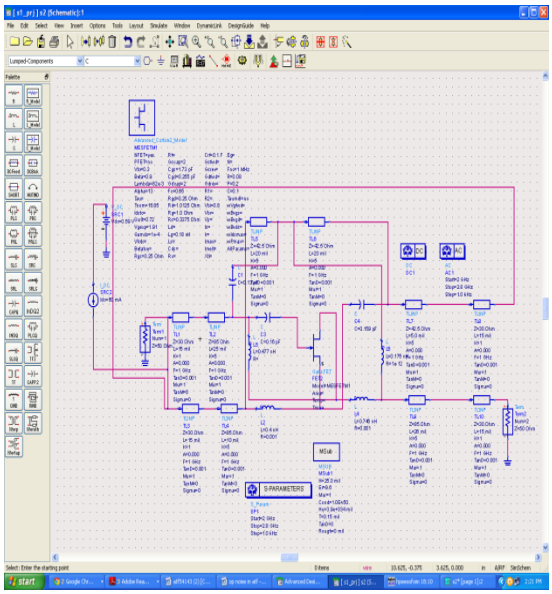

Fig2. Schematic diagram of LNA

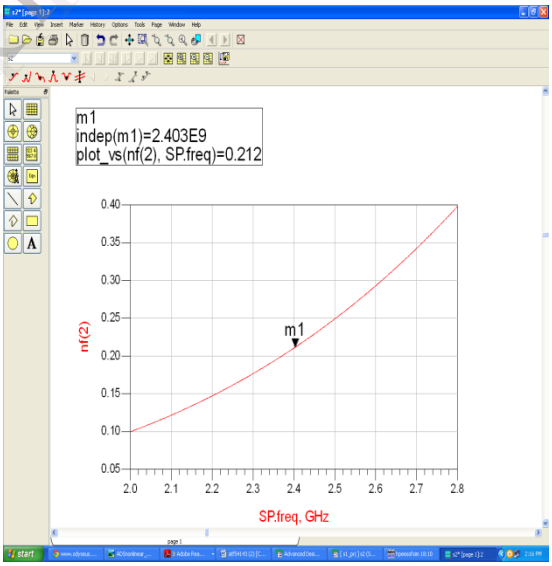

Fig3. Noise Figure

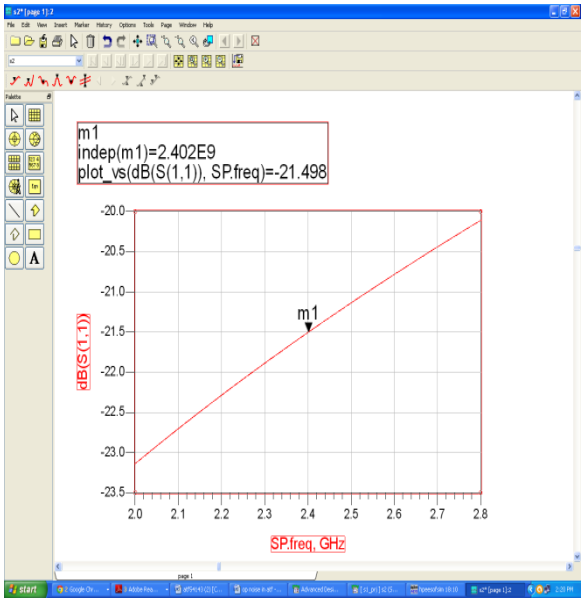

Fig4. Input Return Loss

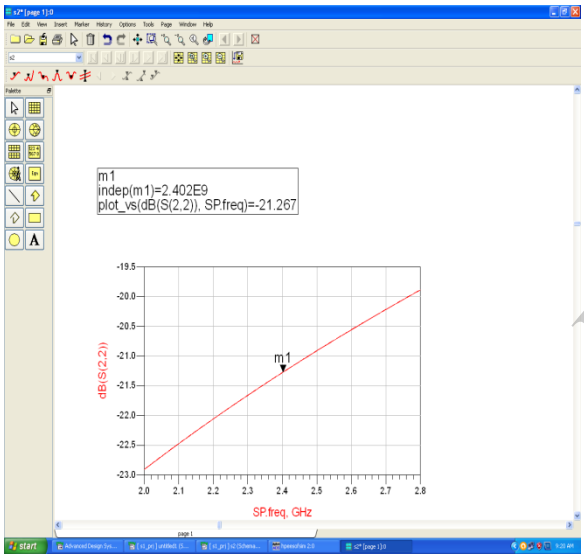

Fig5. Output Return Loss

III. SIMULATION RESULTS AND DISCUSSION

The simulation result for the proposed low noise amplifier is shown in below figures. The designed low noise amplifier provides a noise figure (NF) of 0.21 dB, input return loss (S11) of -21.49dbdB and output return loss (S22) of -21.26 dB for 2.4 GHZ frequency

IV. EXPECTED OUTCOME AND FUTURE WORK

In this paper, the low noise amplifier is designed to meet the following specification

1. Frequency: 2.4 GHZ
2. Supply Voltage: 3V
3 .Drain Current: 60mA
4. Noise Figure: 0.212dB
5 .Input Return Loss: -21.49dB
6. Output Return Loss: -21.26 dB

We have achieved 75% of the desired result in the low noise amplifier for its gain. The design of amplifier will be further improved in our future work.

REFERENCES

1) Avago Technologies datasheet,"ATF-54143 Low noise enhancement mode pseudomorphic HEMT in a surface mount plastic package,"avago technologies, USA, tech AV01 - 0602EN august 5, 2008.
2) G.Gonzalez (1997)," Microwave transistor amplifier: analysis and design", 2nd edition, upper saddle river, NJ:prentics - hall inc. 217, 294-303.
3) Yazid Mohamed, Norsheila fiscal and Mazlina Esa,"Simulation study of broadband LNA for software radio applicaion"june 2000.
4) Joseph C, Bardinand, Sander Weinreb," A 0.1 GHz to 5 GHz cryogenic SiGe MMIC LNA,"ieee microwave and wireless components letters, vol.19,no.6, June 2009.
5) Viranjay M.Srivasava, K.S. Yadav, and G.Singh,"Analysis of double gate cmos for double pole four throw RF switch design at 45nm technology." J of computational electronics, vol.10, no.1-2, pp.229-240, june 2011.
6) Viranjay M.Srivasava, K.S. Yadav, and G.Singh,"Design and performance analysis of double gate mosfet over single gate mosfet for RF switch, "microelectronics journal, vol.42, no.3, pp.527-534, march 2011.
7) M.E.kaamouchi, M.S.Moussa, P.Delatte, G.Wybo, A.Bens, J.P.Raskin," A 2.4 GHz fully integrated ESD protected low noise amplifier in 130nm PD SOI CMOS technology," ieee trans. Microwave theory tech., vol.55, pp.2822-2831, Dec 2007.
8) A.V.Do, C.C.Boon, M.A.Do, K.S.Yeo, and A.Cabuk," A subthreshold low noise amplifier optimized for ultra low power applications in ISM band, " ieee trans.microwave theory tech., vol.56, pp.286-292, feb 2008.
9) M.Cimino, H.Lapuvade, Y.Deval, T.Taris, and B.Begueret, " Design of a 0.9 V 2.45 GHZ self-testable and reliability-enhanced CMOS LNA," IEEE J. solid state circuits, vol. 43, pp. 1187-1194 may 2008.
10) Ashwini L. Dharmik. Dr. A.Y. Deshmukh, Prof. Sanjay Tembhurne. (2014) "Design cmos low noise amplifier for 2.47 GHz frequency at 0.18µm technology" International journal of pure and applied research in engineering and technology Vo 2 No. 8, pp. 48-58.