

# Design and Analysis of Error Tolerant Adder for Different Bits

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**Abstract**— The objective of this paper is to design Error Tolerant Adder (ETA) of multiple bits and to compare its performance in terms of speed, power and area. As the scale of integration keeps growing more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consumes considerable amount of energy. Performance parameter such as speed, power and area are the major design issues. By adopting an ETA in place of conventional adder, the power consumption, area of the adders can be reduced and computation speed of the adders can be enhanced.

**Keywords:** Adder, VLSI, Low power, Cadence.

## I. INTRODUCTION

The demand for low power adder cores has been on the rise during years. These units are essential building blocks of microprocessors and digital signal processor data paths since hardware implementation of addition involves the realization of multitude of distinct data processing subunits that endure a series of power consuming traditions during the course of their operations, the power consumption of adders are in general quite significant in comparison to that of their integer counterparts, owing to the presence of a relatively high traffic of additions in microprocessors and digital signal processors, the power/performance implications of adders directly impact the power/performance desirability of the target applications. Addition is believed to be the most frequent computer arithmetic operation, also the other operations such as the subtraction, multiplication and division can be derived from addition and hence adders are often seen as the most significant part of arithmetic unit.

Increase in demand for the high fidelity portable devices has laid emphasis on the development of low power and high performance systems. In the next generation processors, the low power design has to be incorporated in to fundamental computation units, such as adders. The characterization and optimization of such low power adder will aid in comparison and choice of adder modules in system design.

The need for low-power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, larger currents have to be delivered and the heat due to larger power consumption must be removed by proper cooling technique. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices.

Addition is a fundamental operation in most signal processing algorithms. Adders have a larger area, long latency and consume considerable power. Therefore low power adder design has been an important part in low-power VLSI system design. There has been extensive work on low-power adders at technology, physical, circuit and logic levels. A systems performance is generally determined by the performance of adder because the adder is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the adders is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, a whole spectrum of adders with different area, speed constraints has been designed with fully parallel. Existing conventional adders are no longer suitable for larger adders because of its low-speed performance.

## II. ERROR TOLERANT ADDER

Architecture of the error tolerant adder is shown in the figure 2. This is the most straight forward structure consists of two parts an accurate part and inaccurate part. The accurate part is constructed using the conventional adder such as the ripple carry adder. The carry-in of this accurate part is connected to ground. The inaccurate part constitutes of two blocks a carry free addition block and a control block. The control block is used to generate the control signals to determine the working mode of the carry-free addition block.

## III. DESIGN OF ACCURATE AND INACCURATE PART

Ripple carry adder is used for addition logic in the accurate part. Hence each bit gets rippled in to the next stage. In a ripple carry adder the sum and carryout bits of any half adder stage is not valid until the carry in of the stage occurs. The propagation delay inside the logic circuitry is the reasons behind this, propagation delay is the time elapsed between the application of an input and occurrence of the corresponding output. The construction of 4 bit ripple carry adder using PG logic is shown in figure3.1. Each block of the ripple carry adder is designed using the 28 transistor the construction is depicted in the figure 3.2.

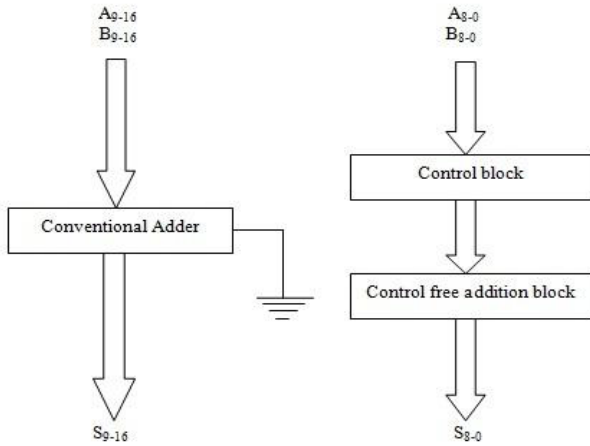


Figure 2. Architecture of ETA

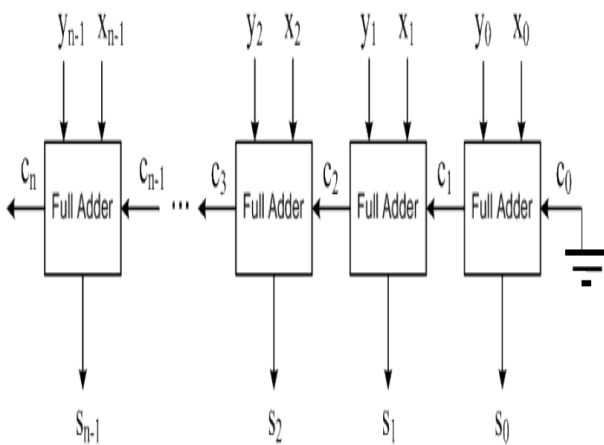


Figure 3.1 Ripple carry adder

Carry generation(G) and carry propagation(P) signals in ripple carry adders are used to describe whether a group of spanning bits  $i \dots j$  inclusive, generate a carry or propagate carry as the P and G signals will have already stabilized by the time the carry arrives. The critical path of the carry ripple adder passes from carry in to carry out along the chain majority gates.

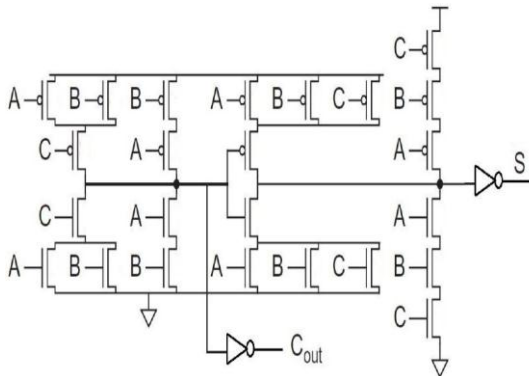


Figure 3.3 28 transistor full adder

$$G_{i:j} = G_{i:k} + P_{i:k} * G_{k-1:j}$$

$$P_{i:j} = P_{i:k} * P_{k-1:j}$$

The critical path delay of the ripple carry adder can be calculated by

$$t_{ripple} = t_{pg} + (N-1) t_{AO} + t_{xor}$$

The working principle of the inaccurate part consists of control logic. The control logic enables the OR operation if its value is zero or else disables the OR operation if its value is one and makes the output to go a logic high. The construction of the control logic is shown in the figure 3.3. The aspect ratio of the PMOS transistor M3 should be varied to attain a proper high state.

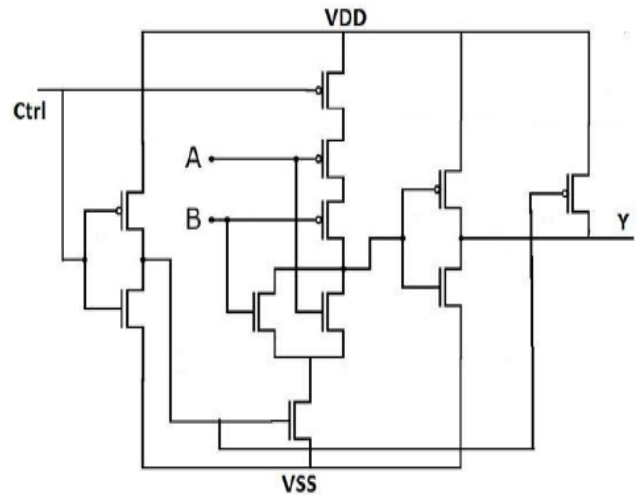


Figure 3.3 Control logic

The individual addition of the inaccurate part is fed to the control logic. This CTL input controls the output of the carry free addition block of the inaccurate part. When both the bits or either of the bits are low, then CTL remains low and CTL is set to logic high when both the bits goes high there by making the output high for any input that comes after the bits that produced high. The truth table of the modified OR logic is shown in table 1.

Table 1: Modified OR logic

Inputs			Output
Ctrl	A	B	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	1	0	1
1	1	1	1

#### IV. RESULTS

Error tolerant adder is designed for 8, 16, 32 bit number the power consumption, delay and area for the adder are tabulated in table 2. Power consumption, area and delay of the Error Tolerant Adder increases with increase in number of bits.

Table2: Result table

Number of bits	Power(nw)	Delay (ps)	Area
8	1.34	152.7	182
16	4.53	259.7	396
32	5.49	365.5	804

#### V. SIMULATION OUTPUT

Transient analysis, DC analysis of 8, 16, 32 bit adder was performed and the waveform of 8 bit are displayed in the figures 5.1 and 5.2 respectively.

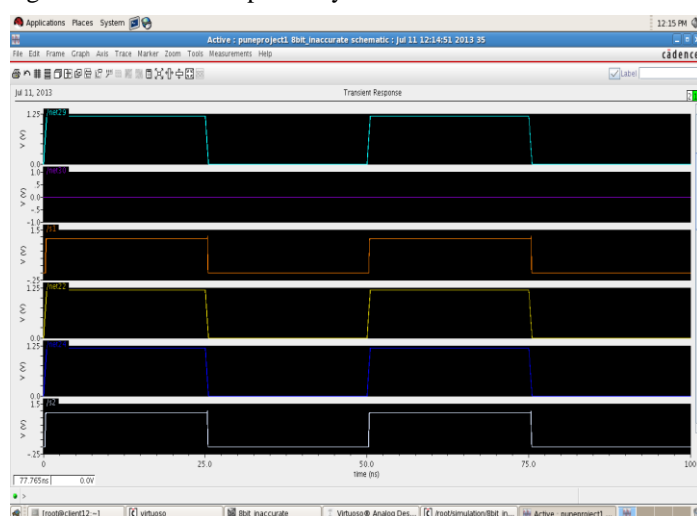


Figure 5.1 Transient analysis

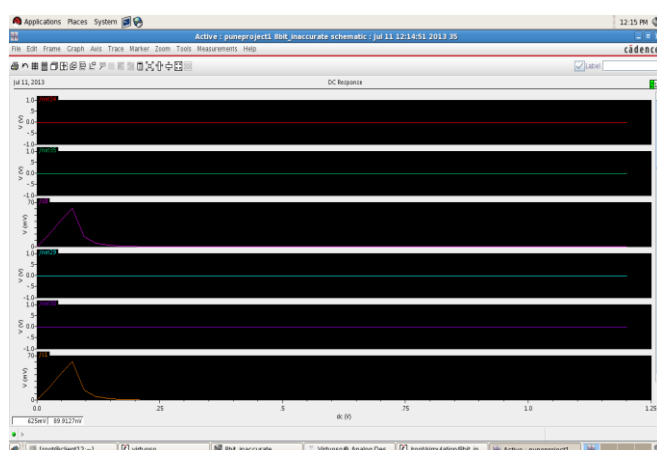


Figure 5.2 DC analysis

#### VI. CONCLUSION

The error tolerant adder is designed using the cadence tool (IC 6.1.4.500.12) in 45nm technology. The performance parameters such as speed, delay increases with increase in number of bits. A great achievement can be obtained if the adder is designed using 18nm technology. The designed ETA can be used in DSP applications where accuracy is not a major concern and speed of operation is important.

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