Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 04, April-2025

Design and Analysis of Double-Gate P-N-I-N Tunnel Field Effect Transistor

Syed Ashruf, Katepally Veerabhadhra Vijay, Nikhil Sai Kanolla,
Graduate Student Member,

Gotam Ravi Lokesh, Vuyyuru Ramtej
Prof. Dept. of ECE
Electronics and Communication Engineering,
Koneru Lakshmaiah Education Foundation (Deemed to be University),
Vaddeswaram, Guntur, Andhra Pradesh, India

ABSTRACT

This research study focuses on examining the influence of incorporating a narrow n-layer within the tunnelling junction of the p-i-n Tunnelling Field-Effect Transistor (TFET) as a potential solution to enhance device reliability in the presence of intense electric fields. Utilizing technology computer-aided design simulations, the effectiveness of this modification in transforming the device into a p-n-i-n TFET is demonstrated. Results show not only an improvement in the drive current, consistent with previous findings, but also an overall enhancement in reliability. A comparative analysis with the conventional p-i-n TFET highlights several advantageous properties of the p-n-i-n TFET, including higher ON-current, reduced, improved lower OFF-current, and higher drain current.

***Keywords*: p-i-n Tunnelling field-effect transistor (TFET), p-n-i-n tunnelling field-effect transistor (TFET), Reliability enhancement, Quantum tunnelling, Low-power operation, High switching speeds, Performance improvement**

I. INTRODUCTION

Ensuring the long-term reliability of tunnelling field-effect transistors (TFETs) is a critical factor for their successful integration into diverse electronic devices[7]. [4]TFETs offer attractive features such as low power consumption and a high on/off current ratio, making them highly desirable for next-generation integrated circuits[1]. However, guaranteeing their durability over extended periods presents a notable obstacle. This study focuses on addressing the reliability concerns of TFETs by utilizing the p-n-i-n (p-type/n-type/intrinsic) structure[17-18]. The p-n-i-n architecture presents unique opportunities to enhance device performance and stability[16]. By incorporating this structure, it becomes feasible to improve the reliability of TFETs and extend their operational lifespan. Various techniques and design optimizations are investigated in this study to enhance the reliability of p-n-i-n TFETs[2]. The impact of different parameters, including doping profiles, material choices, and device geometries, on reliability performance is analyzed. The objective is to identify strategies that alleviate reliability issues such as hot carrier effects, aging effects, and process variations, which can degrade device performance over time. The aim of improving TFET reliability is to contribute to the development of dependable and durable electronic devices. The findings presented in this study will enable engineers and researchers to design TFET-based circuits with enhanced reliability, facilitating the widespread adoption of these transistors in future technology applications[9-15].

II. THE STRUCTURE AND SPECIFICATIONS OF THE PROPOSED DEVICE

Figure 1 depicts the schematic structure of the P-N-I-N Tunnel Field Effect Transistor (TFET) designed for low-power and high-frequency applications. Where energy efficiency, reduced power consumption, and enhanced performance are critical design considerations. The proposed device aims to increase the electric field by introducing a thin heavily doped n+ region between the P and intrinsic regions. In this p-n-i-n structure, the gate work function is 4.17 eV. The electrodes on the ultrathin silicon film, which include the induced source and drain (S/D) regions in the device, have an appropriate metal work function. The source region is "p+" type and is formed within the intrinsic silicon using a metal electrode with a work function of 4.4eV, generating a majority of positive charge carriers (holes) on the source side.

Similarly, thin "N+" region is formed with in the intrinsic silicon using a metal electrode with a work function of 4 eV. On other hand, the drain region is "n" type and is formed within the intrinsic silicon substrate using metal electrode with a work function of 4eV, creating a majority of negative charge carriers (electrons) on the drain side.

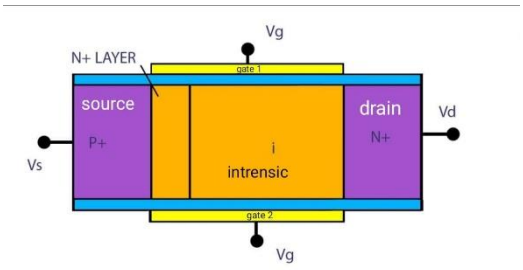


Fig.1: Schematic view of the proposed Device with p-n-i-n region.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 04, April-2025

Table 1. The dimensions and parameters used in simulation of the proposed device

Parameters	Values
Device Length	28nm
Thin N+ Layer thickness	2nm
Thickness of oxide	2nm
Thickness of channel	20nm
Length of source and Drain	20nm
Doping levels of source	$5x10^{19}$
Doping levels of Drain	$5x10^{19}$
Doping level of N+ thin layer	$5x10^{18}$
Work function of Gate	4.17

The device under study possesses specific specifications, including a device length of 28nm, a thin N+ layer thickness of 2nm, an oxide thickness of 2nm, and channel thickness of 20nm. The source and drain regions have a length of 20nm each. The doping levels of both the source and drain are 5x10^19, while the N+ thin layer has a doping level of 5x10^18. The gate's work function is 4.17. These parameters define the dimensions, doping levels, and work function of the device, which significantly influence its behavior and performance.

The investigation focuses on studying the characteristics of a reference device utilizing double-gate p-n-i-n TFET structure, as illustrated in Figure 1[3,23]. This device differs from the conventional p-i-n TFET as it incorporates a thin n-layer at the p-i tunneling junction. The gate dielectric used in the device is a SiO2 layer.[19]. The simulation is carried out based on the parameters provided in Table I, which further define the properties and configuration of the device.

III. NUMERICAL SIMULATIONS

In our study, we conducted an investigation utilizing Silvaco Atlas for simulations on the proposed p-n-i-n Device[6,21]. The purpose was to determine the recombination tunnelling generation rate by employing the BTBT model[24-26]. To ensure accurate results, we implemented a highly refined meshing technique specifically around the source-body junctions. Additionally, we incorporated concentration dependent mobility and electric field dependent mobility models to account for nonlinear effects in charge carrier motilities. Throughout the analysis conducted in our research, a constant supply voltage of 1V was maintained.

IV. RESULTS AND DISCUSSIONS

CASE: - 1

We have observed the comparison between p-i-n TFET and p-n-i-n TFET exhibits different responses to Drain Current with respect to the gate voltage (v).

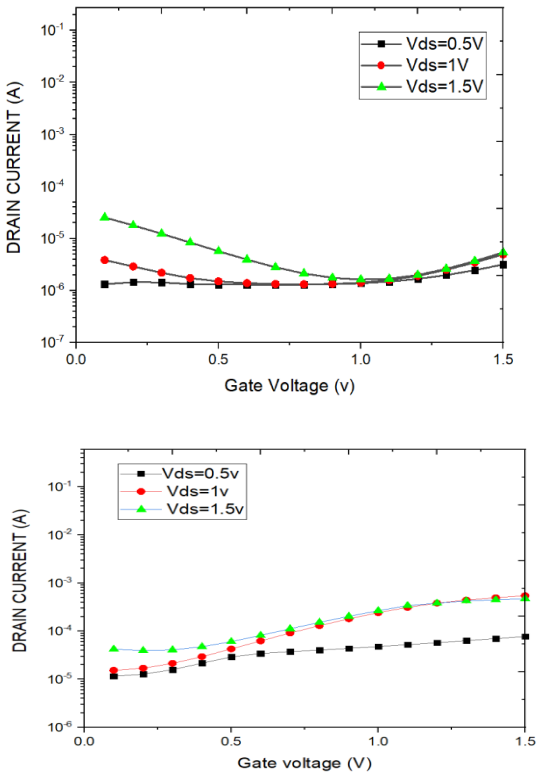


Fig.1. Transfer characteristics for (a) p-i-n TFET and (b) p-n-i-n TFET at Vd=0.5v,1V and 1.5v

Upon analyzing Figure 1(a), we observed the Transfer characteristics for the drain current for the p-i-n TFET at different drain voltages (Vd) including 0.5V, 1V, and 1.5V. At Vd=0.5V, the p-i-n TFET displayed an on-current (I(on)) of $1.32x10^{-06}$ and an off-current (I(off)) of $3.16x10^{-06}$. At VD=1V, the I (on) was measured as $3.84x10^{-06}$, while the I (off) was $4.93x10^{-06}$. Furthermore, for Vd=1.5V, the p-i-n TFET exhibited an I(on) of $2.54x10^{-05}$ and an I(off) of $5.42x10^{-06}$[22].

Figure 1(b) illustrates the transfer characteristics of the drain current for p-n-i-n TFET at the same drain voltages: 0.5V, 1V, and 1.5V [8]. Upon analyzing the graph, it can be observed that at Vd=0.5V, the p-n-i-n TFET demonstrated an I(on) value of $1.16x10^{-05}$ and an I(off) value of $7.77x10^{-05}$. For Vd=1V, the p-n-i-n TFET exhibited an I(on) value of $1.53x10^{-05}$ and an I(off) value of 5.46x10-04. Finally, at Vd=1.5V, the p-n-i-n TFET displayed an I(on) value of $4.23x10^{-05}$ and an I(off) value of $6.11x10^{-04}$.[2]

Through a comparative analysis of Figure 1(a) and Figure 1(b), we investigated the transfer characteristics of the p-i-n TFET and the p-n-i-n TFET. Our examination of drain current in both devices unveiled a notable disparity, with p-n-i-n TFET exhibiting significantly higher drain current compared to the p-i-n TFET. These findings align with previous studies highlighting the enhanced performance of p-n-i-n TFET attributed to incorporation of thin n-type

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 04, April-2025

layer.The inclusion of this layer amplifies the device's drive current capabilities, positioning the p-n-i-n TFET as a promising contender for high-performance applications[9-15].

TABLE-1: Performance Parameters of p-i-n Structure of TFET:

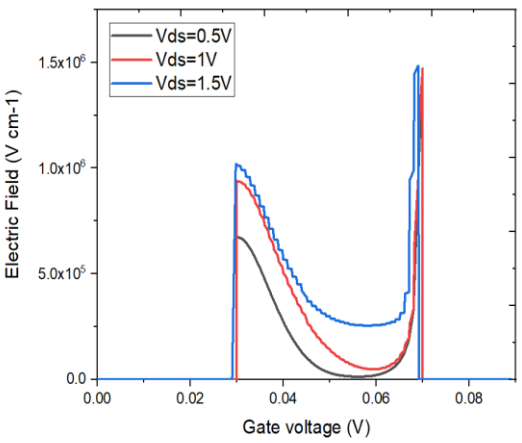
V=0.5V		V=1V		V=1.5V	
Ion	Ioff	Ion	Ioff	Ion	Ioff
1.32x10^{-06}	3.16x10^{-06}	3.84x10^{-06}	4.93x10^{-06}	2.54x10^{-05}	5.42x10^{-06}

TABLE-2: Performance Parameters of p-n-i-n Structure of TFET:

V=0.5V		V=1V		V=1.5V	
Ion	Ioff	Ion	Ioff	Ion	Ioff
1.32x10^{-06}	3.16x10^{-06}	3.84x10^{-06}	4.93x10^{-06}	2.54x10^{-05}	5.42x10^{-06}

CASE: - 2

We have observed the Electric field in p-i-n TFET and p-n-i-n TFET exhibts different responses to the Electric Field with respect to the gate voltage (Vgs).



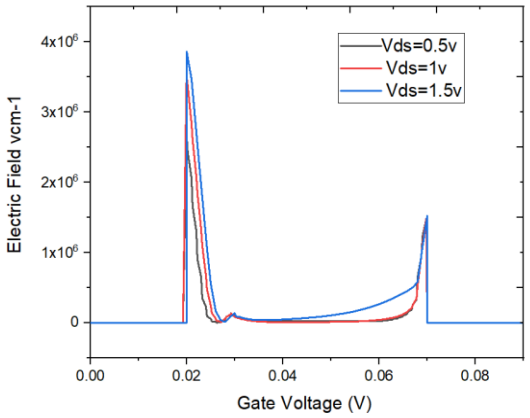


Fig.2(a) Electric Field characteristics of p-i-n TFET 2(b) p-n-i-n at Vd=0.5,1V,1,5V

Figure 2 illustrates the electric field characteristics specifically for p-i-n TFET at different drain voltages (Vd) of 0.5V, 1V, and 1.5V. The graph provides a visual representation of the electric field behavior under the specified conditions.

In Figure 2(a), we observe that the electric field behavior for different drain voltages starts at the same point and continues in a similar manner until reaching Vgs = 0.03V. Beyond this voltage, both electric fields start increasing simultaneously, but the electric field produced by Vd = 1.5V becomes higher compared to Vd = 0.5V and 1V. Eventually, both electric fields decrease and reach a maximum at Vgs = 0.07V. From this analysis, we conclude that in the p-i-n TFET, the electric field exists between Gate voltages of 0.03V and 1.5V.

Figure 2(b) presents the behavior of the electric field in p-n-i-n TFET with respect to the gate voltage (Vgs). Similar to Figure 2(a), the electric field behavior is observed for three different drain voltages: Vd = 0.5V, 1V, and 1.5V. We note that all electric fields start from the same point, but there are differences in the levels of increase. From Vgs = 0.02V to Vgs = 0.07V, the electric field produced by Vd = 1.5V exhibits a higher increase.

Furthermore, we observed that the electric field characteristics for p-i-n TFET raise up to 1.5x^{106}, while for p-n-i-n TFET, it increases up to 4x^{106}. This indicates that the electric field produced by p-n-i-n TFET is greater than the field produced by the p-i-n TFET.

CASE: - 3

We have observed the Potential of p-i-n TFET and p-n-i-n TFET exihibts the different responses to the potential with respect to the gate voltage (Vgs)

Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 04, April-2025

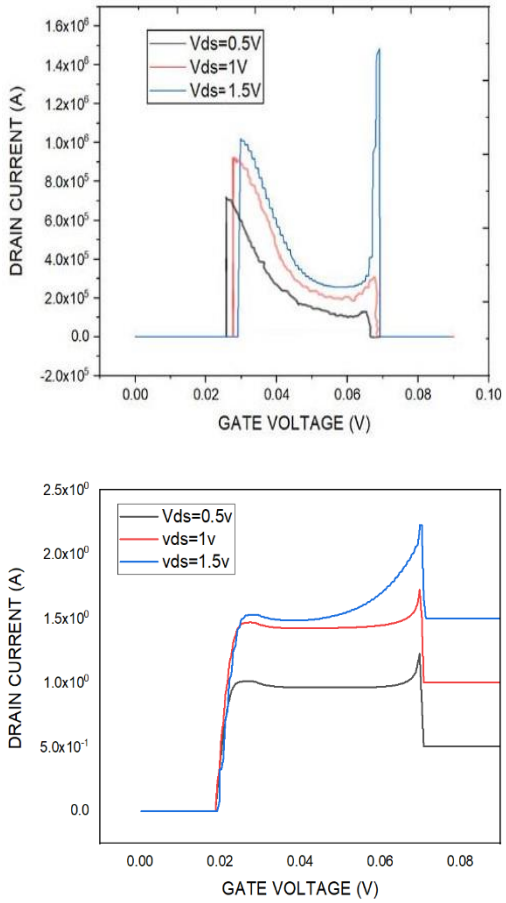


Fig.3. Potential characteristics of (a) p-i-n TFET (b) p-n-i-n TFET at Vd=0.5V,1V,1.5V.

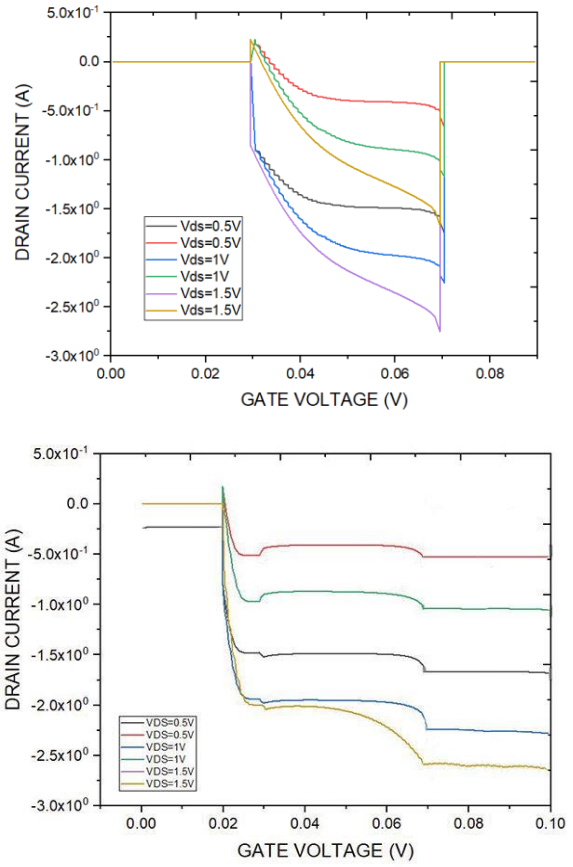


Fig.4. Energy Band characteristics of (a) p-i-n TFET (b) p-n-i-n TFET at Vd=0.5, 1V, 1.5 V.

Figure 3(a) presents the comparison of potential characteristics between p-i-n TFET and p-n-i-n TFET for different drain voltages (Vd). For the p-i-n TFET, the potential waveforms at Vd = 0.5V, 1V, and 1.5V begin at the same gate voltage when Vgs = 0V and end at the same gate voltage when Vgs = 0.9V. However, when the drain voltage is increased to Vd = 1.5V, the potential of the p-i-n TFET rises significantly higher compared to Vd = 0.5V and 1V.

Figure 3(b) Similarly, in the case of p-n-i-n TFET, the potential waveforms at Vd = 0.5V, 1V, and 1.5V also start at the same gate voltage when Vgs = 0V and end at the same gate voltage when Vgs = 0.09V. However, the potential of the p-n-i-n TFET at Vd = 1.5V rises significantly higher compared to Vd = 0.5V and 1V. Additionally, there is a difference in the waveform observed between Vgs = 0.02 and Vgs = 0.07 for the p-n-i-n TFET. Based on this comparison, we can conclude that the potential characteristics of the proposed p-n-i-n TFET are higher than those of the p-i-n TFET. The p-n-i-n TFET exhibits higher potential characteristics, indicating better performance compared to the p-i-n TFET.

CASE: - 4

We have observed the Energy Bands in the p-i-n and the p-n-i-n exhibits different responses to the Electric Field with respect to the gate voltage (v).

Figure 4(a) displays the energy Band characteristics of the p-i-n TFET concerning the gate voltage (Vgs). The energy bands' behaviour in p-i-n TFET is observed for three drain voltages: Vd = 0.5V, 1V, and 1.5V. The energy bands start from the gate voltage Vgs = 0V and extend up to Vgs = 0.07V. Notably, there are two energy bands for the three different voltages. It is worth mentioning that the energy band for the lower drain voltage, Vd = 0.5V, is higher compared to the energy band for the higher drain voltage, Vd = 1.5V.

In Figure 4(b), we can observe the energy band characteristics of the p-n-i-n TFET in relation to the gate voltage (Vgs). The behaviour of the energy bands in the p-n-i-n TFET is studied for three drain voltages: Vd = 0.5V, 1V, and 1.5V. Within the p-n-i-n TFET, the energy bands initiate at Vgs = 0V and span up to Vgs = 0.10V, as depicted in Figure 4(b). The response of the energy bands remains relatively consistent across all drain voltages, although there are noticeable distinctions from Vgs = 0.02V to Vgs = 0.10V.

In summary, we have observed the analytical model of energy bands in the p-i-n TFET and p-n-i-n TFET, highlighting the differences between them. In the p-i-n TFET, there are slight similarities in the raising levels, but the response to the increase in gate voltages differs.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 04, April-2025

CASE: - 5

We have observed the Electron Concentration in the p-i-n and the p-n-i-n exhibits different responses to the Electric Field with respect to the gate voltage (v).

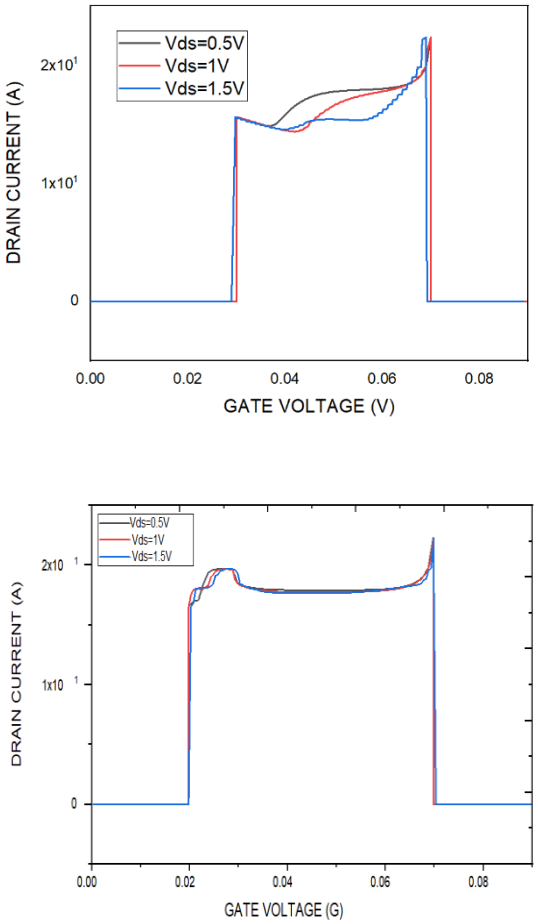


Fig.5. Electron concentration characteristics of (a) p-i-n TFET and (b) p-n-i-n TFET at Vd=0.5,1V, 1.5 V.

Figure 5(a) depicts the comparison of electron characteristics between p-i-n TFET and p-n-i-n TFET for different drain voltages (Vd).

For the p-i-n TFET, the electron characteristic waveforms at Vd = 0.5V, 1V, and 1.5V begin at the same gate voltage when Vgs = 0V and end at the same gate voltage when Vgs = 0.9V. However, when the drain voltage is increased to Vd = 1.5V, the electron concentration of the p-i-n TFET rises significantly higher compared to Vd = 0.5V and 1V.

Similarly, in case of the p-n-i-n TFET, the electron characteristic waveforms at Vd = 0.5V, 1V, and 1.5V also start at the same gate voltage when Vgs = 0V and end at the same gate voltage when Vgs = 0.09V. The electron concentration of the p-n-i-n TFET at Vd = 1.5V rises significantly higher compared to Vd = 0.5V and 1V. Additionally, there is a difference in the waveform observed between Vgs = 0.02 and Vgs = 0.07 for the p-n-i-n TFET.

Based on this comparison, it can be concluded that electron concentration characteristics of the proposed p-n-i-n TFET are similar to the p-i-n TFET. However, there is a difference observed in the operating drain current waveforms between the two devices.

CASE: - 6

We have observed the Hole Concentration in p-i-n and the p-n-i-n exhibits different responses to Electric Field with respect to the gate voltage (v).

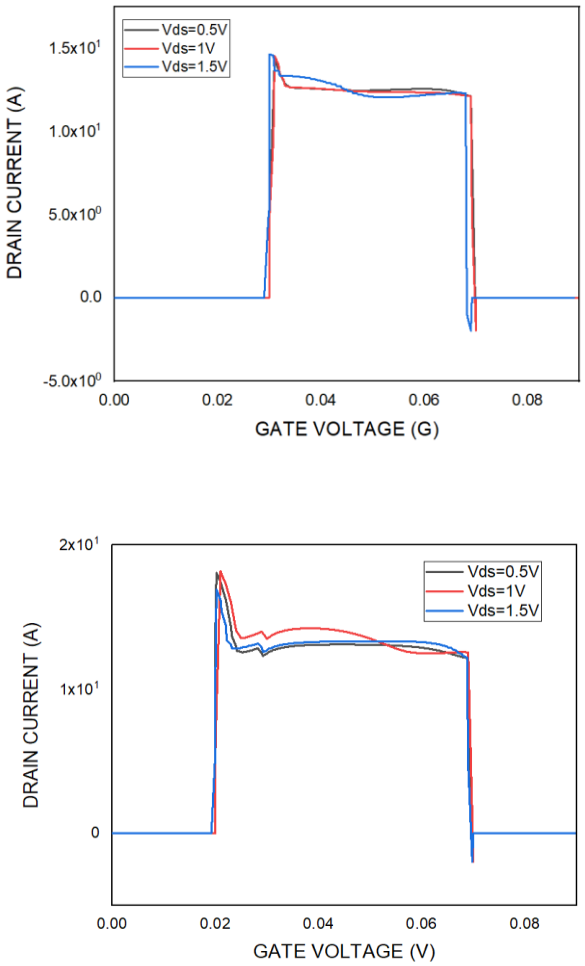


Figure 6(a) illustrates the comparison of whole characteristics between p-i-n TFET (b) p-n-i-n TFET for different drain voltages (Vd).

For the p-i-n TFET, the hole characteristic waveforms at Vd = 0.5V, 1V, and 1.5V start at the same gate voltage when Vgs = 0V and end at the same gate voltage when Vgs = 0.9V. However, when the drain voltage is increased to Vd = 1.5V, the hole concentration of the p-i-n TFET rises significantly higher compared to Vd = 0.5V and 1V. Additionally, there is a difference in the waveform observed between Vgs = 0.02 and Vgs = 0.07 for p-i-n TFET.

Similarly, in case of p-n-i-n TFET, the hole concentration waveforms at Vd = 0.5V, 1V, and 1.5V also start at the same gate voltage when Vgs = 0V and end at the same gate voltage when Vgs = 0.09V. The hole concentration of the p-n-i-n TFET at Vd = 1.5V rises significantly higher compared to Vd = 0.5V and 1V. Additionally, there is a difference in the waveform observed between Vgs = 0.02 and Vgs = 0.07 for the p-n-i-n TFET.

Based on this comparison, it can be concluded that the hole concentration characteristics of proposed p-n-i-n TFET are

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 14 Issue 04, April-2025

similar to p-i-n TFET. However, there is a difference observed in the operating drain current waveforms between the two devices.

V. CONCLUSIONS

This research paper presents a detailed examination of p-n-i-n Tunnel Field Effect Transistor (TFET) through its design and performance analysis [26-30]. The study primarily focuses on evaluating the proposed p-n-i-n TFET, with a specific emphasis on its performance parameters, independent of the fabrication process .Our analysis demonstrates that the proposed p-n-i-n TFET exhibits remarkable sensitivity, particularly regarding the increase in the Electric Field. Notably, we observed that achieving an optimal performance requires a thin N+ layer thickness of precisely 2nm. To explore the influence of N+ layer thickness on the device performance, we conducted experiments by varying the thickness and measuring the resulting drain current. The findings reveal a clear correlation between increasing N+ layer thickness and a decrease in drain current. Additionally, we deliberately reduced the N+ layer thickness below 2nm, specifically to 1nm and 0.5nm, and recorded the corresponding values for comparison. Through our comprehensive analysis, we conclusively establish the critical importance of maintaining an N+ layer thickness of exactly 2nm to ensure reliability across various performance parameters of the p-n-i-n TFET[4-5]. This specific thickness plays a pivotal role in achieving the desired sensitivity and overall performance of the device, underscoring its significance in practical applications.

REFERENCES:

1. Sze, S. M., & Ng, K. K. (2007). Physics of Semiconductor Devices (3rd ed.). Wiley.
2. S. H. Kim, H. Kam, C. Hu, and T. K. Liu, "Germanium-source tunnel field effect transistors with record high ION/IOFF," in Proceedings of the VLSI Symposium Technical Digest, pp. 178-179, 2009.
3. T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive current and < 60 mV/dec subthreshold slope," in Proceedings of thDOe International Electron Devices Meeting (IEDM) Technical Digest, pp. 947-949, 2008.
4. G. F. Jiao, H. Y. Yu, X. Y. Huang, Z. X. Chen, D. M. Huang, N. Singh, G. Q. Lo, D. L. Kwong, and M.-F. Li, "Degradation mechanisms and reliability performance in tunneling field effect transistors," in IEDM Technical Digest, 2009, pp. 741-744.
5. G. F. Jiao, Z. X. Chen, H. Y. Yu, X. Y. Huang, D. M. Huang, N. Singh, G. Q. Lo, D.-L. Kwong, and M.-F. Li, "Experimental studies of reliability issues in tunneling field-effect transistors," IEEE Electron Device Letters, vol. 31, no. 5, pp. 396-398, May 2010.
6. Silvaco, Inc., "Atlas User's Manual," Jun. 11, 2009, pp. 3-114, Eq. 3-413.
7. Y. T. Hou, M. F. Li, Y. Jin, and W. H. Lai, "Direct tunneling hole current through ultrathin gate oxides in metal-oxide-semiconductor devices," Journal of Applied Physics, vol. 91, no. 1, pp. 258-264, Jan. 2002.
8. X. Y. Huang, G. F. Jiao, W. Cao, D. Huang, H. Y. Yu, Z. X. Chen, N. Singh, G. Q. Lo, D. L. Kwong, and M.-F. Li, "Effect of interface traps and oxide charge on drain current degradation in tunneling field-effect transistors," IEEE Electron Device Letters, vol. 31, no. 8, pp. 779-781, Aug. 2010.
9. L. Zhang and M. Chan, "Double-gate tunnel-FETs SPICE modeling incorporating channel transport," IEEE Transactions on Electron Devices, vol. 61, no. 2, pp. 300-307, Feb. 2014.
10. C. Wu, R. Huang, Q. Huang, C. Wang, J. Wang, and Y. Wang, "Analytical surface potential model considering dual-modulation effects in tunnel FETs," IEEE Transactions on Electron Devices, vol. 61, no. 8, pp. 2690-2696, Aug. 2014.
11. M. Bardon, H. Neves, R. Puers, and C. Van Hoof, "Pseudo-two-dimensional model for double-gate tunnel FETs incorporating junction depletion regions," IEEE Transactions on Electron Devices, vol. 57, no. 4, pp. 827-834, April 2010.
12. C. Shen, S.-L. Ong, C.-H. Heng, G. Samudra, and Y. C. Yeo, "Variational approach to the two-dimensional nonlinear Poisson's equation for tunneling transistor modeling," IEEE Electron Device Letters, vol. 29, no. 11, pp. 1252-1255, Nov. 2008.
13. E. Kane, "Zener tunneling phenomenon in semiconductors," Journal of Physics and Chemistry of Solids, vol. 12, no. 2, pp. 181-188, 1960.
14. S. H. Kim, H. Kam, C. Hu, and T. K. Liu, "Germanium-source tunnel field effect transistors with record high ION/IOFF," in VLSI Technology Symposium Digest, pp. 178, 2009.
15. T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive current and subthreshold slope less than 60 mV/dec," in International Electron Devices Meeting (IEDM) Technical Digest, pp. 947, 2008.
16. V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: A novel high-performance transistor," IEEE Transactions on Electron Devices, vol. 55, pp. 1013, 2008.
17. G. F. Jiao, H. Y. Yu, X. Y. Huang, Z. X. Chen, D. M. Huang, N. Singh, G. Q. Lo, D. L. Kwong, and M.-F. Li, "New degradation mechanisms and reliability performance in tunneling field effect transistors," in International Electron Devices Meeting (IEDM) Technical Digest, pp. 741, 2009.
18. G. F. Jiao, Z. X. Chen, H. Y. Yu, X. Y. Huang, D. M. Huang, N. Singh, G. Q. Lo, D.-L. Kwong, and M.-F. Li, "Experimental studies of reliability issues in tunneling field-effect transistors," IEEE Electron Device Letters, vol. 31, pp. 396, 2010.
19. G. Lee, J. S. Jang, and W. Y. Choi, "Dual-dielectric-constant spacer hetero-gate-dielectric tunneling field-effect transistors," Semiconductor Science and Technology, vol. 28, pp. 052001, March 2013.
20. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Gate-drain overlap-free tunnel field-effect transistor," Applied Physics Letters, vol. 91, pp. 053102, July 2007.
21. Silvaco Inc., "ATLAS Device Simulation Software," Santa Clara, CA, Version 5.14.0.R, 2013.

a. Pal, A. B. Sachid, H. Gossner, and V. R. Rao, "Insights into the design and optimization of tunnel-FET devices and circuits," IEEE Transactions on Electron Devices, vol. 58, pp. 1045-1053, April 2011.

22. M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, "Pseudo-two-dimensional model considering junction depletion regions for double-gate tunnel FETs," IEEE Transactions on Electron Devices, vol. 57, pp. 827-834, April 2010.

a. M. Ionescu and H. Riel, "Energy-efficient electronic switches: Tunnel field-effect transistors," Nature, vol. 479, no. 7373, pp. 329-337, Nov. 2011, doi: 10.1038/nature10679.

23. C. Seabaugh and Q. Zhang, "Beyond CMOS logic: Low-voltage tunnel transistors," Proceedings of the IEEE, vol. 98, no. 12, pp. 2095-2110, Dec. 2010, doi: 10.1109/JPROC.2010.2070470.
24. W. Young Choi, B.-G. Park, J. Duk Lee, and T.-J. King Liu, "Tunneling field-effect transistors with subthreshold swing less than 60 mV/dec," IEEE Electron Device Letters, vol. 28, no. 8, pp. 743-745, Aug. 2007, doi: 10.1109/LED.2007.901273.
25. L. Barboni, M. Siniscalchi, and B. Sensale-Rodriguez, "TFET-based circuit design using the transconductance generation efficiency Gm/Id method," IEEE Journal of Electron Devices Society, vol. 3, no. 3, pp. 208-216, May 2015, doi: 10.1109/JEDS.2015.2412118.
26. F. Settino et al., "Potential and limitations of tunnel FETs for low-voltage analog/mixed-signal circuits," IEEE Transactions on Electron Devices, vol. 64, no. 6, pp. 2736-2743, Jun. 2017, doi: 10.1109/TED.2017.2689746.
27. H. Liu, X. Li, R. Vaddi, K. Ma, S. Datta, and V. Narayanan, "RF rectifier design for energy harvesting applications using tunnel FETs," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 4, no. 4, pp. 400-411, Dec. 2014, doi: 10.1109/JETCAS.2014.2361068.
28. M. Seok Kim, X. Li, H. Liu, J. Sampson, S. Datta, and V. Narayanan, "Current-steering D/A converter design using steep-slope heterojunction tunnel FETs for low-power high-SFDR applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 6, pp. 2299-2309, Jun. 2016, doi: 10.1109/TVLSI.2015.2500160.