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Design and Analysis of CMOS Two Stage OP-AMP in 180nm and 45nm Technology

R Bharath Reddy
M.Tech, Dept. of ECE,
S J B Institute of technology
Bengaluru, India

Shilpa K Gowda
Asso Prof, Dept of ECE
S J B Institute of technology
Bengaluru, India

***Abstract*— This paper presents the buffered CMOS two stage op-amp which uses 180nm and 45nm process for design and analysis of CMOS two stage op-amp. Keeping 1.8V power supply, 20µA bias current, aspect ratio W/L, slew rate 20V/µs, input common mode ratio constant. The trade-off among various parameters such as Open loop gain, Phase margin, Gain Bandwidth Product and Power consumption are measured. It has been demonstrated that due to recent development through scaling the size of transistors decreases power dissipated through the device also decreases. This design has been carried out in Cadence design tools.**

Keywords—CMOS Analog circuit, buffered Opamp, 180nm,45nm, CADENCE, Power consumption

I.INTRODUCTION

The operational amplifier, which has become one of the most versatile and important building blocks in analog circuit design. Operational amplifiers are amplifiers that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer function is practically independent of gain. Operational amplifier that use two or more gain stages are widely used when higher gains are needed. One of the most popular op amps is a two-stage op amp. CMOS op amps are very similar in architecture to their bipolar counterparts. A good portion of overall gain is provided by differential-input stage, which improves noise and offset performance. If op-amp drive a low-resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large swing. Biasing circuits are provided to establish the proper operating point for each transistor in its quiescent state. Compensation is required to achieve stable closed-loop performance.

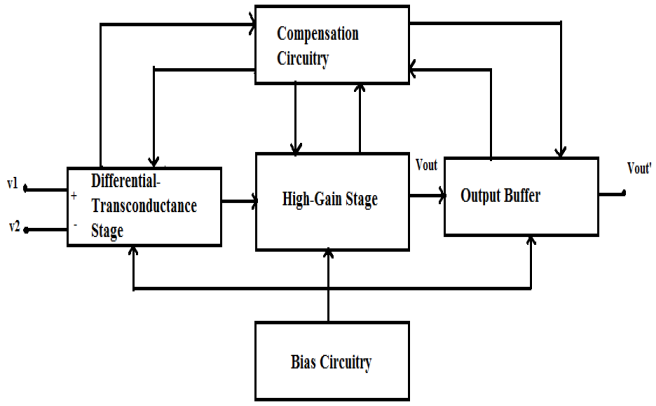

Fig1. General block diagram of two stage Op-Amp

II. LITERATURE SURVEY

In [4], document gives the information about an unbuffered (Operational-transconductance amplifiers or OTAs) two stage operational amplifier which was designed for moderate DC gain, high output swing and reasonable open loop Gain Band product (GBW).Results shows that a two stage op-amp has been designed with gain of 48dB, unity gain frequency of 40MHz, Phase margin of 89degree.Design has been carried out in GPDK180 Cadence design tools.

In [5], document gives the information about an operational amplifier which uses an adaptive biasing circuitry along with an auxiliary circuit to improve the slew rate. Auxiliary circuit gets used when there is large transient or slewing period. Auxiliary circuit improves slew rate and at high frequencies less power is dissipated. Results shows that a two stage op-amp has been designed with slew rate of 31.31V/µs, gain of 40.09dB,unity gain frequency of 52MHz,Phase margin of 88degree.Design has been carried out in GPDK90 Cadence design tools.

In [6], document gives the information about a buffered two stage operational amplifier which was designed in both 180nm and 45nm.And the results of these designs have been compared. Results shows that 180nm two stage op-am gives gain of 47.85dB,unity gain frequency of 668.42MHz,Phase margin of 63.22 degree and 45nm two

stage op-am gives gain of 52.68dB,unity gain frequency of 2.22GHz,Phase margin of 60.92 degree. Power dissipated through 45nm is very less compared to180nm. Design has been carried out in GPDK180 and GPDK45 Cadence design tools.

In [7], document gives the information about an unbuffered (Operational-transconductance amplifiers or OTAs) two stage operational amplifier which was designed for gain of 71dB,unity gain frequency of 37KHz,Slew Rate of 2.344V/µsec and power dissipation of 10mW. Design has been carried out in GPDK180 Cadence design tools.

III. DESIGN PROCEDURE

Relationships describing the op-amp performance[1]:

Slew rate SR $= \frac{I_5}{C_c}$.(i)

First $-$ stage gain Av1 $= -\frac{g_{m1}}{g_{ds2}+g_{m4}} = \frac{-2g_{m1}}{I_5(\lambda_2+\lambda_4)}$.(ii)

Second-stage $A_{v2} = \frac{-g_{m6}}{g_{m6}+g_{m7}} = \frac{-g_{m6}}{I_6(\lambda_6+\lambda_7)}$.(iii)

Gain bandwidth GB $= \frac{g_{m1}}{C_c}$.(iv)

Output pole $p_2 = \frac{-g_{m6}}{C_L}$. (v)

RHP zero $Z1 = \frac{g_{m6}}{C_c}$.(vi)

Positive CMR Vin(max) = V_{dd} - $\sqrt{\frac{I_5}{\beta_3}} + |V_t|(\max)$ $+V_{T1}(\min)$.(vii)

Negative CMR Vin(min) $=V_{ss}+ V_{t1}(\max)+V_{Ds5}(\text{sat})$ $+\sqrt{\frac{I_5}{\beta_1}}$.(viii)

Saturation voltage $V_{DS}(\text{sat}) = \sqrt{\frac{2I_{ds}}{\beta}}$.(ix)

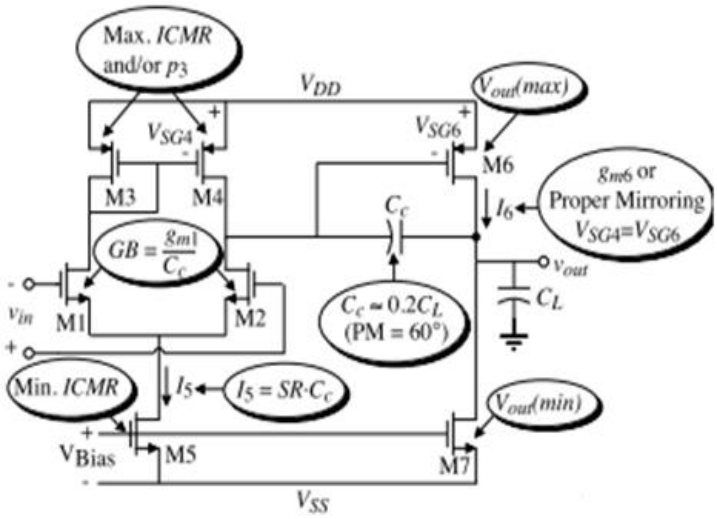

Fig.2 Two stage Op-Amp

1) The design procedure begins by choosing a device length to be used throughout the circuit.

2) The minimum value for the compensation capacitor C_c should be 0.22 times more than C_L to get phase margin 60º.

3) Based on slew rate requirements the value of tail current I_5 is determined.

4) The aspect ratio of M_3 can be determined by positive input common mode ratio range by using the equation (vii).

5) Aspect ratio of M_1 can be determined through transconductance g_{m1} by using equation (iv).

5) To calculate the saturation voltage of transistor M_5 negative input common mode ratio range is used by equation (viii).

6) For reasonable phase margin, the value of g_{m6} is approximately ten times the input stage transconductance g_{m1}.To achieve proper mirroring of the first stage current mirror load of M_3 and M_4 requires $V_{SG4} = V_{SG6}$. By V_{SG6} we can get the aspect ratio of M_6.

7) The device size of M_7 can be determined from the I_6 current flowing through M_6 and balanced equation.

8) The total amplifier gain against the specifications is given by[1]

Av $= \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2+\lambda_4)I_6(\lambda_6+\lambda_7)}$

IV. SIMULATION RESULTS

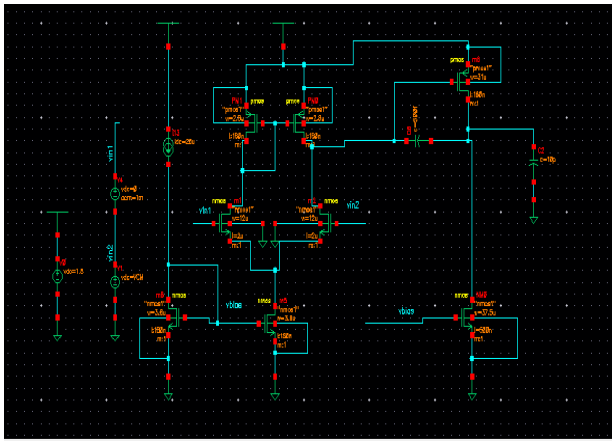

Fig.3Schematic diagram of two stage CMOS Op-Amp

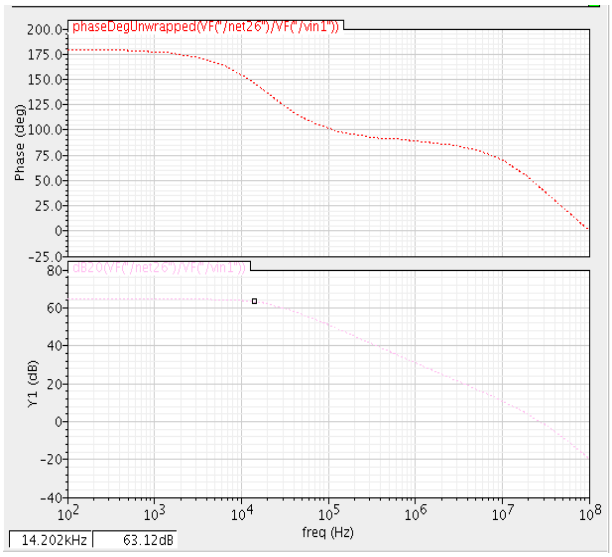

Fig.4 Open loop gain and Phase margin in 180nm .

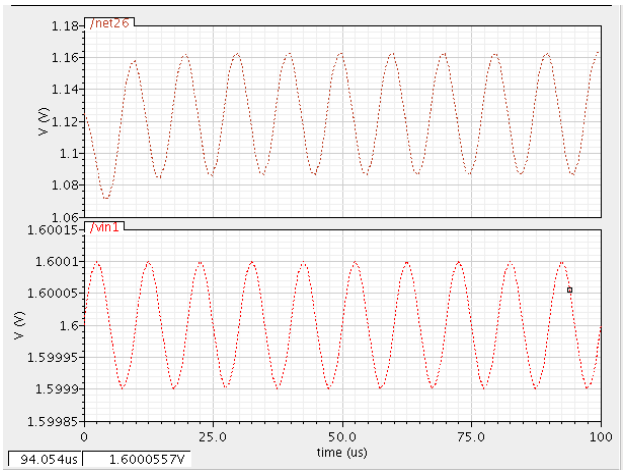

Fig.5Transient Analysis of 180nm

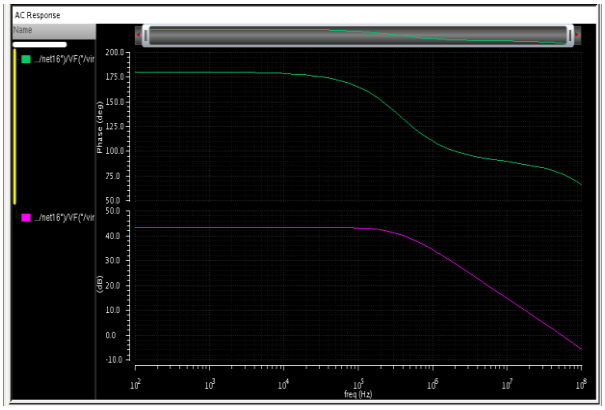

Fig.6 Open loop gain and Phase margin in 45nm .

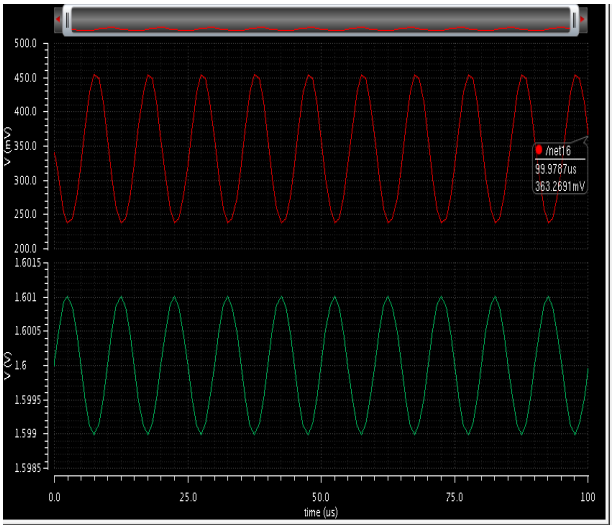

Fig.7 Transient Analysis of 45nm.

Fig3. shows schematic diagram of two stage CMOS op-amp which was designed according to the procedure. For the frequency response plot, an ac signal of 1V is swept with 5 points per decade from a frequency of 100Hz to 100MHz. Fig4 illustrates the frequency response of 180nm op-amp which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of Op-Amp in open loop. The dc gain is found to be 64.95dB and phase margin 60^0 which is good enough for an Op-Amp operating at a high frequency. A dc gain of 64.95dB at unity gain frequency of 34MHz and slew rate 20v/µs is excellent for an Op-Amp when all the other parameters are also set at an optimized value.Fig5.shows the transient analysis of 180nm CMOS Op-Amp. Similarly Fig.6 illustrates the frequency response of 45nm op-amp which shows a dc gain in dB versus frequency in Hz(in log scale) and phase margin of Op-Amp in open loop. The dc gain is found to be 45 dB and phase margin 75^0 which is good enough for an Op-Amp operating at a high frequency. Fig5.shows the transient analysis of 45nm CMOS Op-Amp Power consumed by 45nm is very less compared to 180nm.

TABLE I. COMPARISON WITH PREVIOUS RESULTS

Results	Designed two-stage Op-amp		[4]	[5]	[6]	[7]
Technology(nm)	180	45	180	90	180	180
Power supply(V)	1.8	1.8	3.5	1.2	-	1.8
Bias current(µA)	20	20	-	-	160	-
Cc(fF)	600	600	-	-	100	
Open loop gain(dB)	65	45	48	40	53	71
Phase margin(deg)	60	75	89	89	60	
Gain Bandwidth Product (Mhz)	34	55	40	52	668	.037
Slew rate(v/µs)	20	20	-	31	-	2.34
ICMR(+)(V)	1.6	1.6	-	-	1.6	-
ICMR(-)(V)	0.8	0.8	-	-	0.8	-
Power consumption (µW)	301	142	-	92	3582	

V.CONCLUSION

CMOS two stage op-amp is simulated and analyzed in both 180nm and 45nm. Suitable effort is made to improve the open loop gain, phase margin, gain bandwidth product keeping initial parameters and slew rate constant for both 180nm and 45nm. .The 180nm CMOS two stage op-amp is giving high performance with gain 65dB,phase margin 50deg, Gain Bandwidth Product 30MHz, power consumption 300µW which is very much suitable for switched capacitor filters, analog to digital converters and instrumentation amplifiers. Results shows power consumption through 45nm op-amp is very less compared to 180nm.

REFERENCES

[1] P. Allen and D. Holberg, CMOS Analog Circuit Design. New York: Holt Rinehart and Winston, 1987.
[2] Behzad Razavi, Design of Analog CMOS Integrated circuits, McGraw-Hill Company, New York, 2001.
[3] David Johns, Ken Martin, Analog integrated circuit design, John Wiley & Sons, New York,1997.
[4] D. Nageshwar rao, K. Suresh Kumar, Y. Rajasree Rao, G. Jyothi. "Implementation and simulation of CMOS two stage operational amplifier".
[5] Biplab Panda, S. K. Dash, S. N. Mishra. "High Slew Rate op-amp design for low power Applications".
[6] Siddharth, Mehul Garg, Aditya Gahlaut. " Comparative Study of CMOS Op-Amp in 45nm And 180 Nm Technology".
[7] Shweta karnik, Ajay kumar kushwaha, Pramod kumar jain,D.S.Ajnar. "Design of Operational Trans conductance Amplifier in 0.18µm Technology"
[8] Sanjay Kumar, Pathak Jay, Rajendra Prasad. " Gain improvement of two stage opamp through body bias in 45nm cmos technology ".
[9] Muhammad Syamsi Mohd Taufik,Ahmad anwar Zaimuddin, Anis Nurashikin Nordin."Design and simulation of CMOS two-stage op-amp for MEMS resonator".
[10] Basanta Bhowmik, Manisha Pattanaik, Pankaj Srivastava. "A Low Power Low Noise Two Stage CMOS Operational Amplifier for Biopotential Signal Acquisition System".

Mr. R Bharath Reddy Received B.E Degree from BMS Institute of Technology, Bangalore and presently pursuing M.Tech in VLSI Design and Embedded Systems from Dept. of ECE, SJBIT, Bangalore, Karnataka, India.

Mrs. Shilpa K Gowda Received M.tech Degree from SJCIT, Chikkaballapur and presently working as associate professor in Dept. of ECE, SJBIT, Bangalore, Karnataka, India.