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Design and Analysis of Buck Converter

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***Abstract*—Designs of the power electronics circuitry are now-a-days reducing the size, space and weight of converter / inverter circuits. This is possible because of the availability of new high switching frequency devices. This paper presents a generalized model of buck converters. The converter used for stepping down the voltage is called buck converter. Buck converter is designed, analyzed, simulated & developed. The proposed model of Buck converter consists of two parts: (i) Main converter circuits with the components like switch, inductor, diode, capacitor, and a load, (ii) A control circuit for controlling the operation of the switch using microprocessor through opto-coupler. This model can accurately predict the steady-state behaviors for average load current and voltage across the load of a single switch dc-dc converter. To verify the proposed model, the circuit is prepared & their experimental results were compared with the results obtained by simulation of the circuit in pspice.**

Keywords*—Duty cycle(D_r), Average output voltage(V_o), Input voltage (V_{IN}), ON-time of switch, OFF-time of switch, p-to-p ripple in capacitor voltage(ΔV_C) & inductor current(ΔI_L), frequency (f).

I. INTRODUCTION

The dc-dc converter is a dc power supply that is small, lightweight & highly efficient, and uses a semiconductor-switching element. It can response quickly and suitable to changes in input voltage within the scope of normal operating conditions to return to the normal operating state. It is comprised of (i) switching power supply unit which, can turn ON/OFF switching elements that can be turned ON/OFF at high frequency to convert a dc input voltage V_{IN} into a dc output voltage V_{OUT}, and (ii) a control unit, which is used to control the ON/OFF operation of the switching element of said switching power supply unit [1, 2]. The dc input voltage to the converters is assumed to have zero internal impedance &in the output stage of the converter, a small filter is treated as an integral part of the dc-to-dc converter. The output is assumed to supply a load that can be represented by an equivalent resistance. Computer-based analysis/simulation tools have been used for power-electronics circuits for many years. Challenges in the area of analysis/simulation tools for power-electronics are described in literature [3]. The simulation package (pspice) is used to calculate the circuits wave forms, dynamic and steady state performance of the developed system.

The buck converter is introduced using the evolutionary approach. Let us consider the circuit in Fig.1, containing a single pole double-throw switch. For the circuit in Fig.1, the output voltage equals the input voltage when the switch is in position A and it is zero when the switch is in position B. By varying the duration for which the switch is in position A and B, it can be seen that the average output voltage can be varied, but the output voltage is not pure dc. The output voltage contains an average voltage with a square-voltage superimposed on it as shown in Fig.2. Usually the desired outcome is a dc voltage without any notice able ripple content and the circuit in Fig.1 is to be modified accordingly. This is performed by addition of components in steps and observing their waveforms.

The circuit in Fig.1 can be modified as shown in Fig.3 by adding an inductor in series with the load resistor. An inductor reduces ripple in current passing through it and the output voltage would contain less ripple content. Since the current through the load resistor is the same as that of the inductor.

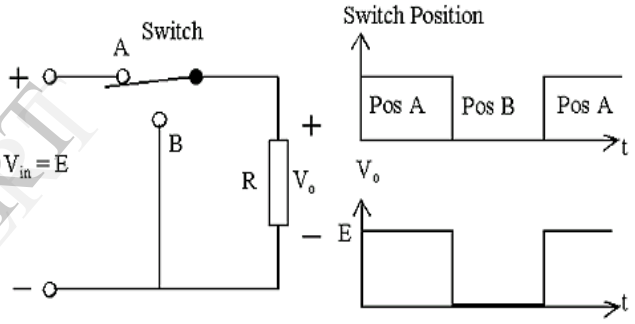

Fig. 1. A resistor with a single-pole double-throw switch

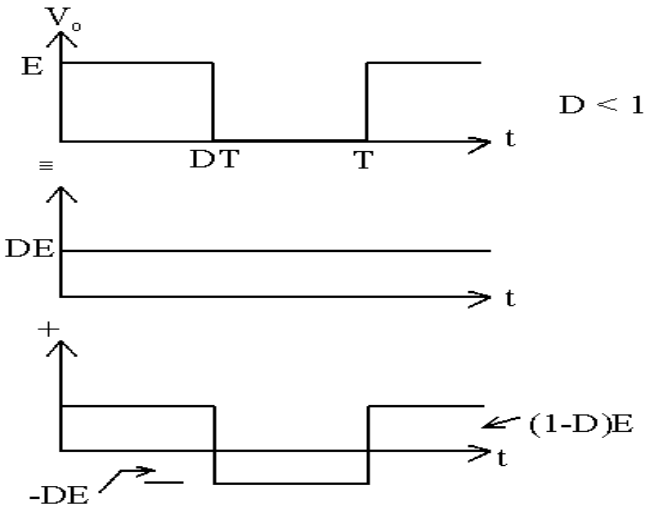

Fig. 2. Output waveform decomposed

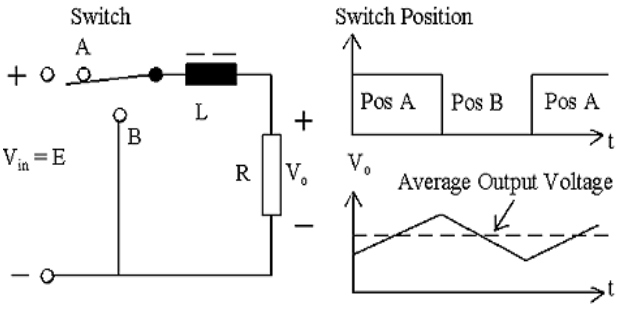

Fig. 3. Effect of adding inductor

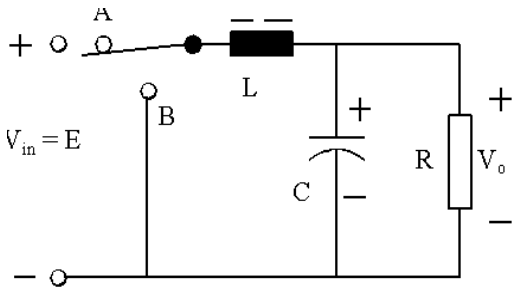

Fig. 4. Effect of adding capacitor

When the switch is in position A, the current through the inductor increases and the energy stored in the inductor increases. When the switch is in position B, the inductor acts as a source and maintains the current through the load resistor. During this period, the energy stored in the inductor decreases and its current falls. It is important to note that there is continuous conduction through the load for this circuit.

If the time constant due to the inductor and load resistor is relatively large compared with the period for which the switch is in position A or B, then the rise and fall of current through inductor is more or less linear, as shown in Fig.3.

The next step in evolutionary development of the buck converter is to add a capacitor across the load resistor and this circuit is shown in Fig.4. A capacitor reduces the ripple content in voltage across it, whereas an inductor smoothes the current passing through it. The combined action of LC filter reduces the ripple in output to a very low level [4].

A. EQUATIONS

The equations that govern the operation of the circuit is as follows:-

In the first state (when the switch is on)

$$di_L / dt = V_S - V_O / L \quad (1)$$

$$dV_O / dt = (I_L - V_O / R) / C \quad (2)$$

Second state (When the switch is off and diode is on)

$$di_L / dt = - V_O / L \quad (3)$$

$$dV_O / dt = (I_L - V_O / R) / C \quad (4)$$

Third state (Both diode and switch are off and inductor is at rest with no energy stored in it)

$$dV_O / dt = (- V_O / R) / C \quad (5)$$

B. SELECTION OF CONVERTER

Table (1) shown below is the converter decision matrix that illustrates, why a Buck converter topology has been selected for this paper. Each factor was weighted equally with a true or false value, with 1 (one) being true and 0 (zero) being false. The assigned points were summed and the converter design with the greatest total was chosen. The linearity criterion refers to the linear relationship between the voltage transfer ratio and the duty cycle [5].

The Buck converter is perfectly linear and has a 1:1 ratio between the voltage transfer ratio and the duty cycle. To meet project specifications a positive voltage is required on the output rather than a negative. Also, the voltage will need to be reduced as the specifications state that the input voltage is to be a nominal 12V and the output voltage a constant 7V. The Buck converter meets both of the aforementioned criteria, as it will reduce the input voltage without inversion.

Fewer number of components leads to a simpler design, which again, the Buck converter has. Therefore, the Buck converter is chosen as the design because it meets all of the specified criteria. Then, the basic circuit topology of the Buck converter, which includes five standard components: (1) a pulse-width modulating controller, (ii) a switch, (iii) an inductor, (iv) a capacitor, and (v) a diode.

Table 1. Converter decision matrix

	Linearity	**Positive Output Polarity**	**Fewest Number of Components**	**Reduces Output Voltage**	**Total**
Buck	1	1	1	1	4
Boost	0	1	1	0	2
Buck-Boost	0	0	1	1	2
Cuk	0	0	0	0	0
SEPIC	0	1	0	0	1

C. OPEN LOOP CONTROLLER

The control circuit acts upon the sensed input and output characteristics of the dc-dc converter and ultimately adjusts the duty cycle to allow the converter to respond to system component and load variations. The key component of the control circuit, which would dictate how the control circuit would do its processing, was chosen based on the results of the decision matrix as shown in Table 2.

Table 2. Control circuit decision matrix

	Ease of Use	Cost	Additional Components	Total
Microprocessor	2	2	1	5
FPAA	1	1	2	4
DSP	0	0	0	0

The microprocessor and DSP are well known control components. The FPAA (Field Programmable Analog Array) is a new integrated circuit, which can be configured to implement analog functions using a set of configurable analog blocks and a programmable interconnection network, and is programmed with the use of on-chip memories.

The criteria in the matrix were rated as 0, 1, or 2. For ease of use, 2 represent the easiest component to implement, while 0 would be the most difficult. The most costly component will receive a 0 in the cost criterion while the least expensive will receive a 2. In the additional components column a rating of 2 means this implementation will have the least amount of extra components and a 0 rating will need the most additional components. The option with the highest cumulative score is selected in this case, the control circuit decision matrix indicate that, the microprocessor is the best choice for buck converter as control circuit.

II. ANALYSIS OF BUCK CONVERTER

A. *BUCK CONVERTER CIRCUIT & ITS PARAMETERS*

Buck converter circuit is shown in Fig.5.

Specifications
VDC = 12V
FREQUENCY = 82.24 KHZ
MOSFET (IRFZ44)
DIODE (1N4500)
DUTY CYCLE = 0.63

Parameters
L=151.5uH
C=4.7uF
R=10ohm

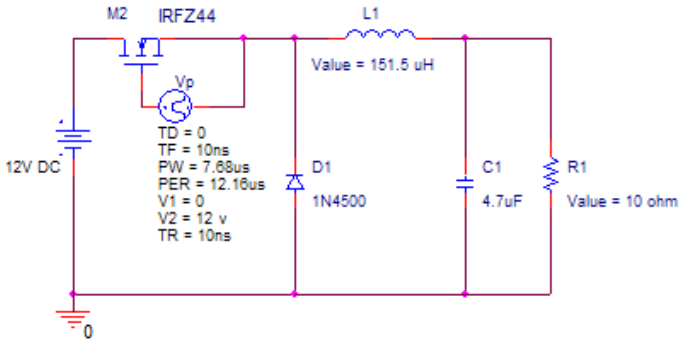

Fig. 5. Buck converter circuit

B. *EQUATIONS*

(a) Output voltage:

$$Vo = D_r \times V_{IN}$$

(b) P-to-P ripple in capacitor voltage:

$$\Delta V_C = [V_{IN} \times D_r (1 - D_r)] / 8LC f^2$$

(c) Inductor current (ΔI_L):

$$\Delta I_L = [V_{IN} \times D_r (1 - D_r)] / f L$$

(d) Maximum and minimum current of inductor:

$$I_{MAX} = I_{O+} V_O T_{OFF} / 2 L$$

$$I_{MIN} = I_O - V_O T_{OFF} / 2L$$

(e) Determination of filter inductance:

$$L = 3.33 V_O (T_S - T_{ON}) / I_O$$

(f) Determination of filter capacitance:

$$\Delta V_C = V_{IN} D_r (1 - D_r) / 8LC f^2$$

III. DESIGN CONSIDERATION OF BUCK CONVERTER

In designing a buck switching converter, certain specifications are needed as: (i) Nominal input dc voltage = V_{IN} volt, (ii) Variation of input voltage = ±25% of V_{IN} (say), (iii) Output voltage = V_{OUT} volt, (iv) Maximum load current = I_{MAX} (max) A, (v) Minimum load current = I_{MIN} (min) A, and (vi) Output maximum ripple voltage =ΔV_O volt (p–to-p) [6, 7].

IV. HARDWARE REQUIREMENT

A. *SPECIFICATION OF THE CIRCUIT*

The specifications of the components used in the circuit (Fig. 6) are mentioned below:-

(A) Main circuit:- Input supply of 12 volt, Switch MOSFET (IRFZ44), Diode (1N4007), Inductor (Ferrite core) = 151.5 ∝H, Capacitor (electrolytic)=4.7∝F, Resistive load (R)=10ohm/5 watts.

(B) Auxiliary circuit: - Input supply of 12volt, Opto-coupler (MCT2E), Transistor (2C547), Three Resistors (100 ohm, 1 kilo ohm, 1 kilo ohm).

B. *PRACTICAL VALUES*

(A) Generation of square wave:

In Intel 8085 microprocessor, Time for 1T state is 320nsec.

Therefore,

Delay Time = 320 × 10^{-9} ×24
= 7.68 µsec

OFF- Time = 320 × 10^{-9} ×14
= 4.48 µsec

Total time period (T_S) is given by
= T_{ON} + T_{OFF}
= (7.68+4.48) µsec

T_S = 12.16 µsec

F = 82.24 K HZ

(B) Duty cycle :

$D_r = T_{ON} / T$
$= 7.68/12.16$
$D_r = 0.63$

(C) Determination of L: We have,

$L = 3.33\ V_O\ (T_S - T_{ON}) / I_O$

Output Power $= (I_O)^2 \times R_L$
$5 = (I_O)^2 \times 10$
$I_O = 0.70$ amp

Therefore, $L = 3.33\ V_O\ (T_S - T_{ON}) / I_O$
$L = 3.33 \times 7.56\ (12.16 - 7.86) \times 10^{-6} / 0.70$
$L = 154.64$ µH

(D) Determination of C

$\Delta V_C = V_O\ (V_{IN} - V_O) / 8LC f^2 V_{IN}$

As ripple is independent of the output load power, so long as the converter operates in continuous conduction mode. It should be less than or equal to one. i.e $\Delta V_C \leq 1$.Let the ripple in output voltage be 0.07.

From above the calculation, value of C is given as 4.7µF i.e. C =4.7µF.

V. OBSERVATION

It is observed that output voltage across load is come out to be approximately 7.2 volt, which is about 40% of the input (12 volt).

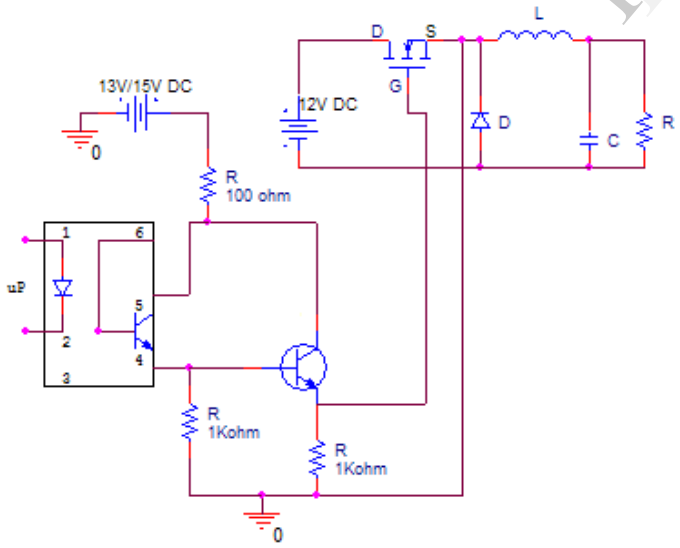

Fig. 6. Hardware circuit

VI. SIMULATION RESULTS

Buck converter with pspice:

1) Make the circuit for Buck converter, using the following parts:

VDC (Voltage source)
V Pulse
IRFZ44 (MOSFET switch)
R (Resistance)
L (Inductance)
C (Capacitance)
IN4007 (Diode)
GND-signal

2) Connect the differential voltage marker and current marker at different position [7].

3) Get plots for the following: -

Load voltage & current, Inductor voltage & current, Capacitor current. Results of the simulation of these waveforms are shown in Fig.7, Fig.8, Fig.9, Fig.10, and Fig.11 respectively.

VII. CONCLUSION

In this work, Buck converter is analyzed, designed for low output voltage ripple (0.07) with the output voltage of 7.2 volts & maximum current of 1A. The circuit has been simulated using pspice software and then hardware has been developed & controlled by microprocessor. The simulation results and experimental results are almost in agreement with each other.

VIII. SUGGESTION FOR FUTURE WORK

The developed buck converter can be modified to operate in a closed loop. If micro-controller is used for controlling the switching operation, the circuit will become more compact and reliable.

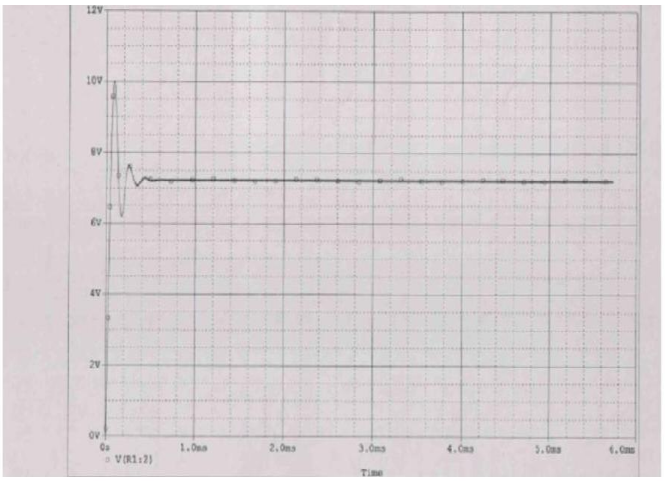

Fig. 7. Load - Voltage waveform

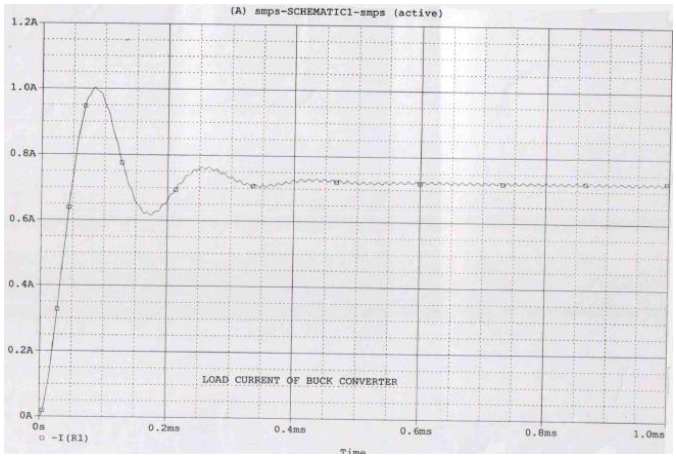

Fig. 8. Load - Current of Buck converter

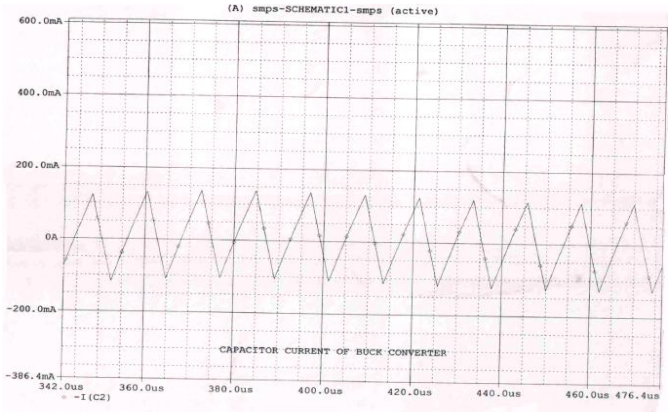

Fig. 11. Capacitor - Current of Buck converter

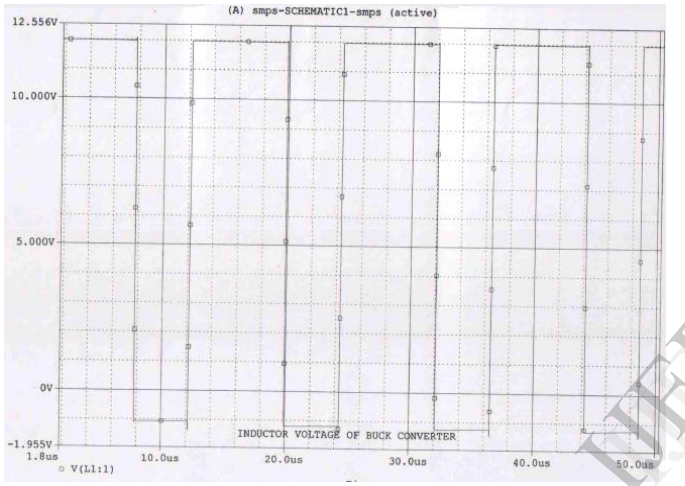

Fig.9: Inductor - Voltage of Buck converter

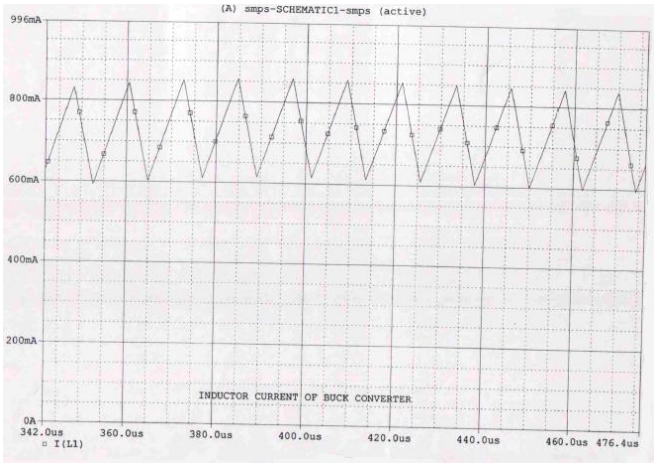

Fig. 10. Inductor - Current of Buck converter

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