Design And Analysis Of Adder And Multipliers For Quantum – Dot Cellular Automata

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Abstract - Quantum -dot cellular automata (QCA) is an emerging nanotechnology, with the potential for faster speed, smaller size, and lower power consumption than transistor-based technology. Quantum -dot cellular automata has a simple cell as the basic element. The cell is used as a building block to construct gates and wires. Previously, adder designs based on conventional designs were examined for implementation with QCA technology. That work demonstrated that the design trade-offs are very different in QCA. This paper utilizes the unique QCA characteristics to design a carry flow adder that is fast and efficient. Simulations indicate very attractive performance (i.e., complexity, area, and delay). This paper also explores the design of serial parallel multipliers. A serial parallel multiplier is designed and simulated with several different operand sizes.

Index Terms—Adder, carry lookahead adder, mulitplier, layout, logic design, quantum-dot cellular automata (QCA), simulation.

I. INTRODUCTION

NANOTECHNOLOGY draws much attention from the public nowadays. Because the current silicon transistor technology faces challenging problems, such as high power consumption and difficulties in feature size reduction, alternative technologies are sought from researchers. The ITRS report[1] offers a good summary of future technologies. Quantum -dot cellular automata (QCA) is one of the promising future solutions. Since it was first introduced in 1993 [2], experimental devices for semiconductor , molecular and magnetic approaches have been developed [3]–[8]. Recent papers show that QCA can achieve high density [9], fast switching speed [10], and room temperature operation [6], [11]. In the QCA research area, there are two approaches. One is a physical design and the other is an algorithmic design. High-level designs focus on the logical and algorithmic design in addition to the physical design. Even though the actual QCA circuit designs need to manage considerable physical interactions which are possibly undesirable and disruptive, the algorithmic approach is also an important aspect in large systems. Recently several QCA circuit designs have been introduced [12]–[17].

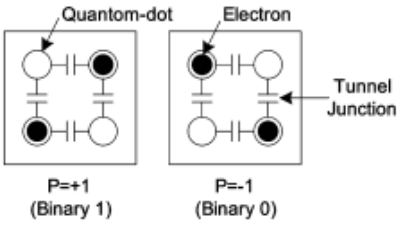

Fig. 1. Basic QCA cells and two possible polarizations.

To exploit the characteristics from circuit design perspectives, a comparison with different circuits is needed. A recent paper presented a comparison of several different adders [18], but it concentrated on small word sizes. That is a good starting point for comparisons, but it does not address the significant size and complexity issues that arise with large word sizes. This paper presents practical adder designs of three different types of adders in QCA: ripple carry adders, carry lookahead adders, and conditional sumadders. The designs follow the conventional design approaches, but due to the technology differences, they are modified for the best performance in QCA. The architectural designs are based on modular structures for design reuse. The comparisons are based on real circuit layouts and simulations according to the complexities and performances. The final designs show different delay characteristics among the adder styles. The only remaining issue is comparing current technology (CMOS) with something that is very far out. This paper considers how to use QCAs if they ever become practical. Also the result in this paper can perhaps provide guidance to the physics community. The paper is organized as follows. In Section II, the background of QCA technology and the design approaches are presented. Sections III and V show the architectural design and implementation of the three types of adders in QCA. Analyses of simulation results and comparisons follow in Section VI and conclusions are presented in Section VII.

II. QCA DESIGN SCHEMES

A. QCA Cell

A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells confining free electrons. Each cell has four quantum dots which can possess a single electron per dot. The four dots are located in the

corners of a square structure. The cell can be charged with two free electrons which can tunnel through to neighbouring dots. By the clocking mechanism, the electrons tunnel through to the proper location during the

clock transition. A high potential barrier locks the state and results in

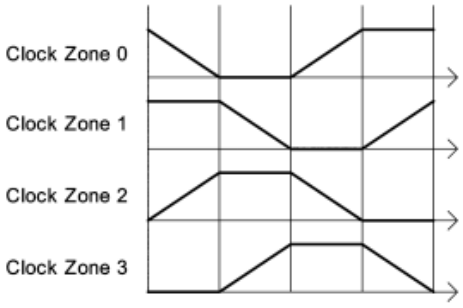

Fig. 2. QCA clock zones.

a local polarization which is determined by Coulombic repulsion. The two electrons reside in opposite corners so that two polarizations are possible as seen in Fig. 1. Thus, two binary states can be represented. Once the cell polarization is set, the adjacent cell is affected by that cell and has the same polarization due to Coulombic repulsion. In this way, signals are propagated. Also there are special purpose rotated cells that are used for wire crossings as described in Section II-E.

B. Clock Zones

TheQCAcell itself is a storage cell, computing cell, andwire. A series of QCA cells act like a wire. The signal flow is controlled by clocks. As the main source of the synchronization, a clock plays a key role in the QCA circuit. QCA circuit areas are organized into four clock zones. As shown in Fig. 2, there is a 90 phase shift from one clock zone to the next. In each clock zone, the clock signal has four states: high-to-low, low,low-to-high, and high. The cell begins computing during the high-to-low state and holds the value during the low state. The cell is released when the clock is in the low-to-high state and inactive during the high state.

Fig.3. QCA wire

Fig. 3 shows a QCA wire. In this wire, half the clock zones are deactivated. So the cell is refreshed every cycle. To be used as a memory cell, a loop of the cells is needed, in which a series of clock zones are used.

C. Logic Gates

For QCA circuit elements, basic logic gates are required. In QCA, they are an inverter and a three-input majority gate. The logic equation for a majority gate is $M(a,b,c)= ab + bc + ca$ .The gate symbols and their layouts are shown in Fig. 4. AND and OR gates are implemented by setting one input to a constant

$$a.b = M(a,b,0)$$

$$a + b = M(a,b,1)$$

If one input is set to 0, then the output is the AND of the other two inputs. If one input is set to 1, then the output is the OR of the other two inputs. With ANDs, ORs, and inverters, any logic function can be realized. Several examples of optimal gate construction are introduced in [19], [20]. A 7-input complex gate

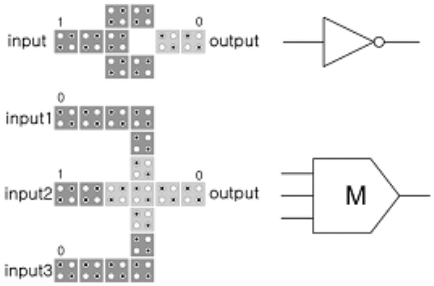

Fig. 4. QCA inverter and majority gate.

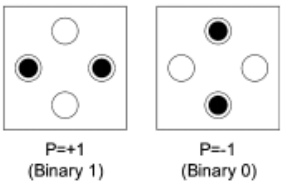

Fig. 5. QCA rotated cells and two possible polarizations.

structure is described in [21] that supports a wide range of logic functions.

D. Pipeline Design

In QCA, wire is composed of QCA cells and the cells are refreshed every clock cycle, so all signals should be synchronized at each computational point.With four different clock zones, the signal propagations are synchronized. The cells in each clock zone behave like a single latch. This can simplify pipeline design. Signal feedback is possible but not recommended because extra wires are needed to keep the previous state value. Feedforward design is better in QCA. Based on these QCA characteristics, a pipeline design with no feedback is chosen for the design of three different adders.

E. Crossover Design

In QCA, there are two crossover options. There are coplanar crossings and multilayer crossovers. Coplanar crossings use only one layer, but require using two cell types (regular and rotated). The regular cell and the

rotated cell do not interact with each other when they are properly aligned, so rotated cells can be used for coplanar wire crossings. Multilayer crossovers use more than one layer of cells like multiple metal layers in a conventional IC. The rotated cell diagram is represented in Fig. 5 and example layouts of coplanar and multilayer wire crossings are shown in Figs. 6 and 7.

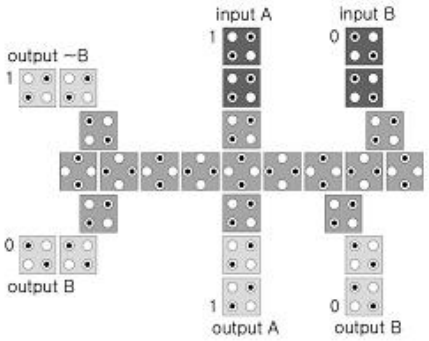

Fig.6. Layout of coplanar wire crossing.

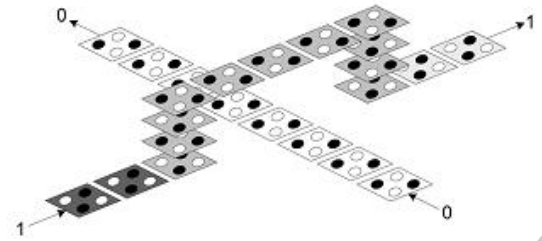

Fig.7. Layout of multilayer wire crossing.

In the coplanar crossing, rotated cells are used when two wires cross. By choosing the connection point from rotated cells, either an original or an inverse of the input is available. In a coplanar crossing, there is a possibility of a loose binding of the signal which causes a discontinuity of the signal propagation and there is the possibility of back-propagation from the far side constant input. So putting enough clock zones between the regular cells across the rotated cells is required.

On the other hand, a multilayer crossover is quite straight forward from the design perspective and the signal connection is steadier. The implementation process is less well understood than that for coplanar crossings.Most of the designs in this paper use the multilayer crossovers, but some use coplanar crossings for comparison to the multilayer designs. For consistent comparisons, only the multilayer crossover designs are shown in the layout figures. The comparisons between coplanar and multilayer crossovers are discussed in Section VI.

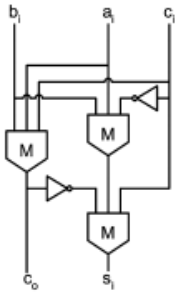

Fig.8. Full Adder Schematic.

F. Design Rules

Cells are assumed to have a width and height of 18 nm and quantum dots are 5 nm in diameter. The cells are placed on a grid with a cell center-to-center distance of 20 nm. Thus, the cell size can be defined as 20 nm. Current literature shows that possible QCA implementations have cell sizes of 3 nm [23], 2.8 nm [24], and 1.32 nm [25]. As an assumption, a 25 nm cell size was used in [26]. Thus, the 20 nm assumption is valid for conservative designs.

Because there are propagation delays between cell-to-cell reactions, there should be a limit on the maximum cell count in a clock zone. This insures the proper propagation delay and reliable signal transmission. In

Fig.9. Full Adder Layout.

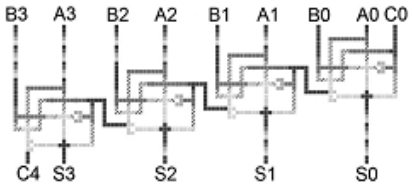

Fig.10. 4 bit ripple carry adder layout.

physical design perspectives, there are several circuit operation issues. Long span wires are more vulnerable to noise and possibly signal back propagation [22]. The current QCA technology does not specifically set the possible operating frequency and actual propagation delays. Thus, the maximum cell count can be set as a design parameter. Throughout the designs, a maximum of 15 cells are used in a single clock zone. This provides

freedom to make possible wire routes and a reasonable size for each clock zone.

The minimum separation of two different signal wires is the width of two cells. Also the clock is incremented synchronously at the input sides of a gate.

For the circuit layout and functionality check, a simulation tool for QCA circuits, QCADesigner [27], is used. This tool allows users to do a custom layout and then verify QCA circuit functionality by simulations. It includes two different simulation engines such as a bistable approximation and a coherence vector.

G. Multiplier Design

The structure shown in Fig. 15 is used for the QCA circuit implementation since it minimizes the latency from the first input to the first output. Fig. 16 shows the block diagram of the optimized design for QCA layout

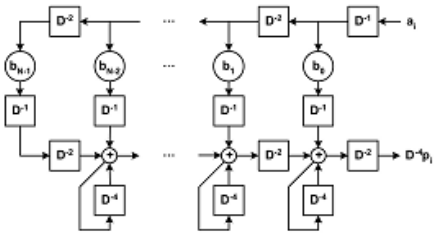

Fig.11. CDM network for QCA.

H. QCA Implementation

Bit-serial adders are used to realize the carry delay multiplier.

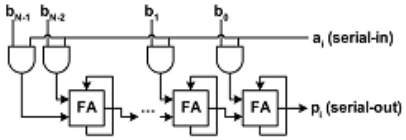

Fig. 12. Multiplier block diagrams for CDM.

The bit-serial adder is modified from the full adder so that the carry-in and carry-out are connected internally with a one clock delay. Figs. 17a and 17b show the schematic and layout of the bit-serial adder.

For N-bit inputs, the multiplier receives N þ 1 inputs (a serial input and N parallel inputs) and produces a serial output. The serial input and output are ordered from LSB to MSB and parallel inputs are repeated whenever a new serial input is provided (N cycles). For initialization of the multiplier, zero bits are input for N clock cycles. Zero bits are provided between successive inputs. The time to complete an N-bit multiplication is 2N cycles.

CONCLUSIONS

QCA circuits have significant wire delays. For a fast design in QCA, it is generally necessary tominimize the complexity. Based on the QCA characteristics, this paper presents a new adder design, the carry flow adder. This paper designs the adders and multipliers with 4 bit, 8 bits and if possible 16 bits.

QCA technology is really a big step towards overcoming the challenge of the modern silicon technology. Though there are various other design technologies, this QCA technology deals with 20 nm scale and so helps in scaling of the modern silicon technology. Moreover, there are not much more number of QCA cells used for the design and overcome the problem of complexity.

ACKNOWLEDGEMENT

This paper is a significant extension of the conference papers dealing with less bit design and simulation of adders like look ahead adder, ripply carry adders and conditional adders.

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