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Design and Analysis of a 13-Level Switched Capacitor Boost Multilevel Inverter with Reduced Number of Switches

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***Abstract* - This paper presents the design and simulation of a high step-up 13-level switched-capacitor multilevel inverter (SC-MLI) with a reduced number of power switches. The proposed inverter topology is capable of generating thirteen output voltage levels using a single DC source, thereby eliminating the need for multiple isolated sources or bulky transformers. A switched-capacitor configuration is employed to achieve voltage boosting while maintaining self-voltage balancing of the capacitors. Nearest Level Modulation (NLM) is adopted as the control strategy to generate the gating signals, which enables low switching frequency operation and reduces switching losses. The performance of the proposed inverter is evaluated using MATLAB/Simulink under no-load and load conditions, and key parameters such as output voltage waveform, RMS voltage, voltage regulation, and total harmonic distortion (THD) are analyzed. Simulation results demonstrate that the proposed 13-level SC-MLI achieves high voltage gain, improved power quality, and acceptable voltage regulation with reduced circuit complexity. Due to its compact structure and efficient operation, the proposed inverter is suitable for renewable energy and medium-power applications.**

Keywords* - *Switched Capacitor, Nearest Level Modulation, Multilevel Inverter, Total Harmonic Distortion

I. INTRODUCTION

In renewable energy systems including photovoltaic (PV) arrays, wind energy conversion systems, and fuel cell applications, multilevel inverters are widely acknowledged as an efficient power conversion option. Higher voltage operation, decreased dv/dt stress, lower voltage stress on power semiconductor devices, and better output waveform quality with less harmonic distortion are the main advantages of MLIs. Neutral-point-clamped multilevel inverters (NPC-MLI), flying capacitor multilevel inverters (FC-MLI), and cascaded H-bridge multilevel inverters (CHB-MLI) are the three main types of multilevel inverter structures. Nevertheless, clamping diodes in NPC-MLIs, flying capacitors in FC-MLIs, and separated DC sources in CHB-MLIs become much more necessary as the number of voltage levels increases. Furthermore, in order to preserve capacitor voltage stability, NPC and FC topologies require extra balancing circuits and intricate control schemes. To achieve greater AC voltage levels, an output-side transformer or a front-end DC–DC boost converter is frequently also required. These elements increase the size, complexity, and expense of the system.

Switched-capacitor-based multilevel inverters (SCMLIs) have become a viable substitute to overcome these drawbacks. By using switched capacitors, SCMLIs increase the number of voltage levels and provide voltage boosting capacity without requiring large transformers or inductors. A nine-level output voltage is achieved with a switched-capacitor T-type multilevel inverter design that guarantees capacitor voltage self-balancing without the need for further balancing circuits. Nevertheless, in order to control the voltages between the clamping capacitors, this arrangement depends on two symmetrical DC sources. Additionally, it has been stated that a back-end H-bridge design is frequently used to produce the negative voltage levels at the output.

However, the H-bridge's applicability for high-voltage applications is limited since its four switches must withstand the maximum output voltage. As an alternative, a multilevel inverter topology with a single DC source and no H-bridge was presented. The number of switched capacitors and semiconductor devices increases in proportion to the number of output voltage levels, even though this arrangement lessens the voltage stress across individual power switches. In recent years, switched-capacitor-based multilevel inverters have gained significant attention as an alternative approach to address the drawbacks of conventional MLIs. These inverters utilize capacitors that are dynamically connected in series and parallel configurations to achieve voltage boosting without the need for bulky transformers or inductors. As a result, switched-capacitor inverters offer compact size, high power density, and inherent voltage boosting capability. Moreover, properly designed switched-capacitor topologies can achieve self-voltage balancing of capacitors, eliminating the need for additional sensing or control mechanisms.

II. PROPOSED TOPOLOGY

A. Description of the Proposed SC Based 13-Level MLI

The proposed 13-level switched-capacitor multilevel inverter (13LSCI) topology is composed of a single DC input source (Vin), fourteen controlled power switches (S1–S14), one diode (D1), and three switched capacitors (C1, C2, and C3). Each power switch is connected with an antiparallel diode to enable bidirectional current flow, which is essential for inductive load operation. The primary objective of this topology is to generate a high-quality multilevel AC output with a significantly

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boosted voltage using a reduced number of components and without employing a conventional H-bridge. The proposed inverter is capable of producing thirteen distinct voltage levels at the output, namely 0, ±Vdc, ±2Vdc, ±3Vdc, ±4Vdc, ±5Vdc, and ±6Vdc. Unlike conventional multilevel inverters, polarity reversal is inherently achieved through the switching configuration itself, eliminating the need for a separate back-end H-bridge. As a result, the voltage stress across the switches is substantially reduced, since no switch is required to block the full output voltage. The circuit diagram of the proposed 13-Level Switched Capacitor MLI is shown in the below figure 1.

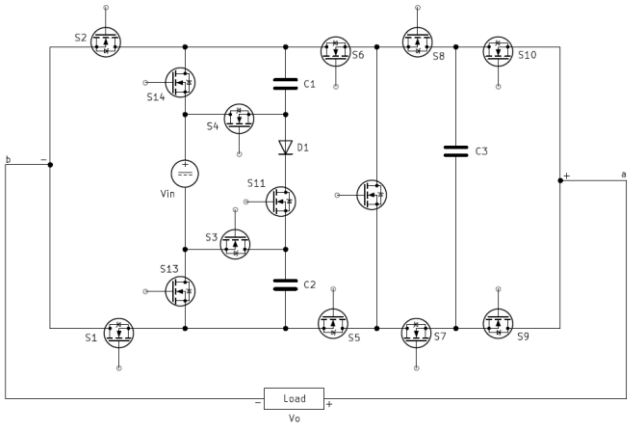

Fig. 1 Circuit Diagram of the 13-Level Switched Capacitor Multilevel Inverter

The voltage boosting capability of the inverter is realized through the series and parallel combination of the switched capacitors. During different switching states, capacitors C1 and C2 are charged to the input voltage Vin, while capacitor C3 is charged to three times the input voltage (3Vin). By appropriately connecting these capacitors in series with the DC source, the output voltage can be increased up to six times the input voltage without the use of bulky transformers or inductors. This switched-capacitor-based boost operation significantly improves the power density of the inverter system.

A key advantage of the proposed circuit is the reduction in the total number of power switches. Switches S3 and S4 perform dual functions by participating in both capacitor charging and discharging processes during specific operating states (states 2, 5, 9, and 12). This multifunctional operation allows the inverter to achieve a higher number of voltage levels with fewer switches compared to conventional multilevel inverter topologies. Consequently, the overall system complexity, cost, and gate driver requirements are reduced.

B. Operation of the Proposed SC Based 13-Level MLI

Mode 1 operation: In mode 1 the capacitor C1 is directly connected in parallel with the DC input source Vin and is charged to the input voltage level. During this operating state, capacitors C1 and C2 are configured in series with capacitor C3 through the selected switching combination. The current flows from the DC source through the active switches and the load, while capacitors C2 and C3 contribute to the output by discharging. As a result, the inverter produces the minimum positive output voltage level, equal to +Vin. The circuit diagram of Mode 1 is shown in the below figure 2.

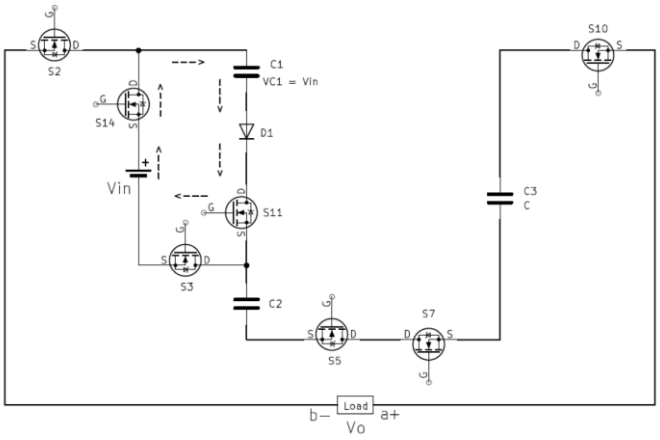

Fig. 2 Circuit Diagram of Mode-1 Operation

Mode 2 operation: In mode 2 the switches S4 and S11 are turned ON, which connects capacitor C2 directly in parallel with the DC input source Vin. As a result, capacitor C2 is charged to the input voltage level Vin. Simultaneously, the DC source Vin and the previously charged capacitor C1 are connected in series through switch S4, forming the main current path to the load. During this mode, capacitor C1 discharges and contributes its stored energy along with the input source to the output. Capacitor C3 remains electrically isolated and does not participate in the energy transfer during this state. Due to the series combination of Vin and C1, the output voltage across the load becomes the sum of their voltages, resulting in an output level of +2Vin. The circuit diagram of Mode 2 is shown in the below figure 3.

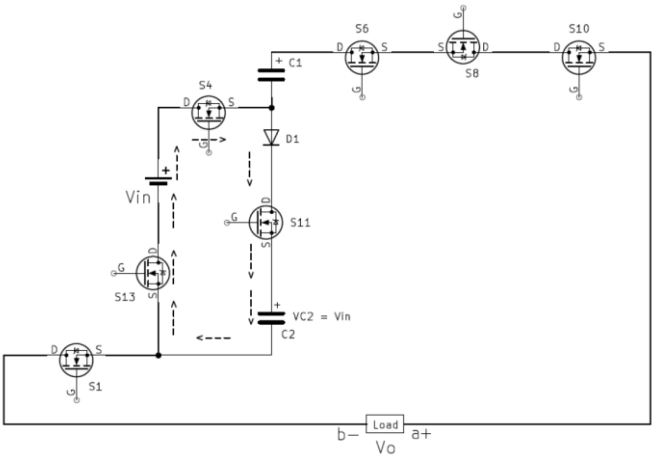

Fig. 3 Circuit Diagram of Mode-2 Operation

Mode 3 operation: In mode 3 the switches S3 and S4 are simultaneously turned ON, which connects the DC source Vin in series with capacitors C1 and C2. Since capacitors C1 and C2 are already charged to Vin from previous operating states, their series combination with the input source results in a cumulative voltage of 3Vin being applied across the load. During this mode, both C1 and C2 discharge and transfer their stored energy to the load along with the input source. At the same time, capacitor C3 is connected in parallel with the series combination of Vin, C1, and C2 through the appropriate switching path. Consequently, C3 is charged to a voltage level

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equal to +3Vin. The circuit diagram of Mode 3 is shown in the below figure 4.

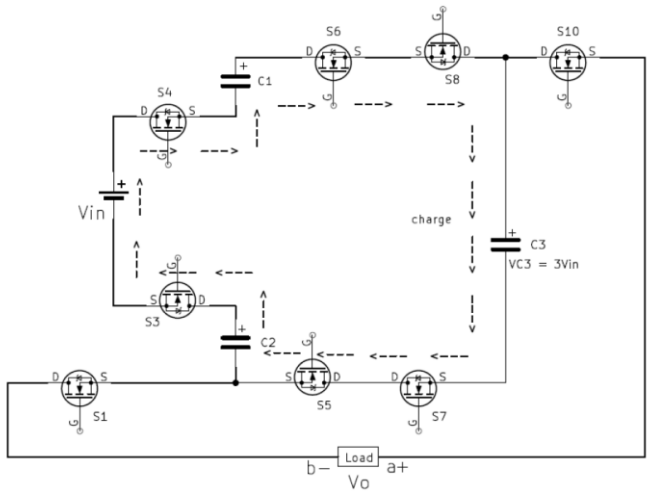

Fig. 4 Circuit Diagram of Mode-3 Operation

Mode 4 operation: In mode 4 the switching configuration connects the input DC source Vin in series with capacitor C3, which has been previously charged to 3Vin during State 3. Through the appropriate conduction path established by the active switches, Vin and C3 discharge together through the load. As a result, the output voltage becomes the algebraic sum of the input source voltage and the capacitor voltage, yielding an output level of +4Vin. The circuit diagram of Mode 4 is shown in the below figure 5.

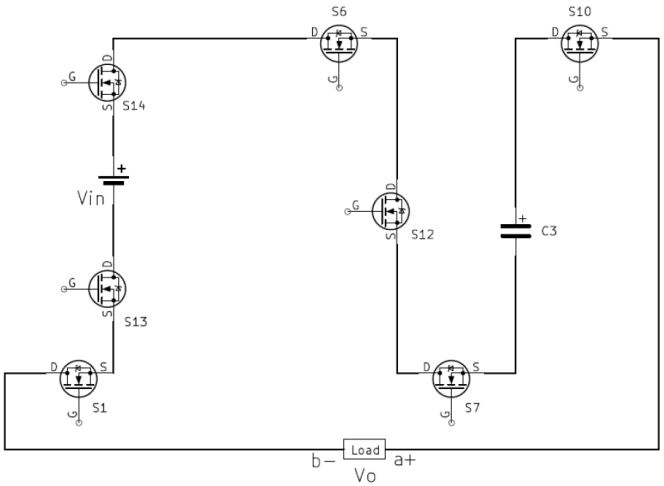

Fig. 5 Circuit Diagram of Mode-4 Operation

Mode 5 operation: In mode 5 the selected switching configuration connects the DC input source Vin and capacitor C1 in series with the high-voltage capacitor C3. Since capacitor C1 is charged to Vin and capacitor C3 holds a voltage of 3Vin from earlier operating states, their series combination with the input source results in a total output voltage of +5Vin across the load. During this mode, both C1 and C3 discharge and supply energy to the load together with the DC source. The circuit diagram of Mode 5 is shown in the below figure 6.

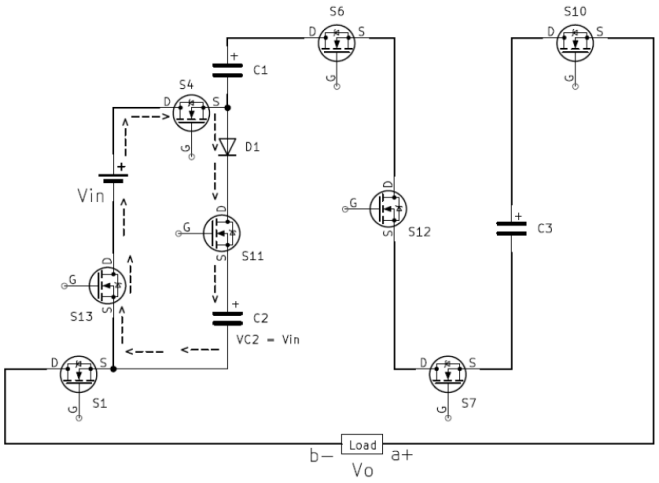

Fig. 6 Circuit Diagram of Mode-5 Operation

Mode 6 operation: In mode 6 the switching configuration connects the DC input source Vin and all three switched capacitors C1, C2, and C3 in series across the load. Since capacitors C1 and C2 are charged to Vin and capacitor C3 is charged to 3Vin in earlier operating states, their cumulative series connection with the input source produces the maximum output voltage level of +6Vin. During this mode, all three capacitors discharge simultaneously and transfer their stored energy to the load along with the input source. The circuit diagram of Mode 6 is shown in the below figure 7.

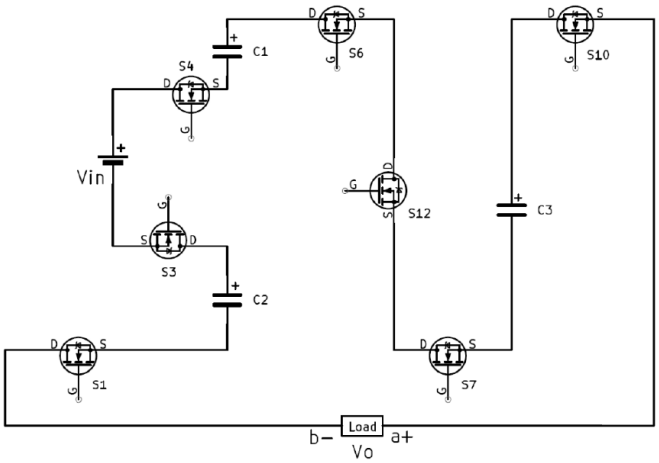

Fig. 7 Circuit Diagram of Mode-6 Operation

During State 6, all three capacitors C1, C2, and C3 are connected in series with the input DC source and discharge simultaneously through the load. In this condition, the stored energy of each capacitor is fully utilized, and their combined voltages add to the input source voltage, resulting in the maximum positive output voltage of the inverter. This simultaneous discharge marks the completion of the positive half-cycle and demonstrates the high voltage boost capability of the proposed switched-capacitor topology. In contrast, the negative output voltage levels, corresponding to States 8 to 13, are produced in a manner that is electrically symmetrical to the positive voltage states 1 to 6.

Mode 7 operation: In mode 7 the inverter operates in the zero-voltage mode, in which the output terminals are shorted

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through an appropriate combination of switches, resulting in zero output voltage across the load. During this state, the load current either freewheels through the antiparallel diodes or circulates through the conducting switches, depending on the nature of the load. This zero state provides a smooth transition between the positive and negative half-cycles of operation.

At the same time, capacitors C1 and C2 are connected in parallel with the DC input source Vin and are charged to the input voltage level. Capacitor C3 remains electrically isolated and does not participate in the charging or discharging process during this state. The charging of C1 and C2 during the zero-output condition plays a crucial role in maintaining the self-voltage balancing of the capacitors, ensuring that they are properly prepared for the subsequent operating states. The circuit diagram of Mode 7 is shown in the below figure 8.

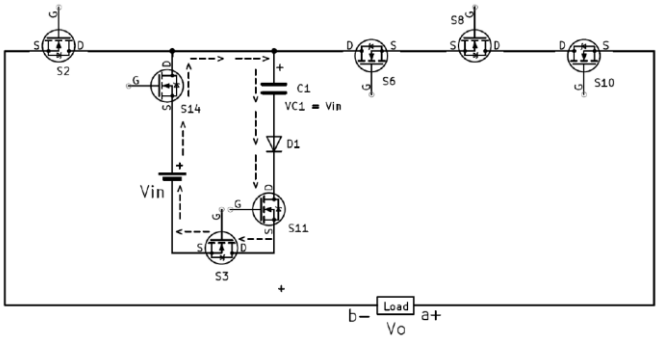

Fig. 8 Circuit Diagram of Mode-7 Operation

The switching states of the proposed 13-level switched-capacitor inverter along with the corresponding output voltage levels is shown in the below table. The inverter operates in thirteen distinct states during one fundamental cycle, enabling the generation of positive, negative, and zero voltage levels. Each state is defined by a specific combination of ON switches, which determines both the output voltage magnitude.

TABLE I: Switching states of the proposed inverter

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	Vo
	ON	ON		ON		ON			ON	ON				Vdc
ON			ON		ON		ON		ON	ON				2Vdc
ON		ON	ON	ON	ON	ON	ON		ON					3Vdc
ON					ON	ON			ON		ON	ON	ON	4Vdc
ON			ON		ON	ON			ON	ON	ON			5Vdc
ON		ON	ON		ON	ON			ON		ON			6Vdc
ON			ON	ON		ON		ON		ON				zero
ON			ON		ON		ON	ON		ON				-1Vdc
	ON	ON		ON		ON		ON		ON				-2Vdc
	ON	ON	ON	ON	ON	ON	ON	ON						-3Vdc
	ON			ON			ON	ON			ON	ON	ON	-4Vdc
	ON	ON		ON			ON	ON		ON	ON			-5Vdc
	ON	ON	ON	ON			ON	ON			ON			-6Vdc

C. *Modulation Technique*

NEAREST LEVEL MODULATION: Nearest Level Control (NLC), also known as the rounding method, is a time-domain modulation technique in which the inverter output voltage is generated by selecting the discrete voltage level that is closest to the instantaneous value of the reference signal. In this method, the reference output voltage is continuously compared with the available discrete voltage levels, and the level with the minimum deviation is chosen. Unlike space vector–based approaches, NLC directly operates on discrete voltage levels rather than space vectors.

Compared to Space Vector Control (SVC), which simultaneously regulates all three phases through optimal vector selection, NLC treats each phase independently. The control is implemented using sinusoidal reference signals that are phase-shifted by 120º, and the nearest voltage level is selected for each phase separately. The primary advantage of NLC lies in its simple and low computational requirement, as determining the nearest voltage level is significantly less complex than identifying the closest space vector. Consequently, the control strategy offers a straightforward and efficient implementation, where the output voltage level selection is reduced to a simple mathematical operation.

In Nearest Level Modulation, the reference sinusoidal voltage is normalized with respect to the DC source voltage and rounded to the nearest integer to determine the switching state. The inverter output voltage is then generated by multiplying the selected level index with the DC voltage. One of the key advantages of NLM is its low computational complexity. This makes NLM highly attractive for implementation on low-cost digital controllers such as microcontrollers and FPGAs.

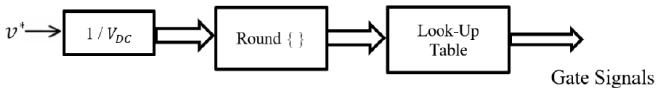

Fig. 9 Flow Diagram of Nearest Level Modulation Technique

As shown in the figure 9, the Nearest Level Control (NLC) technique resembles conventional staircase modulation, it does not provide direct control over the elimination of specific harmonic components. Due to this limitation, NLC becomes less effective for low-level and multilevel inverter applications, where lower-order harmonics are typically dominant. To overcome this drawback, an adaptive modulation approach is introduced by incorporating duty-cycle calculation into the Nearest Level Modulation (NLM) framework.

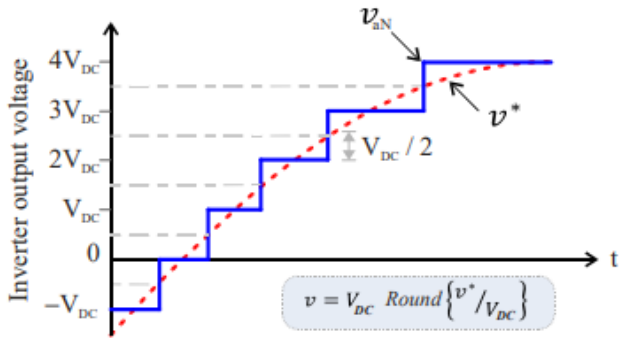

Fig. 10 Voltage Generation of NLM

In this process, the rounding operation produces a single-step transition between voltage levels, which induces a high rate of change in voltage (dv/dt). Since this method does not replicate the reference waveform through as it does not employ time-averaged synthesis, this approach is not categorized as a standard modulation method. Instead, it is regarded as an approximation method, appreciated for its simplicity and computational efficiency.

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III. SIMULATION RESULTS

The parameters used in the simulation is provided below:

Table II: Design Specification of the system

Parameters	Values
DC Voltage (Vin)	56V
Inverter output frequency (f)	50Hz
R Load Value	100Ω
L Load Value	100mH
Capacitor Values (C1, C2, C3)	4700µF
Switching frequency	50Hz
No. of switches used	14
Gate Control Method	Nearest Level Modulation

Table II summarizes the key simulation parameters used to evaluate the performance of the proposed 13-level switched-capacitor multilevel inverter. The DC input voltage is set to 56 V, which represents a low-voltage source typically available from renewable energy systems such as photovoltaic modules. Using the proposed switched-capacitor topology, the inverter achieves a voltage gain of six, resulting in a peak output voltage of approximately 323 V, thereby validating the inherent voltage-boosting capability of the circuit without employing an external DC–DC converter.

The proposed 13-level switched-capacitor multilevel inverter is simulated using MATLAB/Simulink to verify its operating principle, voltage boosting capability, and modulation performance under different load conditions. The simulation model integrates the power circuit, Nearest Level Modulation (NLM) control strategy, and load models within a unified framework.

A DC input voltage of 56 V is applied to the inverter, and the switching states are generated using the NLM technique operating at fundamental frequency (50 Hz). Based on the instantaneous value of the sinusoidal reference signal, the nearest available voltage level is selected, and the corresponding gate signals are generated through a predefined lookup table. These gate pulses are applied to the 14 power switches of the inverter to produce the required stepped output waveform. The switched-capacitor network consisting of capacitors C1, C2, and C3 is modeled with appropriate capacitance and voltage ratings to achieve the desired voltage boosting. During the simulation, the capacitors are charged and discharged in a controlled manner according to the switching states, enabling the generation of output voltage levels ranging from ±Vdc to ±6Vdc. The simulation results confirm that the capacitor voltages remain balanced around their rated values, validating the self-balancing nature of the proposed topology. Both resistive (R) and resistive–inductive (RL) loads are considered to evaluate the inverter performance under different operating conditions. The simulation of 13-level switched-capacitor MLI figure is shown below.

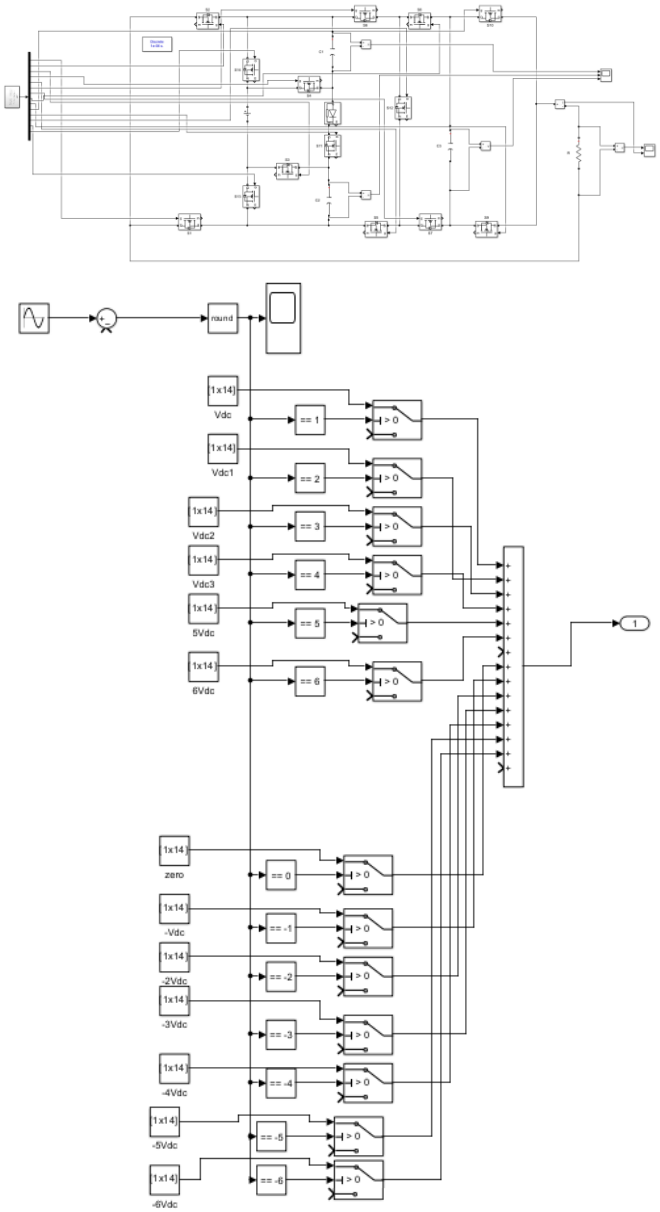

Fig. 11 Simulation of 13-level Switched Capacitor Multilevel Inverter

Resistive Load (R): The output current follows the instantaneous output voltage and directly reflects the 13-level stepped waveform. The capacitor charge-discharge cycle is unaffected by load impedance except for minor voltage drops due to internal resistances.

Inductive-Resistive Load (RL): The presence of inductance introduces a reverse current path, which must be accounted for during capacitor discharge. The inverter's switching sequence ensures that inductive kickback does not overcharge the capacitors, preserving self-voltage balance. The diode D1 provides a freewheeling path for the reverse current, protecting the switches and capacitors. This configuration allows the inverter to supply various types of AC loads reliably, while maintaining stable output voltage levels, minimal ripple, and self-balanced capacitor voltages, even under transient or step-load conditions.

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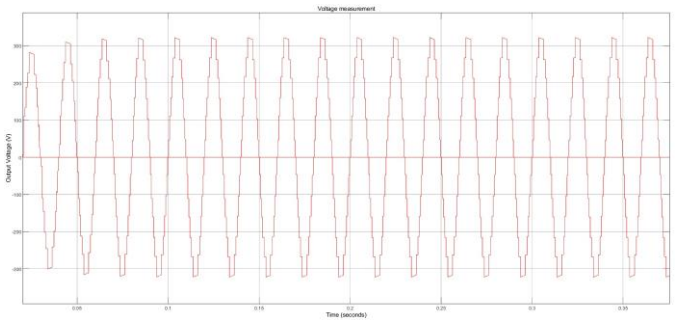

Fig.12 Output Voltage Waveform with R load

The simulated output voltage waveform of the proposed inverter under resistive load conditions is shown in the figure 12. As observed, the inverter generates a 13-level staircase voltage waveform consisting of six positive voltage levels, six negative voltage levels, and a zero level. The voltage steps range from −6Vdc to +6Vdc, resulting in a peak output voltage of approximately ±323 V, which confirms the six-times voltage boosting capability of the proposed switched-capacitor topology.

The waveform exhibits clear and symmetric step transitions in both the positive and negative half cycles, indicating proper switching operation and effective implementation of the Nearest Level Modulation (NLM) strategy. The equal step heights verify that the DC source and capacitor voltages are appropriately combined and balanced during operation. The absence of waveform distortion or voltage collapse demonstrates stable capacitor charging and discharging across all operating states.

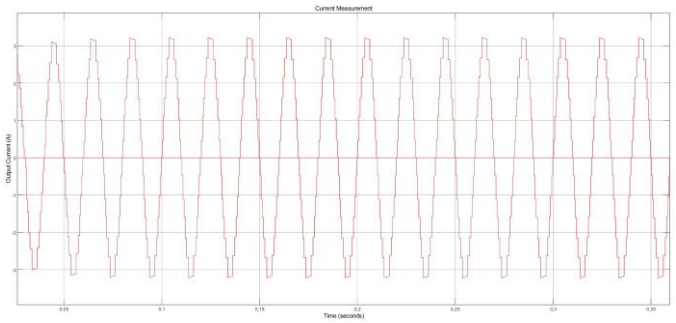

Fig.13 Output Current Waveform with R load

As shown in the figure 13, the simulated output current waveform of the proposed 13-level switched-capacitor multilevel inverter under R load condition. As observed, the current waveform is smooth and continuous, indicating stable operation of the inverter and effective power delivery to the load.

For the resistive load, the output current remains in phase with the output voltage, confirming linear load behavior and correct switching action. The stepped nature of the voltage waveform results in a near-sinusoidal current profile, as the load impedance filters out higher-order voltage harmonics. This demonstrates the advantage of multilevel operation in improving current waveform quality.

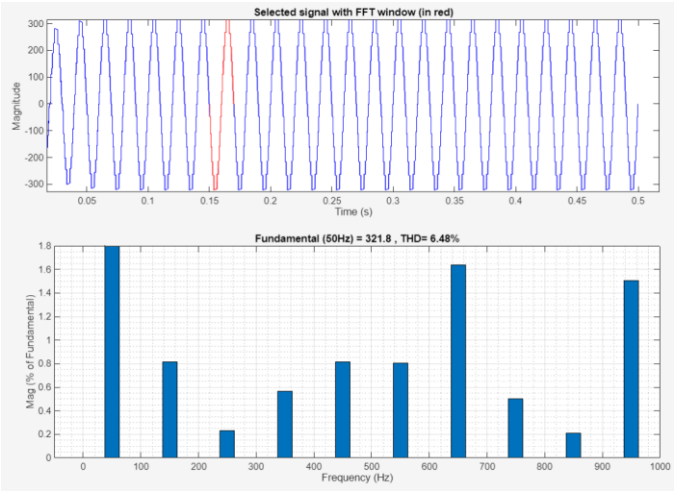

Fig. 14 Voltage THD of inverter with R load

As shown in the figure 14, the Fast Fourier Transform (FFT) analysis of the output voltage waveform of the proposed 13-level switched-capacitor multilevel inverter under resistive load conditions. The upper plot illustrates the selected steady-state voltage waveform window used for spectral analysis, while the lower plot presents the corresponding harmonic spectrum.

From the FFT results, the fundamental component is observed at 50 Hz with a magnitude of approximately 321.8 V, which closely matches the rated output voltage of the inverter. This confirms accurate fundamental voltage generation using the Nearest Level Modulation (NLM) strategy. The harmonic spectrum indicates that the dominant harmonic components are shifted toward higher-order frequencies, while lower-order harmonics are significantly suppressed.

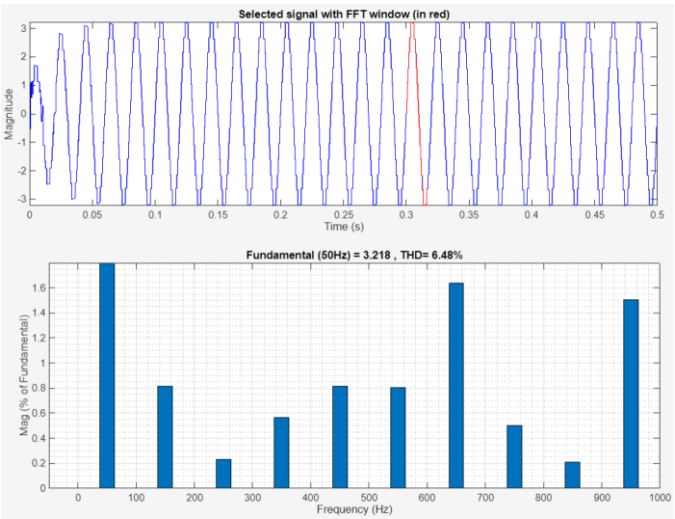

Fig. 15 Current THD of inverter with R load

As shown in the figure 15, the Total Harmonic Distortion (THD) of the output current for the proposed 13-level switched-capacitor multilevel inverter operating under a resistive load is evaluated using Fast Fourier Transform (FFT) analysis. The obtained current THD is approximately 6.48%, indicating a low level of harmonic distortion in the load current. The relatively low current THD value confirms the

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effectiveness of the Nearest Level Modulation (NLM) strategy.

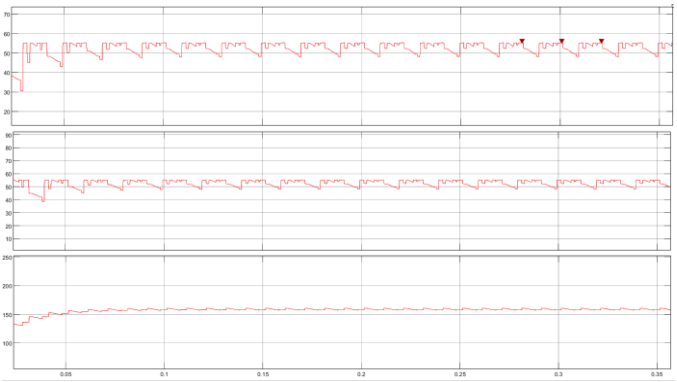

Fig. 16 Capacitor Voltage of VC1, VC2 and VC3

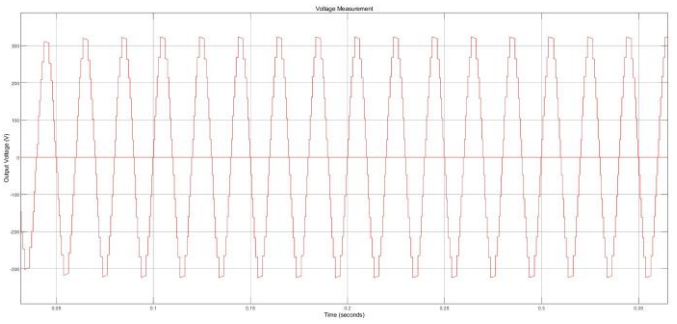

Fig.17 Output Voltage Waveform with RL Load

As shown in the figure 17, the simulated output voltage waveform of the proposed 13-level switched-capacitor multilevel inverter when supplying a resistive–inductive (RL) load. As observed, the inverter continues to generate a 13-level staircase voltage waveform with voltage levels extending from −6Vdc to +6Vdc, demonstrating that the output voltage remains largely unaffected by the presence of inductance in the load.

The stepped voltage profile maintains good symmetry in both the positive and negative half cycles, confirming correct switching operation and proper functioning of the Nearest Level Modulation (NLM) strategy. The peak output voltage of approximately ±323 V further validates the six-times voltage-boosting capability of the proposed topology.

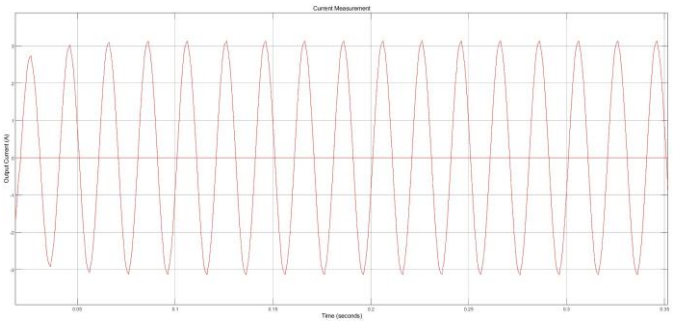

Fig.18 Output Current Waveform with RL Load

As shown in the figure 18, the output current waveform of the proposed 13-level switched-capacitor multilevel inverter supplying a resistive–inductive (RL) load is shown in the figure. As observed, the current waveform is smooth and nearly sinusoidal, which indicates effective filtering of the stepped output voltage by the inductive component of the load.

Due to the presence of inductance, the output current exhibits a phase lag with respect to the output voltage, which is a characteristic behavior of RL loads. The inductance limits the rate of change of current (di/dt), thereby reducing current ripple and smoothing out the high-frequency components present in the stepped voltage waveform.

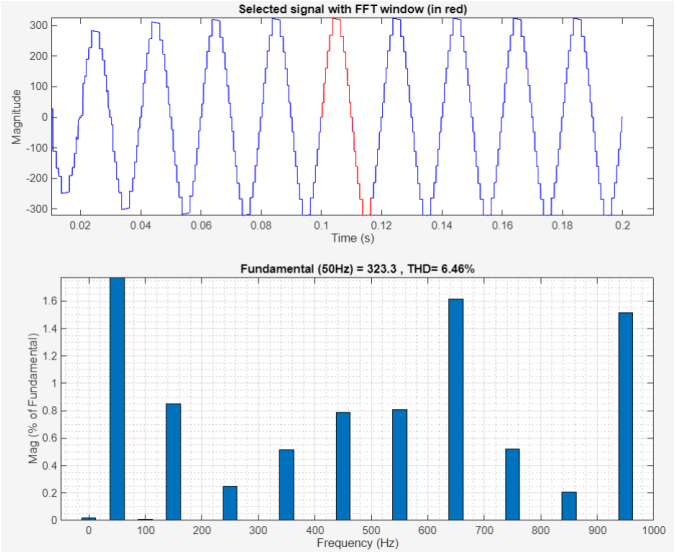

Fig. 19 Voltage THD of inverter with RL load

As shown in the figure 19, From the FFT results, the fundamental component is observed at 50 Hz with a magnitude of approximately 323.3 V, which confirms that the inverter successfully delivers the desired rated output voltage under RL loading conditions. The calculated total harmonic distortion (THD) of the output voltage is 6.46%, indicating a significant reduction in harmonic content due to the increased number of voltage levels and the use of Nearest Level Modulation (NLM).

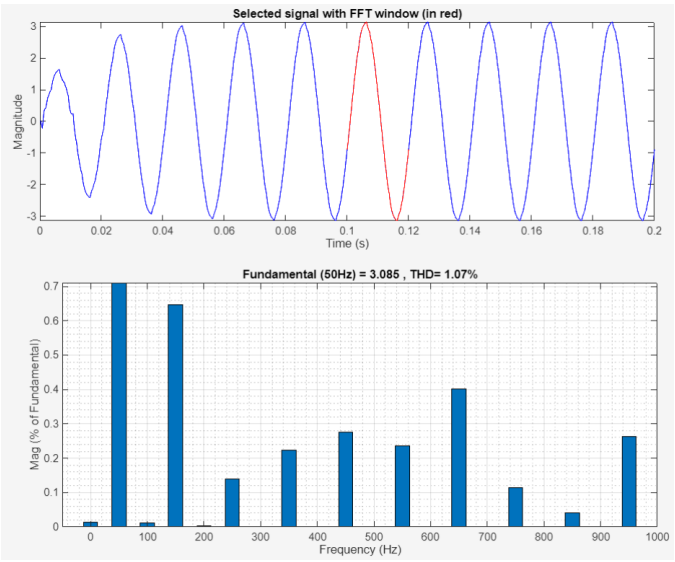

Fig.20 Current THD of inverter with RL Load

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Table III: Comparison of Vrms and Voltage Regulation (%)

Parameters	R Load	RL Load
RMS Voltage	227.5	228.3
Voltage Regulation (%)	0.9	0.74

IV. CONCLUSION

In this paper, a high step-up single-source switched-capacitor based 13-level inverter was designed and simulated using MATLAB/Simulink. The proposed topology successfully generates a multilevel AC output with a voltage gain of six while employing a reduced number of power switches and eliminating the need for a back-end H-bridge. The series–parallel charging and discharging mechanism of the switched capacitors ensures inherent self-voltage balancing without additional control or auxiliary circuits.

Nearest Level Modulation (NLM) was implemented due to its simple structure and low computational burden. Simulation results for both R and RL loads confirm that the inverter produces a staircase voltage waveform closely approximating a sinusoidal output. For an R load, the output voltage and current are in phase, whereas under RL load conditions, the current exhibits a smooth sinusoidal profile with a phase lag, validating proper inductive load operation. The voltage THD obtained is within acceptable limits for multilevel inverters, and the current THD is significantly reduced in the RL case due to the filtering effect of the inductance.

Overall, the results demonstrate that the proposed inverter topology offers high voltage boosting capability, improved waveform quality, reduced harmonic distortion, and lower device stress, making it suitable for medium- and high-voltage applications using low DC input sources.

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