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Design and Analysis of 6T SRAM in 45NM Technology

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Abstract **-- Many processors and system-on-a-chip (SoC) devices now employ Static Random Access Memory (SRAM) and CMOS technology, which necessitates new SRAM design innovations. SRAM bitcells are formed of lowest geometry devices in order to achieve high density and stay up with CMOS technology scaling; as a consequence, They are the first to feel the consequences of technological scaling. Simultaneously, the success of next-generation technology is dependent on the effective realisation of SRAM. As a result, To deal with the nano-regime issues, numerous SRAM bitcell topologies and array layouts have recently been suggested. Poor stability, process variation tolerance, device deterioration due to ageing, and soft mistakes are some of the primary issues in SRAM design. This chapter introduces and discusses the role of SRAM in the memory executive of a contemporary computer system and its peripheral circuitries. Different SRAM bitcell topologies and their benefits and drawbacks are also discussed.**

Keywords – SRAM, CMOS, Power Dissipation, Leakage Power

1. INTODUCTION

If a device's power is on, data is stored in SRAM (static RAM), a kind of random-access memory (RAM). Instead of being a dynamic RAM (DRAM), which must be continuously refreshed, SRAM does not have this requirement, resulting in better performance and lower power usage. However, SRAM is also more expensive than DRAM, and it requires a lot more space**.**

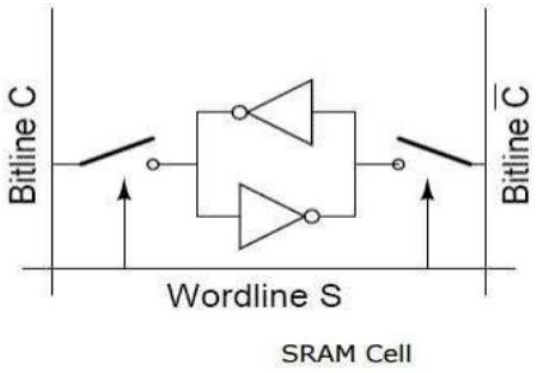
SRAM is commonly used for a computer's cache memory, such as a processor's L2 or L3 cache. It is not used for a computer's main memory because of its cost and size. Most computers use DRAM instead because it supports greater densities at a lower cost per megabyte (MB). However, SRAM is often used for other purposes. For example, it might be part of a RAM digital-to-analog converter (RAMDAC) on a computer's video or graphic card. It might also be used in a disk drive as buffer cache, in a peripheral such as a printer or LCD display, or in a network device such as router or switch.

SRAM can be found in other devices ways as well. For example, SRAM chips are often used in cell phones, wearables and other consumer electronics. They might also be embedded in medical products, which can include anything from hearing aids to body area networks that include multiple devices embedded in the body. In addition, SRAM is used in toys, appliances, automobiles, industrial equipment and a wide range of IoT devices.

2. WORKING OF 6T SRAM CELL

2.1 Working

Two inverters are linked back-to-back in a latch circuit with two stable working points to make up an SRAM data storage cell. Depending on how the two inverter latch circuits are set up, memory cell data is interpreted as logic '0' or '1'.



SRAM Cell

The memory cell is made up of two access transistors and two basic CMOS inverters coupled back to back. To connect a cell to the bit line columns associated with a word line, the access transistors must be triggered before a word line can be read or written on. One of the main advantages of this circuit design is that it consumes relatively little static power, which is effectively limited by a little leakage current.

In this instance, Six transistors make up the SRAM cell, thus the name 6T-SRAM cell. Two NMOS pass gate transistors (PG) are used to access the cell. Pass gates transistors that are linked to the bit lines are read or written to using the word line (BL and BLB). The input/output lines BL and BLB facilitate data reading/writing.

6T SRAM CELL OPERATIONS.

Until power is supplied, The SRAM memory cell holds the data. In preparation for reading, the word lines and bit lines are engaged. read mode is used to access an SRAM cell's stored data, either 0 or 1, is recovered. Turning on the word line enables Access transistors N3 and N4 are N3 and N4. The sensing amplifier looks for changes in the BL or BLB voltage. The sense amplifier is valuable for determining q's value.

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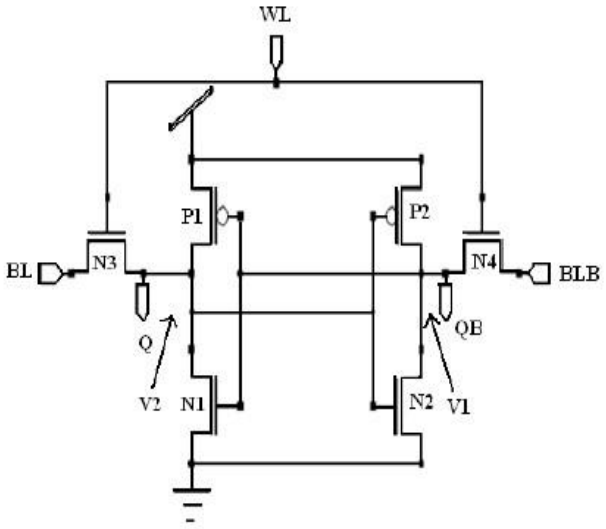

Figure 1: 6T SRAM cell

2.2 Analysis

2.2.1 Power Dissipation: In a CMOS circuit, overall power dissipation may be stated as the sum of three major components:

1. Dissipation of static power
2. Dissipation of dynamic power (when the circuit is switching)
3. Short-circuit power dissipation during transistor switching

2.2.2 Delay: Delay is the delay between input and output. Eliminating delay enhances system speed in every system. SRAM speed is calculated by read/write access times.

3. 6T SRAM CELL DESIGN

The 6T SRAM cell is made up of six MOSFETs, four of which are connected as CMOS inverters, where bits are stored as 1 or 0, while the other two, which operate as pass transistors, control the SRAM cell through the bit line.

3.1 Standby Mode: As a result, the pre-charge cycle in the SRAM circuitry will pull the Bit and Bit bar capacitors HIGH during this mode of operation. A "1" on W.L. means the access pass transistors for the SRAM cell are activated in Standby of Read "1" mode.

3.2 Read Mode: Q=1 and Qbar=0 should be preserved in the memory in this manner. Bit and Bit bar lines should be output lines, and the capacitance should be pre-charged, as well as the other lines, meaning the voltage at the capacitor point should be Vdd. Due to the voltage difference between Qbar and pt, the capacitor next to Qbar discharges. Consequently, There is a reduction in voltage on the bit bar, and the output value is **1.**

3.3 Write Mode**:** To receive data from a cell, a sensing amplifier sends a signal to a write driver, which acts as a receiver. To begin, write drivers are utilised to discharge the bit lines that are connected to them (BT and BTB). Pull up transistor (PU) tries to keep node "1" at a high potential as long as the word line (WL) is high, but the discharged bit line (DBL) pushes it down through the pointer line (PG).

During the write process, the memory block has the values Q=0 and Qbar=1, and W.L. is set to 1. ought to be one. Since we must write to memory, bits and are equivalent to I/P; hence, bitbar must be grounded.

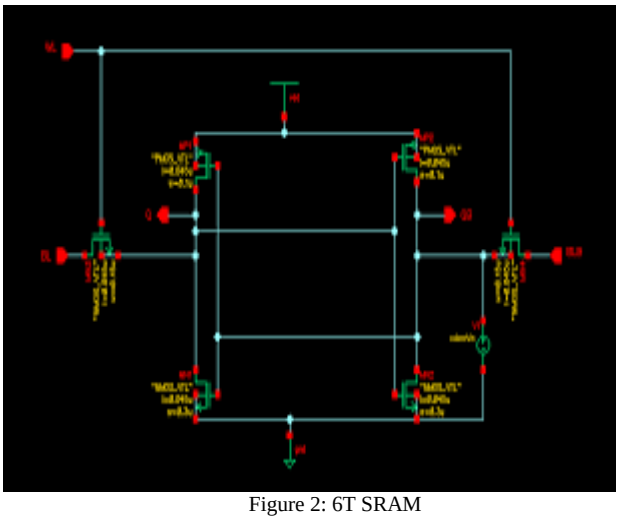

Figure 2: 6T SRAM

4. RESULT ANALYSIS

4.1 Read operation:

SRAM reads need a high word line. Memory must have some value to read. Example: Q=1 and Q=0 memory. To conclusion, emphasise the word line. Bit and bit bar output lines are pre-charged with Vdd. The circuit won't discharge since Q and bit are both high. When Q"=0 and When bit an is high, bit b will have a lower voltage because of a voltage difference. As a result, current will flow and the circuit will discharge. The sensing amplifier is linked to bit and bit b; it functions as a comparator;thus, the output is 1 when bit is low. As a result, when Q=1 was used as an input, the output was 1.

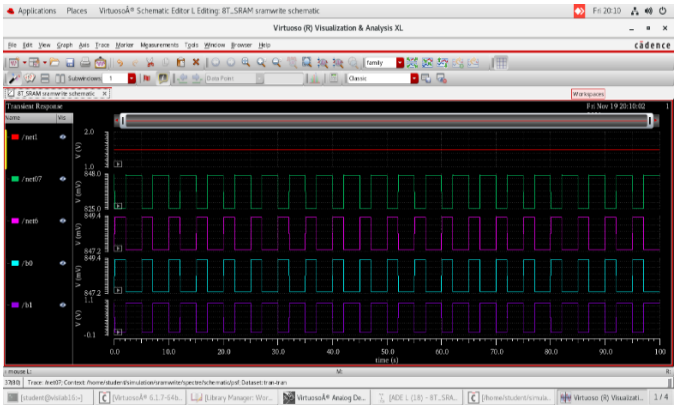

Figure 3: 6T SRAM Read Operation

4.2 Write Operation:

At the beginning of a write cycle, the bit value that needs to be written is written. Set the BL bar to 1 to insert a 0 on the bit lines. Reversing bit lines yields a 1. After saving a value, WL is confirmed. The bit line input-drivers are far more powerful than the cell's weak transistors, enabling them to

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easily overcome the cross-coupled inverters. In the proposed architecture, the write process is far more straightforward than the read operation. While the WL is being brought down, the writing operation begins by rising to VDD. Meanwhile, one of the BLs is being dragged to the ground, and the other is being held at VDD. When the node is powered on, Both N1 and N2 are connected to VDD. When node C is charged to VDD, N1 and N2 are also charged to VDD.

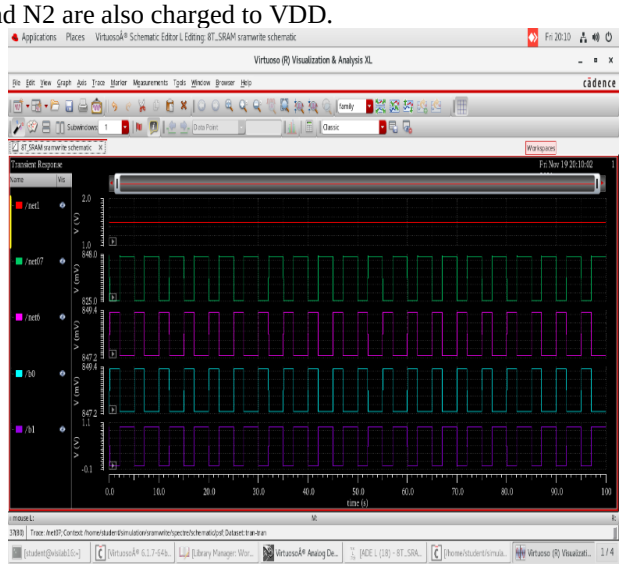

Figure 4: 6T SRAM cell Write Operation

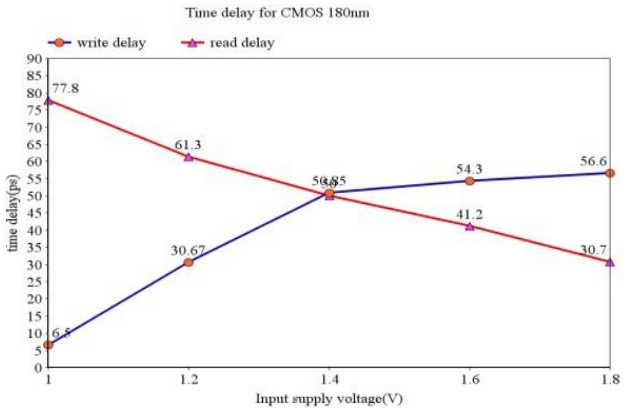

Figure 5: Time delay for CMOS

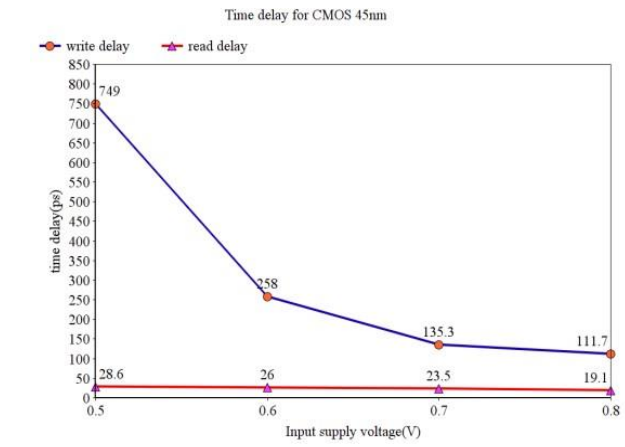

Figure 6: Time delay for CMOS 45nm

Technology	180nm	90nm	45nm
Power (Watts)	519.7n	59.58n	30.68n
SNM for read operation	0.35v	0.17v	0.14v
SNM for write operation	0.31v	0.07v	0.19v

Table: Performance Comparison between 6T SRAM cells in different nanometre technologies

5. CONCLUSION

The simulation in this work is carried out using the Cadence Virtuoso tool. The simulation is performed for a 6T SRAM cell at technology nodes of 180nm, 90nm, and 45nm.The design architecture shows speed improvements along with scaling of technology and delay time also decrease. Power dissipation result analysis are done in terms of power dissipation, delay and SNM.

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