Published by :
http://www.ijert.org

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

Design and Analysis of 1-Bit SRAM

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***Abstract*— SRAM (Static Random-Access Memory) is a memory component and is used in various VLSI chips due to its unique capability to retain data. This memory cell has become a subject of research to meet the demands for future digital electronics and communication systems. SRAM is a major data storage device due to its large storage density, less time to access and consumes less power. It does not require refreshing periodically which makes it the most popular memory cell among VLSI designers. Hence continuous work is going on for the better performance of SRAM cells.**

In this paper 6T SRAM cell circuit is designed for 1-Bit storage. The design is synthesized using the LTspice software tool and the analysis of important memory parameters like read access time, write access time, power and number of transistors is performed.

Keywords*— *CMOS technology; 6T SRAM Cell; 1-Bit SRAM; Simulation and results; Power; Read access time; Write access time.

I. INTRODUCTION

In today's technological changes, there is a drive to develop devices such as memory with low power and high speed. They have turned into a discriminating part of numerous VLSI chips. A memory module is a physical device which is used to store programs or data on a permanent or temporary basis for use in digital electronic systems. SRAM (Static Random-Access Memory) is a static memory cell widely used in various electronic systems, significantly in components used for cache memory in microprocessors, mainframe computers, engineering workstations, and memory in hand-held devices due to high speed and low power consumption [2]. SRAM is a type of semiconductor memory using bi-stable latching circuit to store each bit and exhibits data remanence i.e., residual of data even after repeated deletion attempts, but is still volatile i.e., data is lost when the memory is not powered. Fig. 1 shows a general SRAM array structure, the main SRAM building blocks are - SRAM cell, pre-charge circuit, write driver circuit, sense amplifier circuit and row decoder [2].

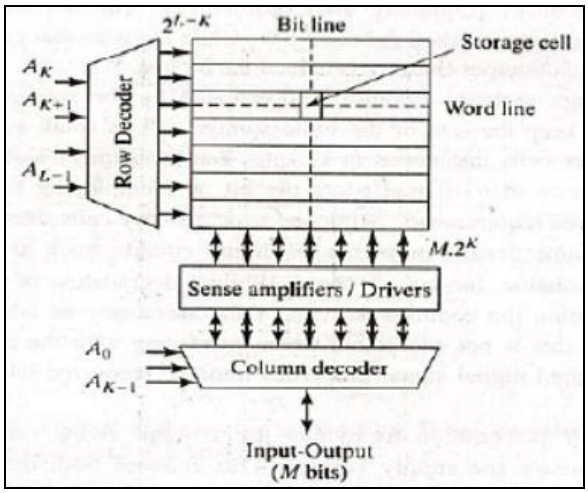

Fig. 1. General SRAM Array Structure

SRAMs can be organized as word-oriented where each address addresses a word of *n* bits (where the popular values of n include 8, 16, 32, or 64) or a bit-oriented where each address accesses a single bit. Column decoders or column MUXs (YMUXs) addressed by Y address bits allow the sharing of a single sense amplifier among 2,4 or more columns. A SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation which impose contradicting requirements on SRAM cell transistor sizing. SRAM cell transistor ratio's that must be observed for successful read and write.

This paper reviews section wise as: In this section, importance and general structure of memory array is discussed. Section II discusses detailed design of peripherals and SRAM. Design and operations of SRAM along with peripherals are presented in section III. Results and Discussions are given in section IV. Finally concluding remarks are made in section V.

II. SRAM AND ITS PERIPHERALS

To get required frequency of operation, efficient peripherals has to be designed, since the memory core exchanges performance and reliability for diminished area, memory plan depends exceedingly on the peripheral hardware to recuperate both speed and electrical integrity. Fig. 2 shows memory cell with monolithic peripheral connectivity. The

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

basic architecture of SRAM includes memory arrays arranged in rows and columns of memory cells called word-lines and bit-lines, respectively with support circuitry to decode addresses, and implement the required read and write operations. Each memory cell has a unique location or address linked to a particular data input/output pin. The SRAM to operate in reading mode and write mode should have "readability" and "write stability" respectively [4]. The complete SRAM array includes peripheral components such as pre-charge circuit, memory cell, write driver circuit, sense amplifier circuit designed and integrated with LTspice software.

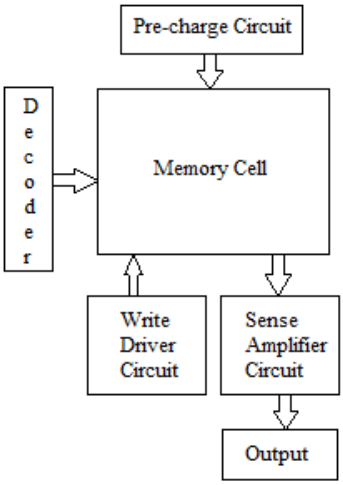

Fig. 2. SRAM with monolithic peripheral

III. SRAM DESIGN AND OPERATION

A. *Pre-charge Circuit*

The pre-charge circuit is one of the vital components that is constantly utilized within the SRAM cell. The job of the pre-charge is to charge the bit-line and bit-line bar to VDD. As shown in Fig. 3, the transistors M1 and M2 will pre-charge the bit-lines while the transistor M3 will equalize them to ensure both bit-lines within a pair are at the same potential before the cell is read [3].

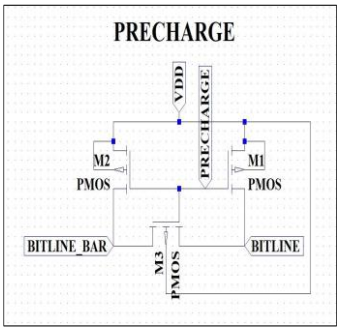

Fig. 3. Pre-charge Circuit Schematic

The pre-charge circuit empowers the bit-lines to be charged high at all times aside from throughout reading and write operation. For every section single pre-charge circuit is utilized.

B. *2:4 Decoder Circuit*

Large memory arrays can have hundreds of different rows of cells. Since only one word of data is selected at a time, having every address assigned to only one pin is a waste of space. To decrease the number of pins needed to choose an address, most memory chips use address decoders. Address decoders use combinations of logic 1's and 0's on the input to choose a unique address. This allows n pins to access 2n locations. In certain cases, pre-decoders may also be added to further reduce the number of pins needed to access each address. Some synchronous chips will also integrate the clock signal with the address decoders so that cells are only selected during a certain portion of the clock cycle. The 2:4 decoder truth table is given in Table I. Circuit schematic and simulation waveform are shown in Fig. 4 and Fig. 5 respectively.

TABLE I. 2:4 DECODER TRUTH TABLE

S0	S1	Y0	Y1	Y2	Y3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

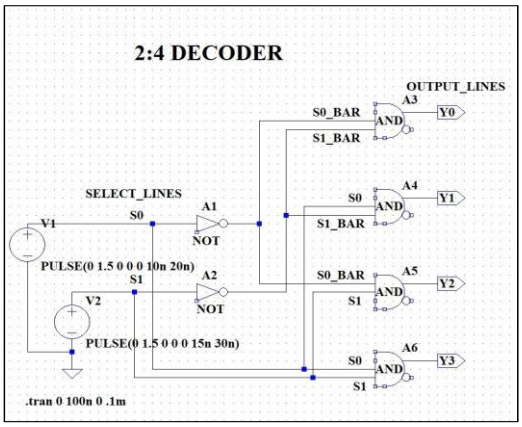

Fig. 4. 2:4 Decoder Circuit Schematic

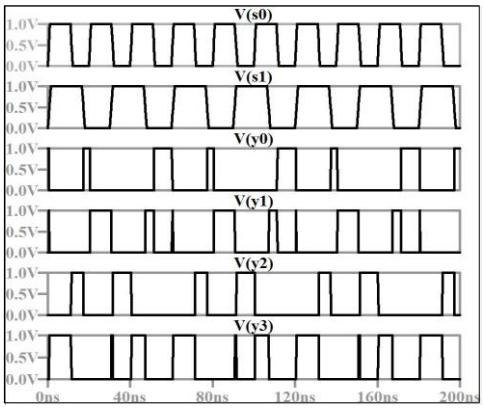

Fig. 5. 2:4 Decoder Simulation

C. *Write Driver Circuit*

The driver circuit also known as a write driver is one of the basic components in the memory design circuit. The job of the driver is to bring the bit-line and bit-line bar to the ground potential which are initially being charged to maximum

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

supply voltage VDD with pre-charge circuit. The driver gets enabled by the write enable which is connected in the upper part as shown in Fig. 6. The function of the SRAM write driver is to write input data to the bit-lines when Write Enable (WRITE_EN) signal is enabled; otherwise, the data is not written onto the bit-lines. It has two nMOS transistors being connected back to back with fascinated manner, also two inverters in the upper part. The two logics are given to the two points of the junction of the nMOS i.e., 0 and 1. The bit-line which is nearer to the 0 logic, gets discharged first after that its logic gets inverted. This way the bit-line and bit-line bar gets discharged to the ground. The voltage difference between bit-line and ground, bit-line bar and ground are zero. Another data can be easily retrieved by the memory cell when more amount of data is to be accessed [2]. Only one write driver is needed for each SRAM column [1].

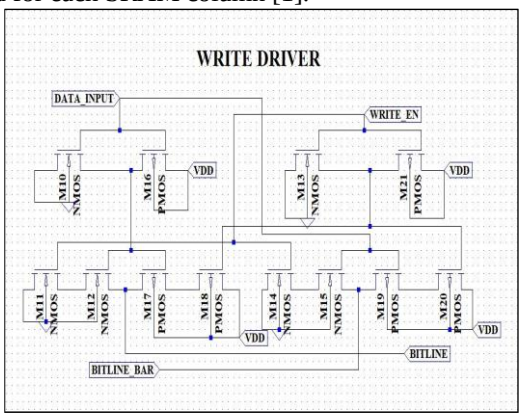

Fig. 6. Write Driver Circuit Schematic

D. Sense Amplifier Circuit

Sense amplifiers are vital components in the memory design. The sense amplifier's primary job is to do amplification of the voltage difference that is being produced on the bit-line and bit-line bar at the time of operation. It senses the bit-line and bit-line bar for proper monitoring action. It improves the read and write speed of the memory cell. It's another job is to reduce the power needed for the operation. A sense amplifier is present in every column of the SRAM array [1]. The sense amplifier circuit as shown in Fig. 7 uses two cross coupled inverters and access transistors connecting the inverter inputs to the bit-lines. The read operation begins by pre-charging and equalizing both the bit-lines, with simultaneously biasing the latch-type sense amplifier in the high-gain meta-stable region by pre-charging and equalizing its inputs. And then to read a particular word from the SRAM array, the corresponding row is selected by enabling the word-line. Once a sufficient voltage difference is built between the bit-lines, the sense amplifier is enabled by read enable (READ_EN) signal. The sense amplifier will sense which bit-line is heading towards high voltage and which bit-line is heading towards ground potential and then a full voltage swing is obtained at the output [3].

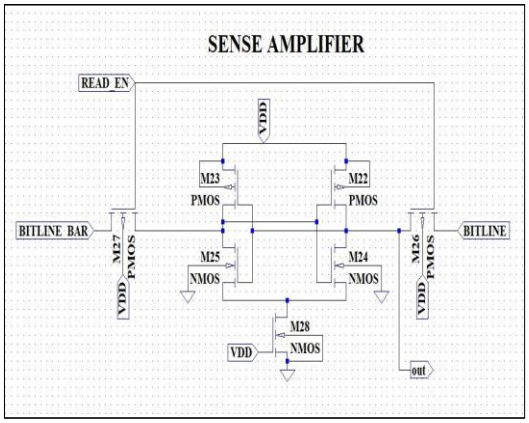

Fig. 7. Sense Amplifier Circuit Schematic

E. 6T SRAM Cell

The 6T SRAM cell design can be done by two back to back cascaded CMOS inverters which is advantageous i.e., this topology has good noise immunity because of its large noise margin and low static power dissipation due to less leakage current in cell. It consists of six transistors, in that two nMOS pass transistors for access as shown in Fig. 8. It has high speed, better noise immunity, and lesser area than other SRAM cells.

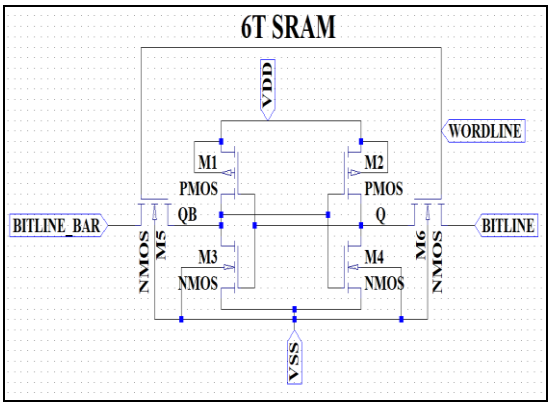

Fig. 8. 6T SRAM Schematic

Each bit in SRAM is stored on two cross-coupled inverters formed by four transistors and has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control a storage cell during reading and writing operations. Access to the cell is enabled by the word-line (WORDLINE in Fig.) which controls the two access transistors M5 and M6. The cell also has two bit-lines that control both the input and output of the data from the cell. The first bit-line known as bit-line, holds the same value that is stored in the cell. The second bit-line, known as bit-line bar or bit-line not, holds the inverse of the value that is stored in the cell [12].

Operation of SRAM cell can be categorized into three different states: Standby Mode-when circuit is in ideal state, Read Mode-when data has to be extracted and Write Mode-when data has to be updated.

a) Standby: When the word-line is not selected, the access transistors M5 and M6 disconnect the cell from the bit-lines. The two cross coupled inverters formed by transistors

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 9 Issue 09, September-2020

M1-M4 will continue to reinforce each other as long as they are provided by supply.

b) Reading: Consider the memory content as a logic 1 stored at Q. The read operation is performed by using the sense amplifiers that pull the data and produce the output. The row decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers.

c) Writing: A write cycle begins by applying the value to be written to the bit-lines. If we wish to write a 0, we would apply a 0 to the bit-lines, i.e., setting BL bar to 1 and BL to 0. A logic 1 is written by inverting the values of the bit-lines. Word-line is then asserted and the value that is to be stored is latched in [3].

F. 1-Bit 6T SRAM

The following configuration of SRAM arrays was designed and analyzed using the Standard 6T, 5T and 4T SRAM cells. A 1-Bit 6T SRAM schematic is shown in Fig. 9. Various peripheral components of the SRAM structure were simulated using LTspice software tools. The signals used in the simulation results: 'pre-charge' from the pre-charge circuit, 'word-line' from 6T SRAM circuit, 'write_en' corresponds to write enable signal from the write driver circuits, 'bit-line' and 'bit-line bar' acts as input or output based on write/read operation, 'q' and 'qb' corresponds to the storage nodes Q and QB of 6T SRAM during write operation. 'read_en' corresponds to the read enable signal given to the sense amplifier circuits and 'out' signal gives the output of reading operation from sense amplifier circuit.

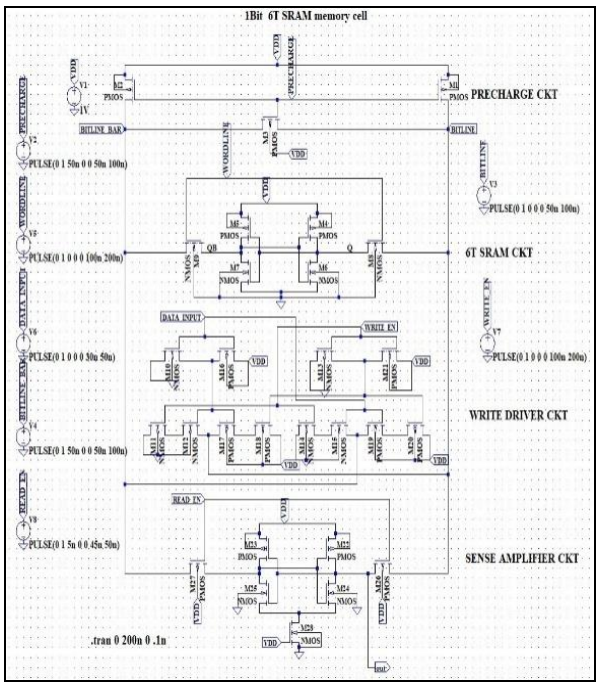

Fig. 9. 1-Bit 6T SRAM Schematic

IV. RESULTS AND DISCUSSIONS

The functionality write/read operation of 1x1 (1-Bit) 6T SRAM cell is shown in Fig. 10. When word-line=1, Write/Read operation takes place. When word-line=0, Hold state as shown in Fig. 10. Write 1 and Write 0 is performed during the write operation. Read 1 and Read 0 is performed during the read operation.

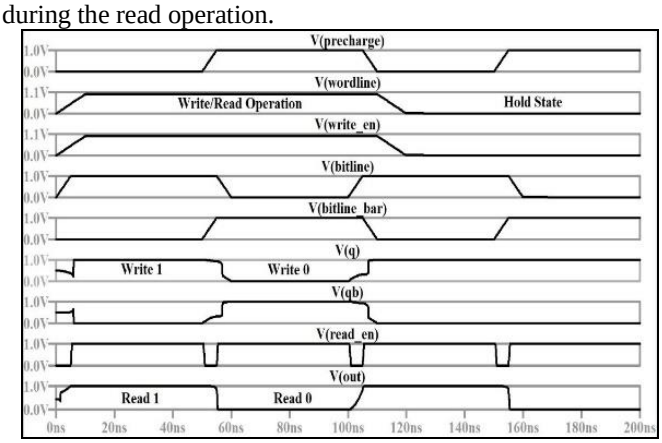

Fig. 10. 1-Bit 6T SRAM Write/Read Operation

Access time is the most important parameter for SRAM operation which is the propagation delay in getting proper SRAM operation. The Read Access time is the time measured from the point at which the READ_EN signal reaches 10% of VDD to the point at which the output signal becomes +/- 10% VDD of the required logic value. The Write Access time is the time measured from the point at which WRITE_EN reaches 50% of VDD to the point at which the storage node of the cell reaches 50% of VDD [1]. Read access time, write access time, power, and the number of transistors for 1-Bit 6T, from the simulation we found number of transistors required for 1-Bit storage and access is 28, the read access time 3.09(ns), write access time 2.07(ns) and power dissipation 6.55(µW).

V. CONCLUSION

All the desired outputs produced are stated and tabulated. Parameter analysis from the 6T has got less read and write access time when compared with 5T and 4T SRAM cells. Less access time indicates faster memory operation. The results can be used to select SRAM cell topology to design and fabricate memory chips which are best suitable for a different type of application. We can design 4x4(16-bit), 16x16(256-bit), 32x32 SRAM cells in CMOS technology. Further study and analysis of extracted parameters and its effects on circuit functionality will prove beneficial in including the cell to a standard cell library.

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Vol. 9 Issue 09, September-2020

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