Delay and Power Optimization of Memristor based basic Sequential Circuit Element

Joy Chowdhury, J. K. Das, N. K. Rout
Faculty of School of Electronics Engineering,
KIIT University, Bhubaneswar

Paulami Roy
School of Electronics Engineering,
KIIT University, Bhubaneswar

***Abstract*— The invention and successful fabrication of the memristor forced nano scale designs to start thinking beyond the scope of the conventional MOSFETS or rather the use of transistors as a whole. Memristors have a history mechanism which enables storage operations along with the inherent bipolar resistive switching property. Various existing mathematical models give shape to a implementable prototype of memristors which can be further implemented and tested in suitable circuits thus determining some crucial circuit parameters and how they differ from the traditional transistor based designs. In this paper D- flip flop has been proposed with the aid of Memristors using MRL(Memristor Ratioed Logic)and a few critical parameters such as delay, power, gate count etc have been calculated and studied. The simulations were run using Verilog-AMS and Virtuoso IC6.1.6 simulator.**

Keywords - D flip flop, Delay, Linear model, Memristors, Power.

I. INTRODUCTION

In 1970 Leon Chua had first postulated the concepts of memristors in [1].Since only the theoretical formulation existed it was thought to have great potential until May 2008 when it was successfully fabricated in HP Labs. The memristor was considered as the fourth fundamental passive two terminal circuit element which redefined many of the concepts underlying basic circuit theory [3]. The memristor device is actually fabricated using thin film TiO_2 variably doped and sandwiched between two Platinum (Pt) electrodes againCst which the bias voltages can be applied. The doping of the thin film TiO_2 is actually in the form of oxygen vacancies which are mobile in nature and help in charge conduction within the memristive devices [2]. The memristor's mathematical function establishes a link between the magnetic flux (which is integral of voltage) and the electric charge between the two plates of the device which is represented as memristance (M).

(1)

The relation between terminal voltage and current flowing across a memristor is given as:

(2)

Where it can be seen that the Memristance is function of charge which is in turn a function of time.

II. MATHEMATICAL MODEL AND MRL

The memristor has the physical property of switching electrically between on and off states each having a variable doping concentration. The doped area has a high resistance value R_{on} while the undoped area has a resistance R_{off} which can be variably switched depending on the conditions of the bias voltage[6]. This kind of a model is referred to as thee linear ion drift model as proposed in [5]. In this model the consideration for non linear phenomenon in the ion drift is very less. So that is compensated by the use of a Window function which helps to introduce substantial amount of non-linearity as well as limit the movement of the ions under drift within the boundaries of the nano - scale device. Several kind of window functions have been described and implemented each having its own advantages and disadvantages tagging along [14]. Several other complicated models had been proposed which were found to be better in terms of non-linearity and even performance of the device such as the Simmons Tunnel Barrier Model, TEAM model etc.

III. PROPOSED DESIGN OF D- FLIP FLOP

Design of Sequential Logic using memristors has not been explored much. So In this paper we propose a design of D- flip flop which is widely used in almost all digital architectures ranging from counters, shift registers, buffers, and any storage element. Memristors are appropriate for the design of sequential circuit as the is no need to define the previous state explicitly. Due to its history remembering mechanism even when there is no power it can still latch on to its previous value[15]. This non volatile nature can be exploited in the long run. Also here a linear ion drift model based memristor is used which utilizes trigonometric non-linearity in the window function.

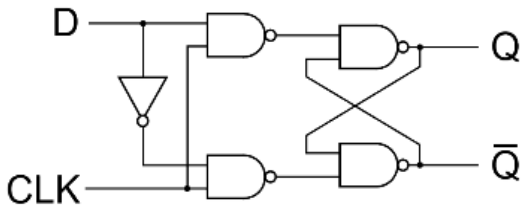

Fig. 1. D- Flip Flop

Now this circuit was implemented in CMOS 180 nm technology in figure 2, and the few critical design metrices were checked. then the same circuit was implemented using memristors and the performance parameters were checked. Then another modification was implemented. Instead of using the NAND gates in the first stage simple AND gates were used and in the second stage NOR gates were used. This also required the inversion of the output terminals Q and Qb respectively. A simple mathematical relationship establishing

this fact can be given using basic laws of boolean algebra. In NAND based D- flip flop, the non inverting output is given as :

$$Q = \overline{(\overline{(D.Clk)}.\bar{Q})} \xrightarrow{yields} Q = \overline{(\bar{d}.\bar{Q} +}$$

While, in case of NOR based D-flip flop the inverting and non-inverting terminals are interchanged because of the realization of NOR using NAND as follows:

$$\bar{Q} = \bar{Q}.\overline{(d.clk)} \xrightarrow{yields} \bar{Q} = \bar{Q}\,.\bar{d} + \bar{Q}.\overline{clk}$$

Hence the modification and its utilization is suitably justified.

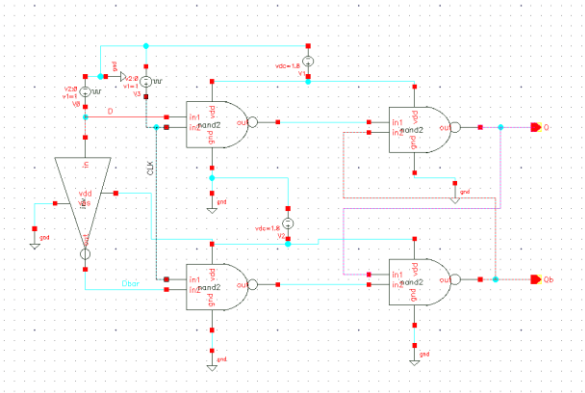

Fig. 2. Schematic of 180nm Transistor based D flip flop

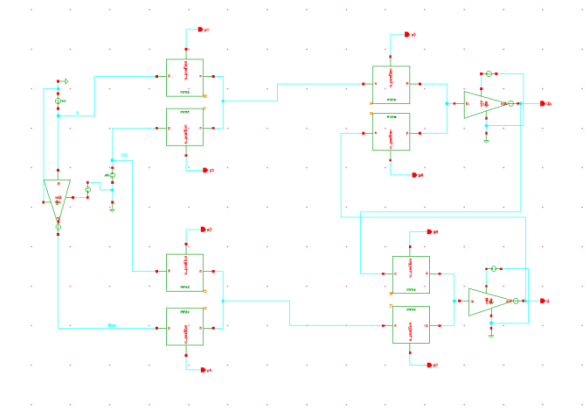

Fig.3. Schematic of Memristor(L=3nm) based D flip flop

IV. RESULTS

The 180 nm D flip flop circuit was simulated and the output waveform was observed after setting proper conditions to determine the previous stage logic.

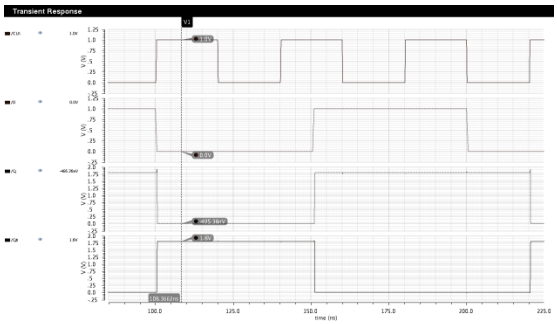

Fig. 4. Input-output waveform of D flip flop

Clock to Q delay = 0.379 ns
D to Q delay = 60.08 ns
Average power dissipation = 108.7 µW

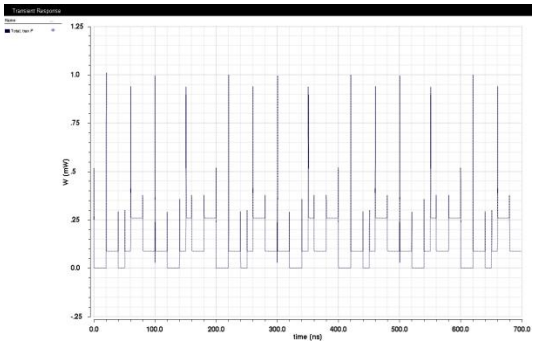

Fig. 5. Transient Power Analysis

Now for memristor based flip flop design using MRL logic CMOS inverter is used for logic inversion in case of NOR gates. Also here there is no explicit need to set the logic states for the previous states in the outputs .

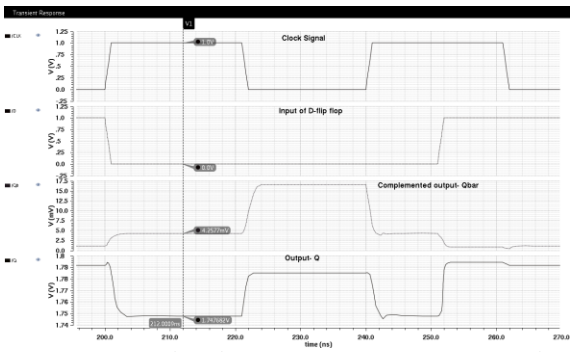

Fig. 6. Output Waveform for Memristor(L=3nm) based D Flip flop.

Clock to Q delay = 0.8312 ns
D to Q delay = 48.98 ns
Average Power Dissipation = 69.49 µW

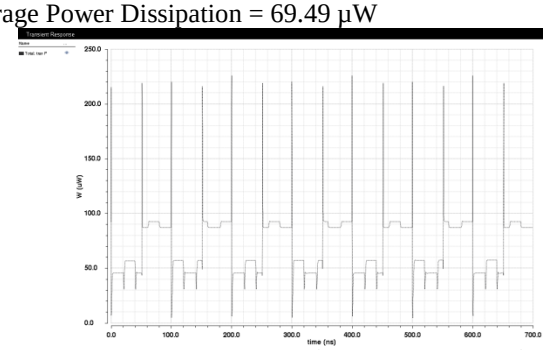

Fig. 7. Transient Power Analysis of Memristor based Flip flop

V. CONCLUSION

From the simulation results it is evident that the proposed design performs better than the conventional architectures with respect to power dissipation; the delay is optimized without having to go for significant trade- off . Also this design is independent of technology. There are some logic degradation due to the use of cmos inverters in the intermediate stages. That can be rectified using higher

voltage values to define the high and low logic levels. Table 1 Given below contains the comparison of the two designs.

TABLE I. COMPARISON OF MEMRISTOR BASED FLIP FLOP ARCHITECTURE WITH THE CONVENTIONAL ONE.

Design Name	Clk to Q delay (ns)	D to Q delay (ns)	Average Power Dissipation (µW)
CMOS based D Flip Flop	0.379	60.08	108.7
Memristor based D flip flop	0.8312	48.98	68.49

Here in this paper it is very difficult to show comparison with any existing reference paper because in most of the works low power techniques have been applied or master slave or gating configuration has been implemented. In almost all cases the configuration used in is more complex than the one shown in this paper. This design has been taken up only to highlight the elusive properties of a newly invented device i.e the Memristor.

VI. REFERENCE

[1] Chua, L.O., "Memristor- the missing circuit element", IEEE Trans. Circuit Theory, 1971, vol. CT-18, no. 5, pp. 507-519.
[2] Chua, L.O. and Kang, S.M.,"Memristive devices and systems‖", Proceedings of the IEEE, 1976, vol. 64, no. 2, pp. 209-223.
[3] Frank Y. Wang, "Memristor for introductory physics", arXiv:0808.0286vl [physics.class-ph] 4Aug2008.
[4] S.Thakoor, A. Moopenn, T. Daud, and A.P. Thakoor, "Solid-state thin-film memistor for electronic neural networks", Journal of Applied Physics, vol. 67, March 15, 1990, pp. 3132-3135
[5] Dimitri Strukov, Gregory Snider , Duncan Stewart , and Stanley Williams, "The missing memristor found", Nature.
[6] A. G. Radwan , M. Affan Zidan and K. N. Salama, "On the Mathematical Modeling of Memristors", International Conference on Microelectronics 2010.
[7] Chris Yakopcic , "A Memristor Device Model", IEEE Electron Device Letters, Vol.32, No.10, Oct 2011.
[8] Y. N. Joglekar and S. J. Wolf, "The Elusive memristor: Properties of basic electrical circuits," Eur. J. Phys., vol. 30, no. 4, pp. 661–675, Jul. 2009.
[9] Z. Biolek, D. Biolek, and V. Biolkova, "SPICE model of memristor with nonlinear dopant drift," Radioengineering, vol. 18, no. 2, pp. 210–214, Jun. 2009.
[10] T. Prodromakis, B. P. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with non-linear dopant kinetics," IEEE Trans.Electron Devices, vol. 58, no. 9, pp. 3099–3105, Sep. 2011.
[11] E. Lehtonen and M. Laiho, "CNN using memristors for neighborhood connections," in Proc. Int. Workshop Cell. Nanoscale Netw. Their Appl., Feb. 2010, pp. 1–4.
[12] J. G. Simmons, "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film," J. Appl. Phys., vol. 34, no. 6, pp. 1793–1803, Jan. 1963.
[13] E. Lehtonen, J. Poikonen, M. Laiho, and W. Lu, "Time-dependency of the threshold voltage in memristive devices," in Proc. IEEE Int. Symp. Circuits Syst., May 2011, pp. 2245–2248.
[14] Shahar Kvatinsky, Eby G. Friedman, Avinoam Kolodny, "TEAM: ThreEshold Adaptive Memristor Model", IEEE Transactions on Circuits and Systems-I, vol.60, no.1, jan-2013.
[15] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching dynamics in titanium dioxide memristive devices," J. Appl. Phys., vol. 106, no. 7, pp. 1–6, Oct. 2009.